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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zlp32300h2832c00tr

Architectural Overview

Zilog's Crimzon[®] ZLP32300 is an OTP-based member of the MCU family of infrared microcontrollers. With 237 B of general-purpose RAM and 8 KB to 32 KB of OTP, Zilog's CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Crimzon ZLP32300 architecture (see [Figure 1](#) on page 3) is based on Zilog's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8[®] CPU offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations:

1. Program Memory
2. Register File
3. Expanded Register File

The register file is composed of 256 Bytes of RAM. It includes four I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Crimzon ZLP32300 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see [Figure 2](#) on page 4). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

► **Note:** *All signals with an overline, “ $\overline{}$ ”, are active Low. For example, $\overline{B/W}$, in which *WORD* is active Low, and $\overline{B/W}$, in which *BYTE* is active Low.*

Power connections use the conventional descriptions listed in [Table 1](#).

Table 1. Power Connections

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

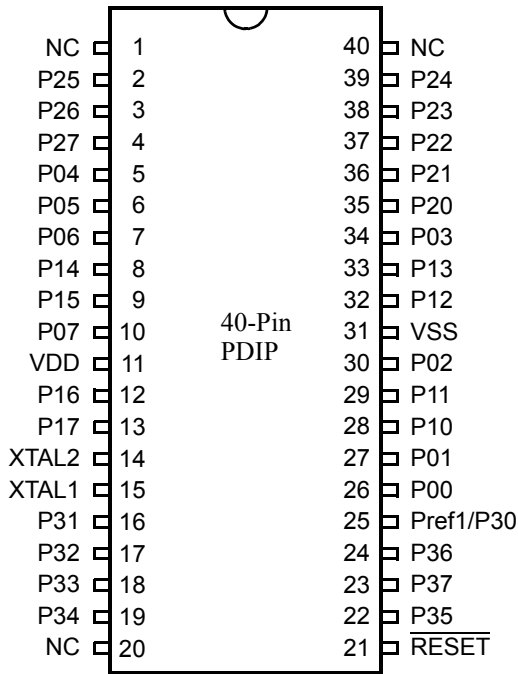


Figure 5. 40-Pin PDIP Pin Configuration

```

LD                                R1, 2                                ; CTR2→CTR1

LD                                RP, #0Dh                            ; Select ERF D
for access to bank D                                                    ; (working
register group 0)
LD                                RP, #7Dh                            ; Select
expanded register bank D and working                                   ; register
group 7 of bank 0 for access.
LD                                71h, 2
; CTRL2→register 71h
LD                                R1, 2
; CTRL2→register 71h

```

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see [Table 7](#) on page 27) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (see [Figure 15](#)). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

► **Note:** *Working register group E0–EF can only be accessed through working registers and indirect addressing modes.*

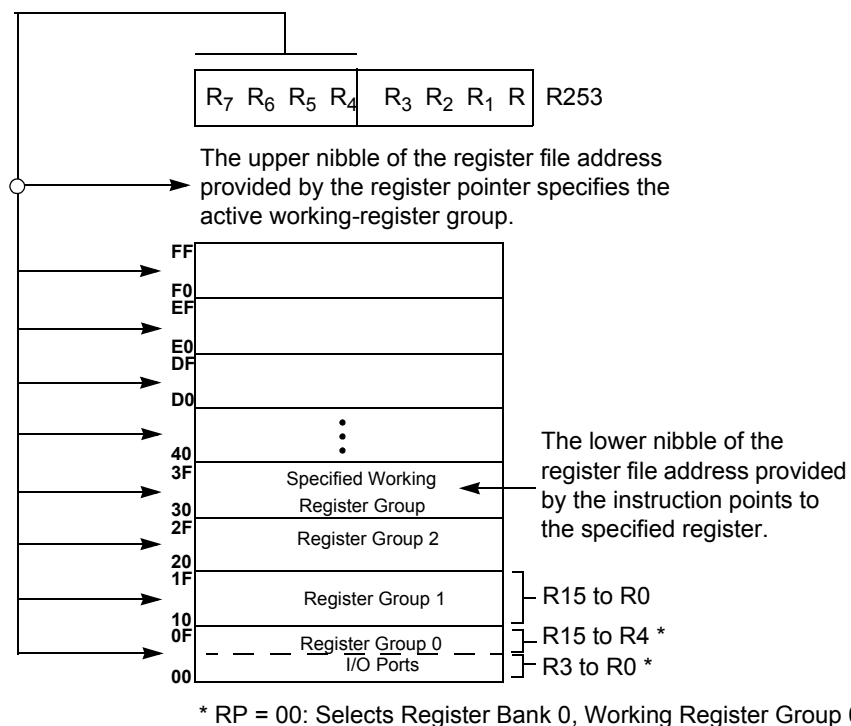


Figure 15. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

Timers

T8_Capture_HI—HI8(D)0Bh

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position	Description
T8_Capture_HI	[7:0]	R/W Captured Data—No Effect

T8_Capture_LO—L08(D)0Ah

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position	Description
T8_Capture_LO	[7:0]	R/W Captured Data—No Effect

T16_Capture_HI—HI16(D)09h

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position	Description
T16_Capture_HI	[7:0]	R/W Captured Data—No Effect

T16_Capture_LO—L016(D)08h

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position	Description
T16_Capture_LO	[7:0]	R/W Captured Data—No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07h

Field	Bit Position	Description
T16_Data_HI	[7:0]	R/W Data

Counter/Timer2 LS-Byte Hold Register—TC16L(D)06h

Field	Bit Position	Description
T16_Data_LO	[7:0]	R/W Data

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.



Caution: *Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers. The first clock of T8 might not have complete clock width and can occur any time when enabled.*



Note: *Ensure to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (DEMODULATION mode) when using the OR or AND commands. These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.*

T8 Clock

These bits define the frequency of the input signal to T8.

Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in DEMODULATION mode.

Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

T8 and T16 Common Functions—CTR1(0D)01h

This register controls the functions in common with the T8 and T16.

[Table 8](#) lists and briefly describes the fields for this register.

Table 8. CTR1(0D)01h T8 and T16 Common Functions

Field	Bit Position		Value	Description
Mode	7-----	R/W	0* 1	TRANSMIT Mode DEMODULATION Mode
P36_Out/ Demodulator_Input	-6-----	R/W	0* 1 0* 1	TRANSMIT Mode Port Output T8/T16 Output DEMODULATION Mode P31 P20
T8/T16_Logic/ Edge_Detect	--54----	R/W	00** 01 10 11 00** 01 10 11	TRANSMIT Mode AND OR NOR NAND DEMODULATION Mode Falling Edge Rising Edge Both Edges Reserved
Transmit_Submode/ Glitch_Filter	----32--	R/W	00* 01 10 11 00* 01 10 11	TRANSMIT Mode Normal Operation PING-PONG Mode T16_Out = 0 T16_Out = 1 DEMODULATION Mode No Filter 4 SCLK Cycle 8 SCLK Cycle Reserved
Initial_T8_Out/ Rising Edge	-----1-	R/W R W	0* 1 0* 1 0 1	TRANSMIT Mode T8_OUT is 0 Initially T8_OUT is 1 Initially DEMODULATION Mode No Rising Edge Rising Edge Detected No Effect Reset Flag to 0

Initial_T8_Out/Rising_Edge

In TRANSMIT mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

Initial_T16 Out/Falling_Edge

In TRANSMIT mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

► **Note:** *Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/T16_OUT.*

CTR2 Counter/Timer 16 Control Register—CTR2(D)02h

Table 9 lists and briefly describes the fields for this register.

Table 9. CTR2(D)02h: Counter/Timer16 Control Register

Field	Bit Position		Value	Description
T16_Enable	7-----	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0*	TRANSMIT Mode
			1	Modulo-N
			0	Single Pass
			1	DEMODULATION Mode
Time_Out	--5-----	R	0*	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
		W	0	No Counter Timeout
			1	Counter Timeout Occurred
			0	No Effect
			1	Reset Flag to 0

Table 9. CTR2(D)02h: Counter/Timer16 Control Register (Continued)

Field	Bit Position		Value	Description
T16_Clock	---43---	R/W	00** 01 10 11	SCLK SCLK/2 SCLK/4 SCLK/8
Capture_INT_Mask	-----2--	R/W	0** 1	Disable Data Capture Int. Enable Data Capture Int.
Counter_INT_Mask	-----1-	R/W	0 1	Disable Timeout Int. Enable Timeout Int.
P35_Out	-----0	R/W	0* 1	P35 as Port Output T16 Output on P35

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In TRANSMIT mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.

In DEMODULATION mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see [T16 DEMODULATION Mode](#) on page 41.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

Set this bit to allow an interrupt when T16 times out.

Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into SINGLE-PASS mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the PING-PONG mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7), see [Figure 26](#).

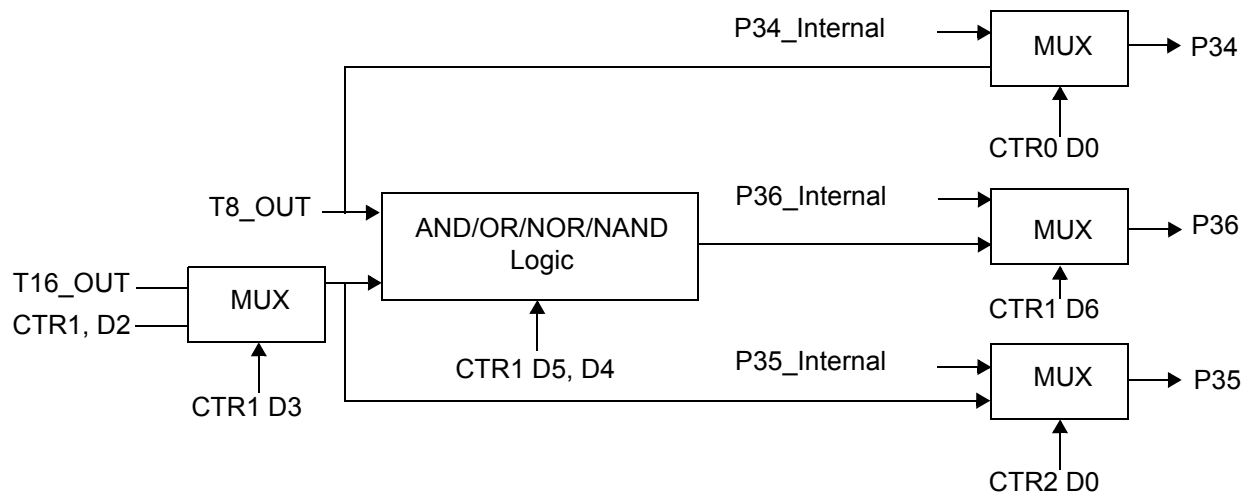


Figure 27. Output Circuit

The initial value of T8 or T16 must not be 1. If you stop the timer and restart the timer, reload the initial value to avoid an unknown previous value.

During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

Timer Output

The output logic for the timers is displayed in [Figure 27](#). P34 is used to output T8-OUT when D0 of CTR0 is set. P35 is used to output the value of T16-OUT when D0 of CTR2 is set. When D6 of CTR1 is set, P36 outputs the logic combination of T8-OUT and T16-OUT determined by D5 and D4 of CTR1.

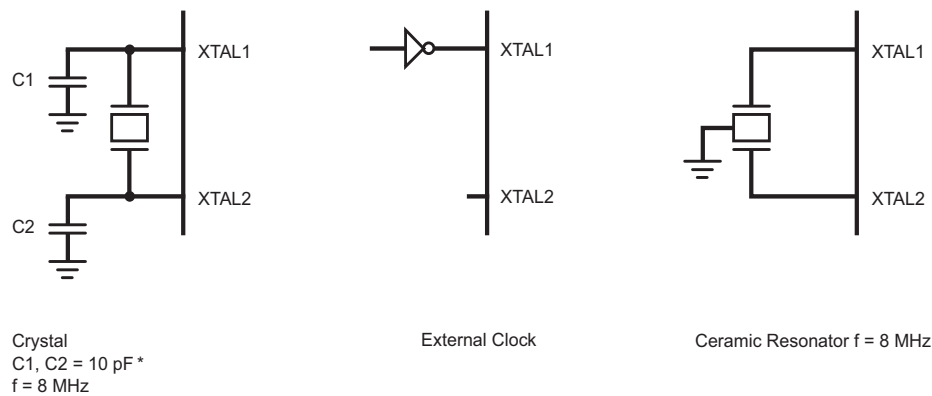
Interrupts

The Crimzon ZLP32300 features six different interrupts (see [Table 11](#) on page 45). The interrupts are maskable and prioritized (see [Figure 28](#)). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the

Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (R_S) less than or equal to $100\ \Omega$. The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors from each pin to ground. The typical capacitor value is 10 pF for 8 MHz. Also check with the crystal supplier for the optimum capacitance.



*Note: preliminary value.

Figure 29. Oscillator Configuration

Zilog's IR MCU supports crystal, resonator, and oscillator. Most resonators have a frequency tolerance of less than $\pm 0.5\%$, which is enough for remote control application. Resonator has a very fast startup time, which is around few hundred microseconds. Most crystals have a frequency tolerance of less than 50 ppm ($\pm 0.005\%$). However, crystal needs longer startup time than the resonator. The large loading capacitance slows down the oscillation startup time. Zilog® suggests not to use more than 10 pF loading capacitor for the crystal. If the stray capacitance of the PCB or the crystal is high, the loading capacitance C1 and C2 must be reduced further to ensure stable oscillation before the T_{POR} (Power-On Reset time is typically 5-6 ms, see [Table 20](#) on page 79).

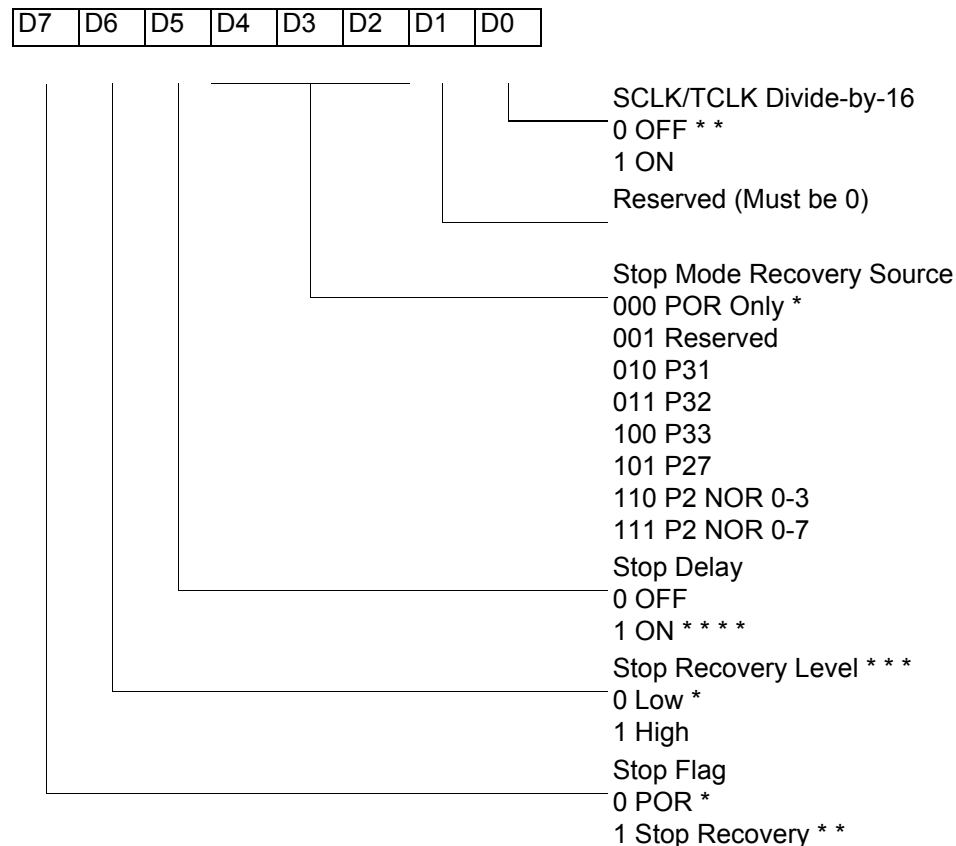
For Stop Mode Recovery operation, bit 5 of SMR register allows you to select the Stop Mode Recovery delay, which is the T_{POR} . If Stop Mode Recovery delay is not selected, the MCU executes instruction immediately after it wakes up from the STOP mode. If resonator or crystal is used as a clock source then Stop Mode Recovery delay needs to be selected (bit 5 of SMR = 1).

Stop Mode Recovery

Stop Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (see [Figure 31](#)). All bits are write only except bit 7, which is read only. Bit 7 is a Flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (see [Figure 33](#) on page 52) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0Bh.

SMR(0F)0Bh



*Default after Power-On Reset or Watchdog Reset

* *Default setting after Reset and Stop Mode Recovery.

* * *At the XOR gate input

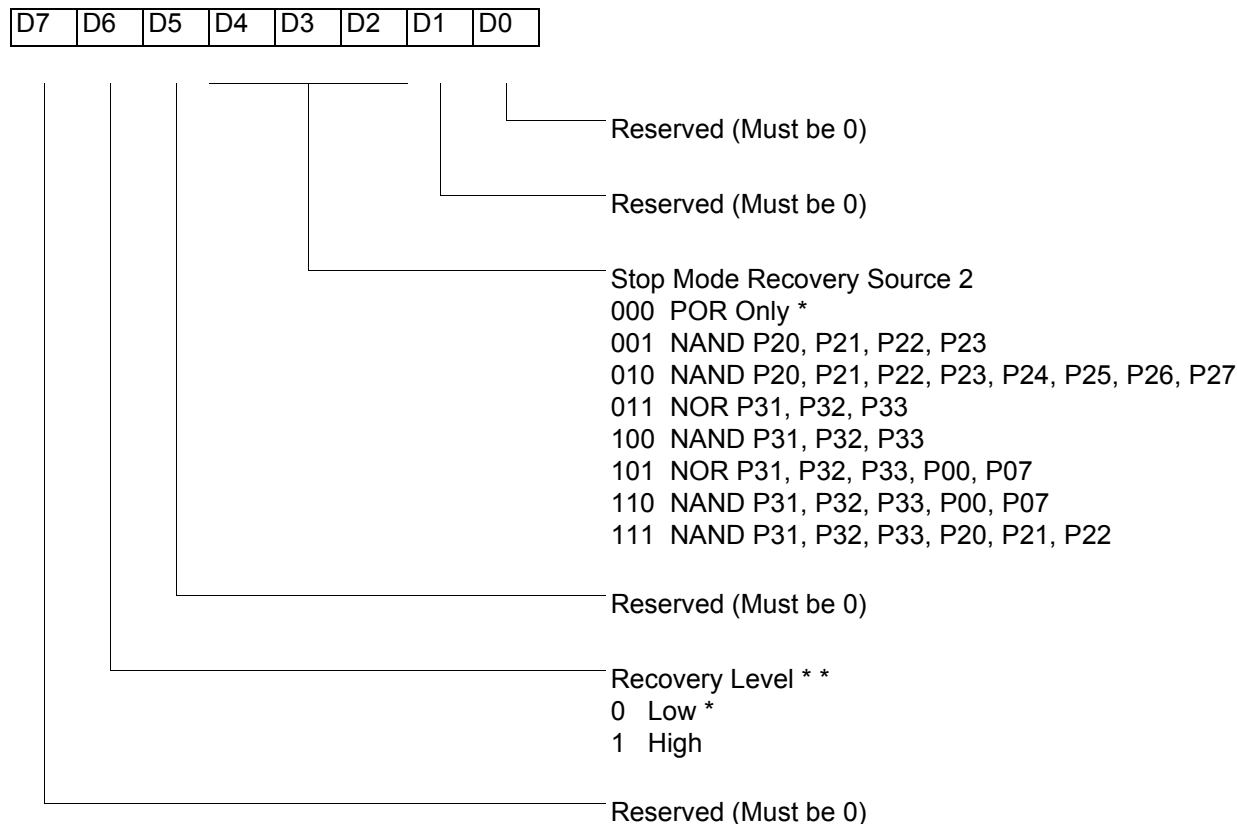
* * *Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 31. Stop Mode Recovery Register

Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (see [Figure 34](#)).

SMR2(0F)Dh



If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.

*Default setting after reset.

**At the XOR gate input.

Figure 34. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

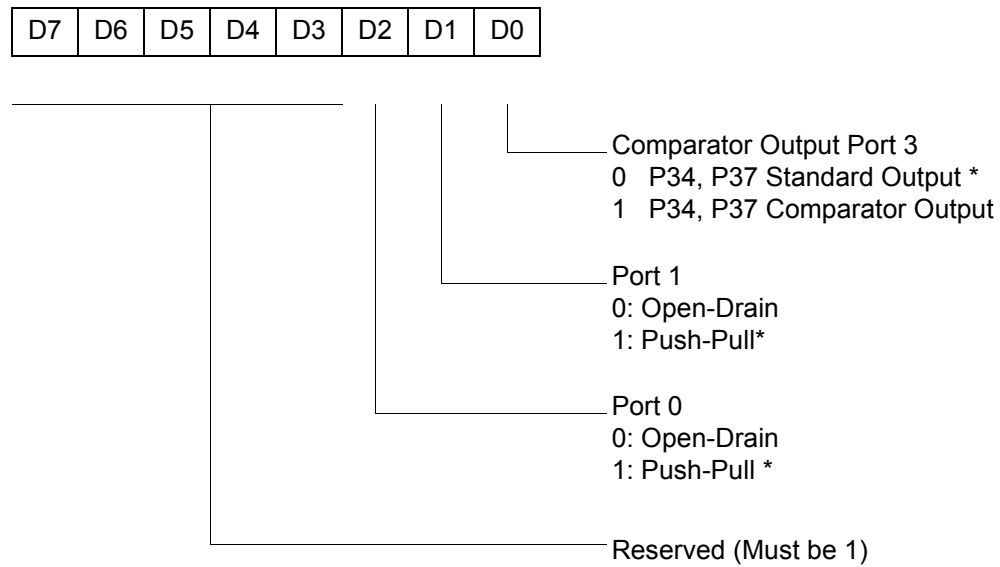
If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

► **Note:** Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are displayed in [Figure 42](#) through [Figure 55](#) on page 74.

PCON(0F)00H



*Default setting after reset

Figure 42. Port Configuration Register (PCON)(0F)00H: Write Only)

Standard Control Registers

The standard control registers are displayed in [Figure 46](#) through [Figure 55](#) on page 74.

R246 P2M(F6H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



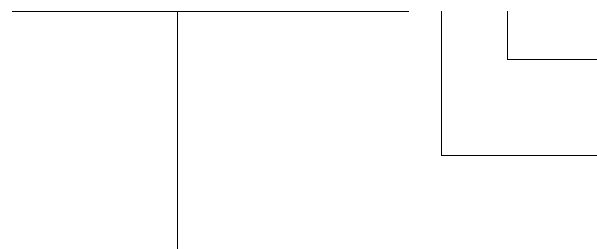
P27–P20 I/O Definition
0 Defines bit as OUTPUT
1 Defines bit as INPUT *

*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 46. Port 2 Mode Register (F6H: Write Only)

R247 P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



0: Port 2 Open Drain *
1: Port 2 Push-Pull
0= P31, P32 DIGITAL Mode*
1= P31, P32 ANALOG Mode

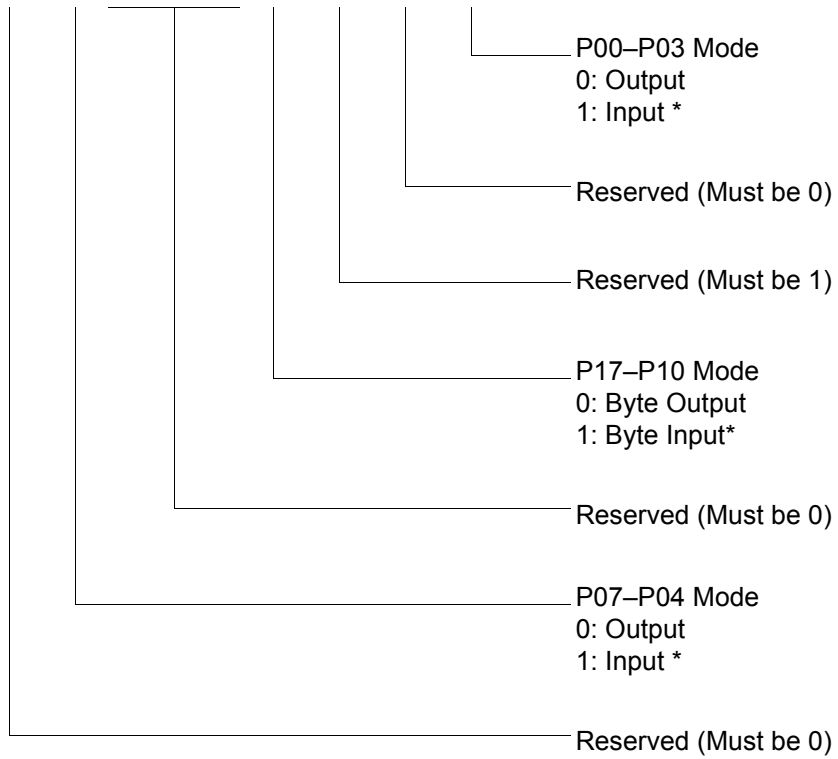
Reserved (Must be 0)

*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 47. Port 3 Mode Register (F7H: Write Only)

R248 P01M(F8H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



*Default setting after reset; only P00, P01 and P07 are available on Crimzon ZLP32300 20-pin configurations.

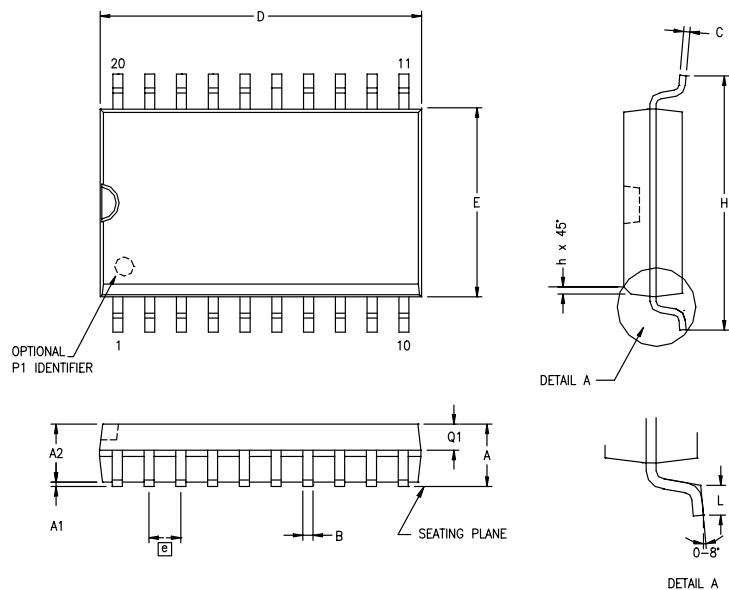
Figure 48. Port 0 and 1 Mode Register (F8H: Write Only)

Table 20. AC Characteristics

T _A =0 °C to +70 °C 8.0 MHz							Watchdog Timer Mode Register (D1, D0)
No	Symbol	Parameter	V _{CC}	Minimum	Maximum	Units	Notes
1	TpC	Input Clock Period	2.0–3.6	121	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1
3	TwC	Input Clock Width	2.0–3.6	37		ns	1
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1
5	TwTinH	Timer Input High Width	2.0–3.6	3TpC			1
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2
9	TwIH	Interrupt Request Input High Time	2.0–3.6	5TpC			1, 2
10	Twsm	Stop Mode Recovery Width Spec	2.0–3.6	12 10TpC		ns	3 4
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4
12	Twdt	Watchdog Timer Delay Time	2.0–3.6 2.0–3.6 2.0–3.6 2.0–3.6	5 10 20 80		ms ms ms ms	0, 0 0, 1 1, 0 1, 1
13	T _{POR}	Power-on reset	2.0–3.6	2.5	10	ms	

Notes

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR–D5 = 1.
4. SMR–D5 = 0.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	.496	.510
E	7.40	7.60	.291	.299
⌀	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

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Figure 59. 20-Pin SOIC Package Diagram

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