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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zlp32300h4808c00tr

Development Features

Table 2 lists the features of Crimzon ZLP32300 family.

Table 2. Crimzon ZLP32300 MCU Features

Device	OTP(KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Crimzon ZLP32300	8, 16, 32	237	32, 24 or 16	2.0–3.6 V
*General purpose				

The additional features include:

- Low power consumption–11 mW (typical)
- Three standby modes:
  - STOP—1.7 µA (typical)
  - HALT—0.6 mA (typical)
  - Low-voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
- Six priority interrupts
  - Three external
  - Two assigned to counter/timers
  - One Low-Voltage Detection interrupt
- Low-Voltage Detection and high voltage detection Flags
- Programmable Watchdog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
  - Port 0: 0–3 pull-up transistors
  - Port 0: 4–7 pull-up transistors
  - Port 1: 0–3 pull-up transistors
  - Port 1: 4–7 pull-up transistors

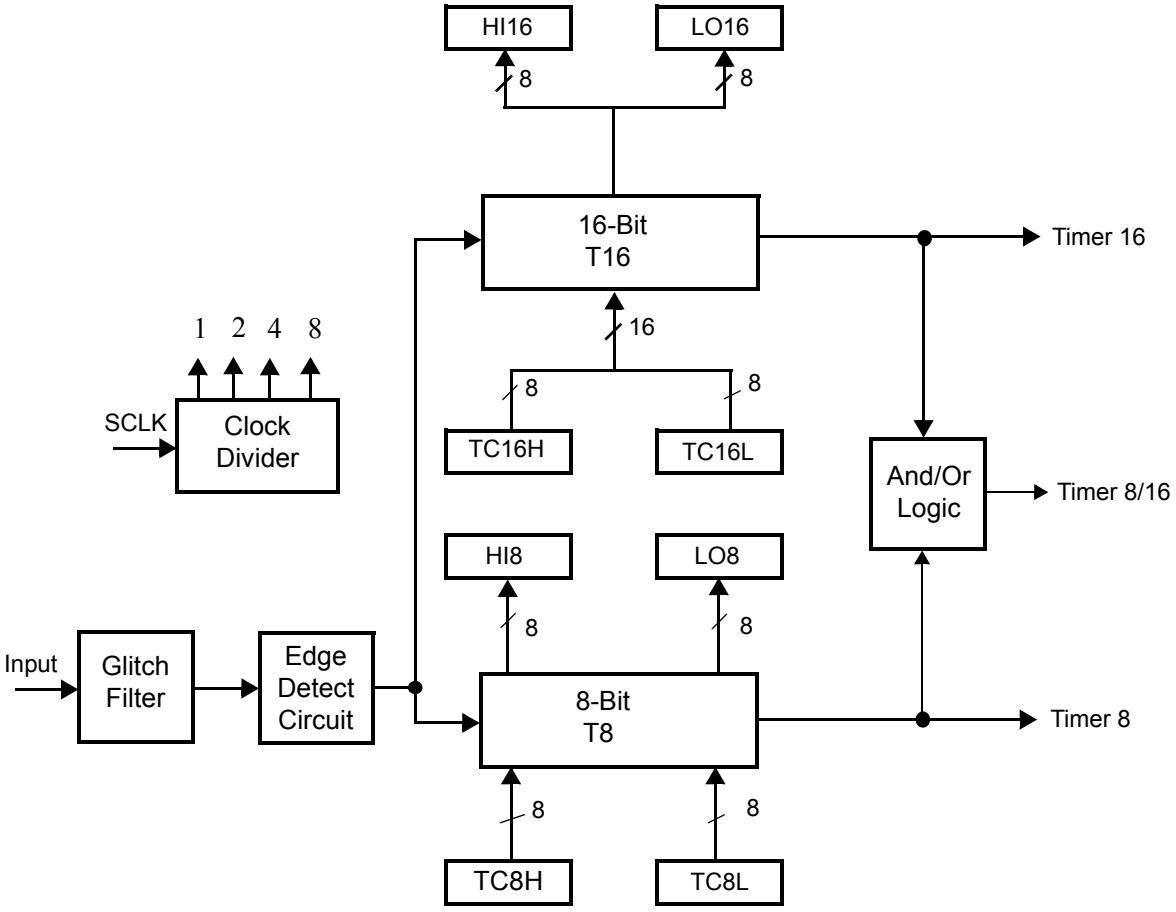


Figure 2. Counter/Timers Diagram

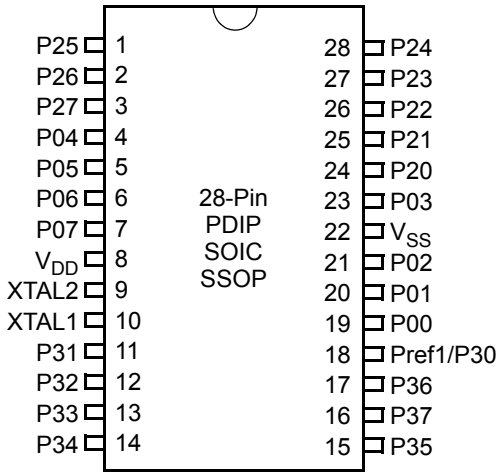


Figure 4. 28-Pin PDIP/SOIC/SSOP Pin Configuration

Table 4. 28-Pin PDIP/SOIC/SSOP Pin Identification

Pin No	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5, 6, 7
4-7	P04-P07	Input/Output	Port 0, Bits 4, 5, 6, 7
8	V_{DD}		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1, 2, 3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30 Port 3 Bit 0	Input	Analog ref input; connect to V_{CC} if not used Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0, 1, 2
22	V_{SS}		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0–4

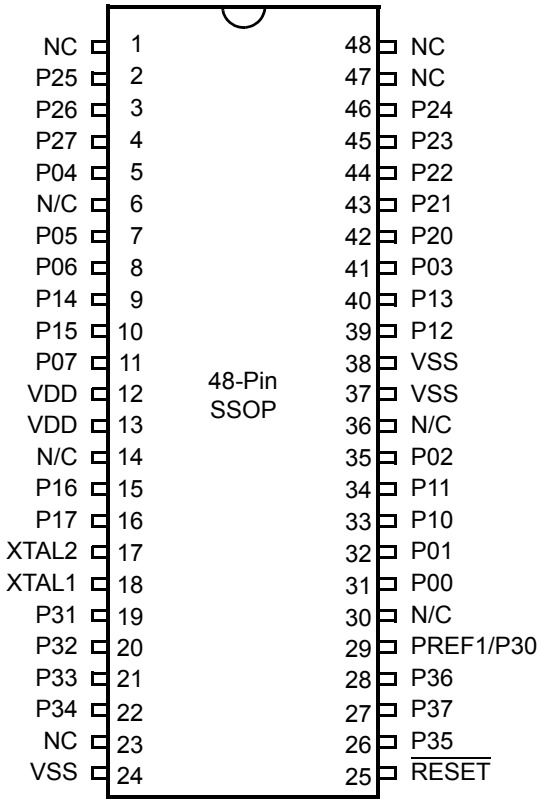


Figure 6. 48-Pin SSOP Pin Configuration

Table 5. 40- and 48-Pin Configuration

40-Pin PDIP No	48-Pin SSOP No	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11

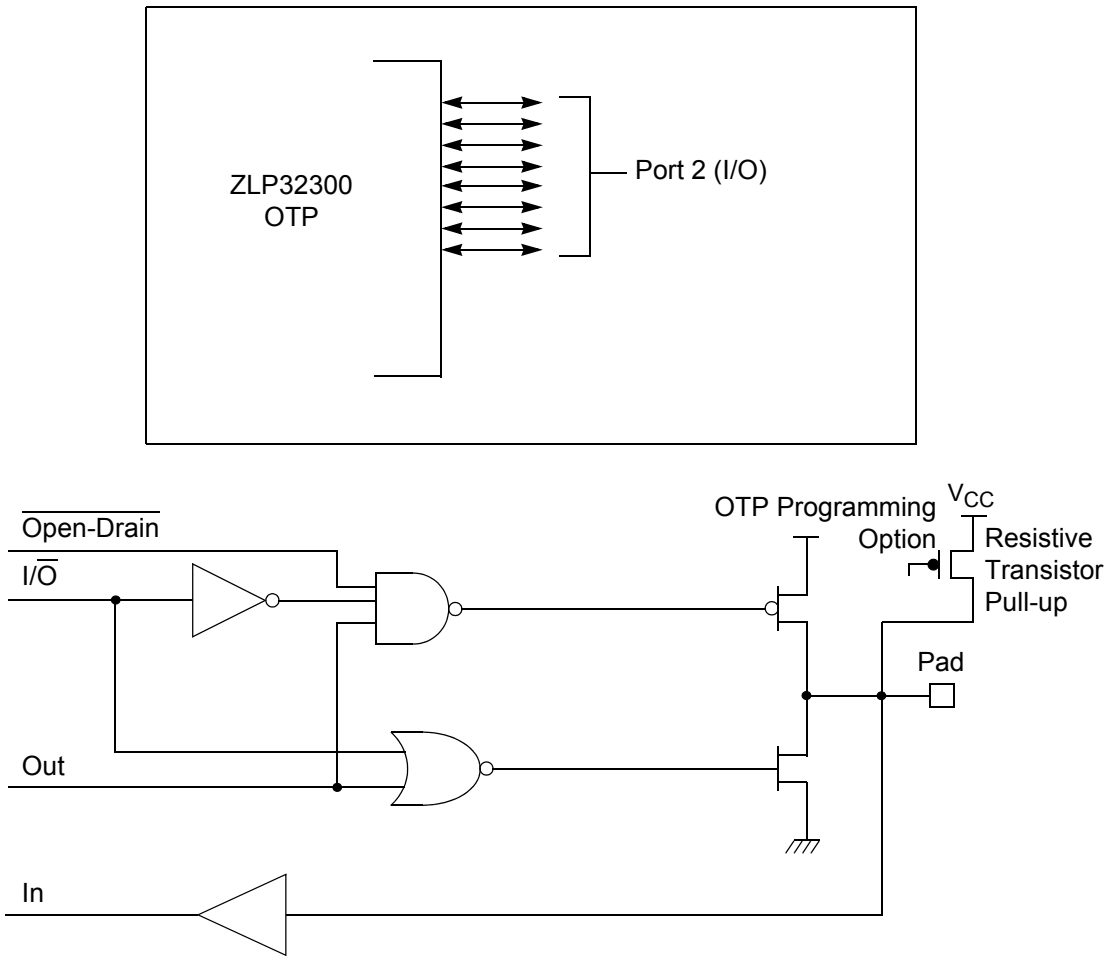


Figure 9. Port 2 Configuration

Port 3 (P37–P30)

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see Figure 10). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.

Functional Description

This device incorporates special functions to enhance the Z8 functionality in consumer and battery-operated applications.

Program Memory

This device addresses 32 KB of OTP memory. The first 12 bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts. See Figure 12.

RAM

This device features 256 B of RAM.

```
LD                      R1, 2                   ; CTR2→CTR1

LD                      RP, #0Dh                ; Select ERF D
for access to bank D
                                                ; (working
register group 0)
LD                      RP, #7Dh                ; Select
expanded register bank D and working            ; register
group 7 of bank 0 for access.
LD                      71h, 2
; CTRL2→register 71h
LD                      R1, 2
; CTRL2→register 71h
```

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 7 on page 27) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (see Figure 15). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note: *Working register group E0–EF can only be accessed through working registers and indirect addressing modes.*

Table 8. CTR1(0D)01h T8 and T16 Common Functions (Continued)

Field	Bit Position		Value	Description
Initial_T16_Out/ Falling_Edge	-------0			TRANSMIT Mode
		R/W	0*	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				DEMODULATION Mode
		R	0*	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

*Default at Power-On Reset
**Default at Power-On Reset. Not reset with a Stop Mode Recovery.

Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

P36_Out/Demodulator_Input

In TRANSMIT mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

T8/T16_Logic/Edge _Detect

In TRANSMIT mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter

In TRANSMIT mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to normal operation mode terminates the ‘PING-PONG Mode’ operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION mode, this field defines the width of the glitch that must be filtered out.

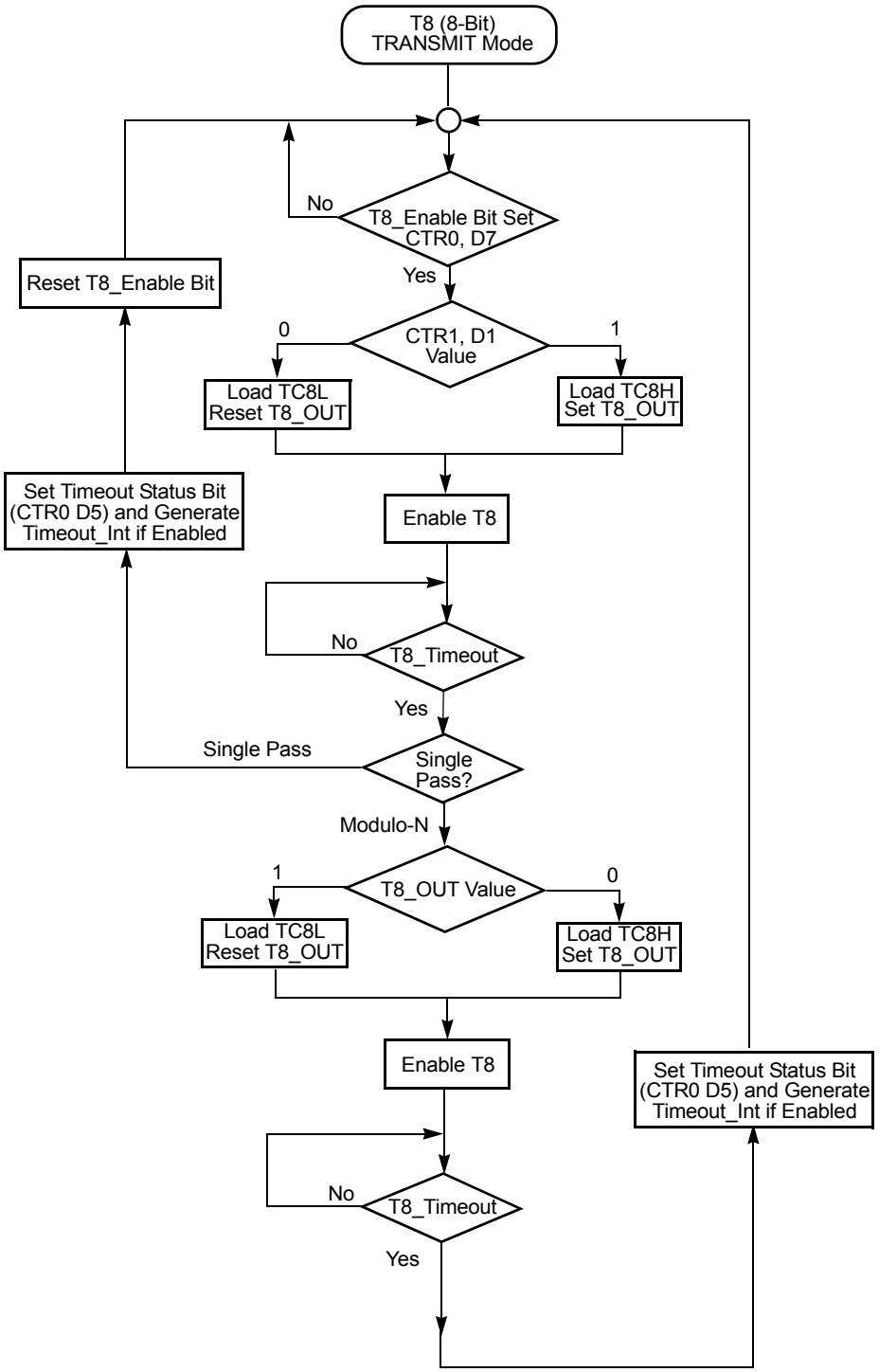
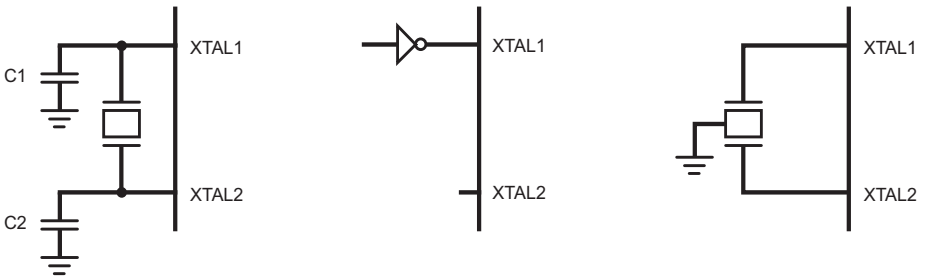


Figure 17. TRANSMIT Mode Flowchart

Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω. The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors from each pin to ground. The typical capacitor value is 10 pF for 8 MHz. Also check with the crystal supplier for the optimum capacitance.



Crystal
C1, C2 = 10 pF *
f = 8 MHz

External Clock

Ceramic Resonator f = 8 MHz

*Note: preliminary value.

Figure 29. Oscillator Configuration

Zilog's IR MCU supports crystal, resonator, and oscillator. Most resonators have a frequency tolerance of less than ±0.5%, which is enough for remote control application. Resonator has a very fast startup time, which is around few hundred microseconds. Most crystals have a frequency tolerance of less than 50 ppm (±0.005%). However, crystal needs longer startup time than the resonator. The large loading capacitance slows down the oscillation startup time. Zilog® suggests not to use more than 10 pF loading capacitor for the crystal. If the stray capacitance of the PCB or the crystal is high, the loading capacitance C1 and C2 must be reduced further to ensure stable oscillation before the T_{POR} (Power-On Reset time is typically 5-6 ms, see Table 20 on page 79).

For Stop Mode Recovery operation, bit 5 of SMR register allows you to select the Stop Mode Recovery delay, which is the T_{POR}. If Stop Mode Recovery delay is not selected, the MCU executes instruction immediately after it wakes up from the STOP mode. If resonator or crystal is used as a clock source then Stop Mode Recovery delay needs to be selected (bit 5 of SMR = 1).

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 15.

Table 15. Watchdog Timer Time Select

D1	D0	Timeout of Internal RC-Oscillator
0	0	5 ms min
0	1	10 ms min
1	0	20 ms min
1	1	80 ms min

WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1, see Figure 36.

Standard Control Registers

The standard control registers are displayed in Figure 46 through Figure 55 on page 74.

R246 P2M(F6H)

D7	D6	D5	D4	D3	D2	D1	D0

P27–P20 I/O Definition
0 Defines bit as OUTPUT
1 Defines bit as INPUT *

*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 46. Port 2 Mode Register (F6H: Write Only)

R247 P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0

0: Port 2 Open Drain *
1: Port 2 Push-Pull

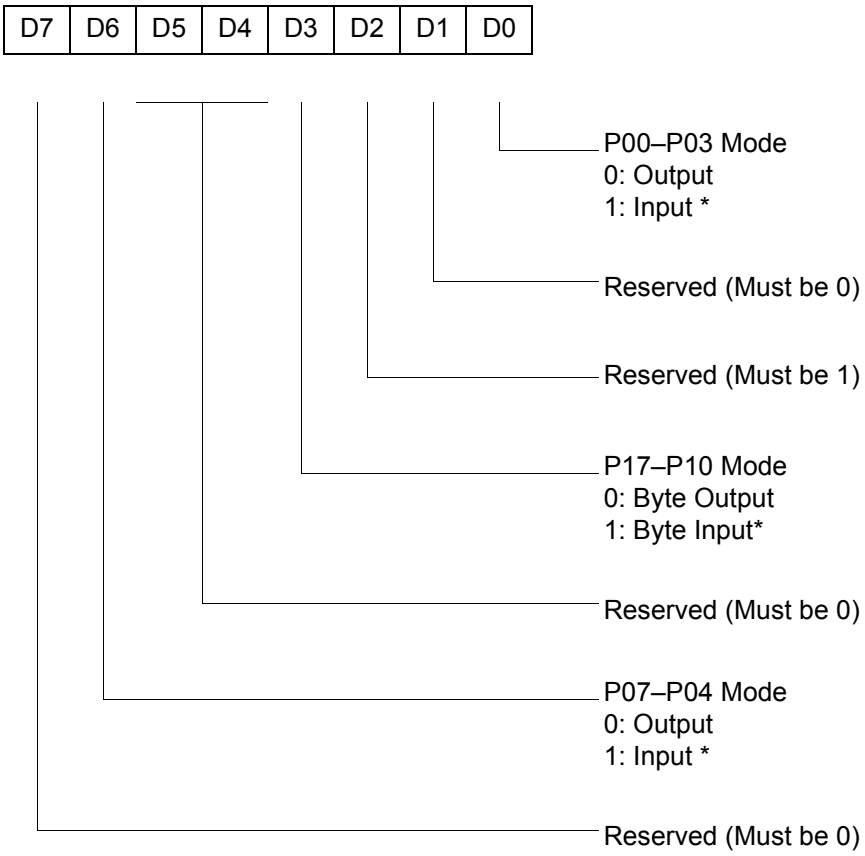
0= P31, P32 DIGITAL Mode*
1= P31, P32 ANALOG Mode

Reserved (Must be 0)

*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 47. Port 3 Mode Register (F7H: Write Only)

R248 P01M(F8H)



*Default setting after reset; only P00, P01 and P07 are available on Crimzon ZLP32300 20-pin configurations.

Figure 48. Port 0 and 1 Mode Register (F8H: Write Only)

Table 19. DC Characteristics (Continued)

			T_A= 0 °C to +70 °C					
Symbol	**Parameter**	**V_{CC}**	**Min**	**Typ(7)**	**Max**	**Units**	**Conditions**	**Notes**
I_{IL}	Input Leakage	2.0-3.6	–1		1	µA	V_{IN} = 0 V, V_{CC} Pull-ups disabled	
R_{PU}	Pull-Up Resistance	2.0 3.6	225 75		675 275	kΩ kΩ	V_{IN} = 0 V, Pull-ups selected by mask option	
I_{OL}	Output Leakage	2.0-3.6	–1		1	µA	V_{IN} = 0 V, V_{CC}	
I_{CC}	Supply Current	2.0 3.6		1 5	3 10	mA mA	at 8.0 MHz at 8.0 MHz	1, 2 1, 2
I_{CC1}	Standby Current (HALT Mode)	2.0 3.6		0.5 0.8	1.6 2.0	mA	V_{IN} = 0V, V_{CC} at 8.0 MHz Same as above	1, 2, 6 1, 2, 6
I_{CC2}	Standby Current (STOP Mode)	2.0 3.6 2.0 3.6		1.6 1.8 5 8	8 10 20 30	µA µA µA µA	V_{IN} = 0 V, V_{CC} WDT is not Running Same as above V_{IN} = 0 V, V_{CC} WDT is Running Same as above	3 3 3 3
I_{LV}	Standby Current (Low Voltage)			1.2	6	µA	Measured at 1.3 V	4
V_{BO}	V_{CC} Low Voltage Protection			1.9	2.0	V	8 MHz maximum Ext. CLK Freq.	
V_{LVD}	Vcc Low Voltage Detection			2.4		V		
V_{HVD}	Vcc High Voltage Detection			2.7		V		

Notes
1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 µF), physically close to VDD and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 ºC.

AC Characteristics

Figure 57 and Table 20 describe the Alternating Current (AC) characteristics.

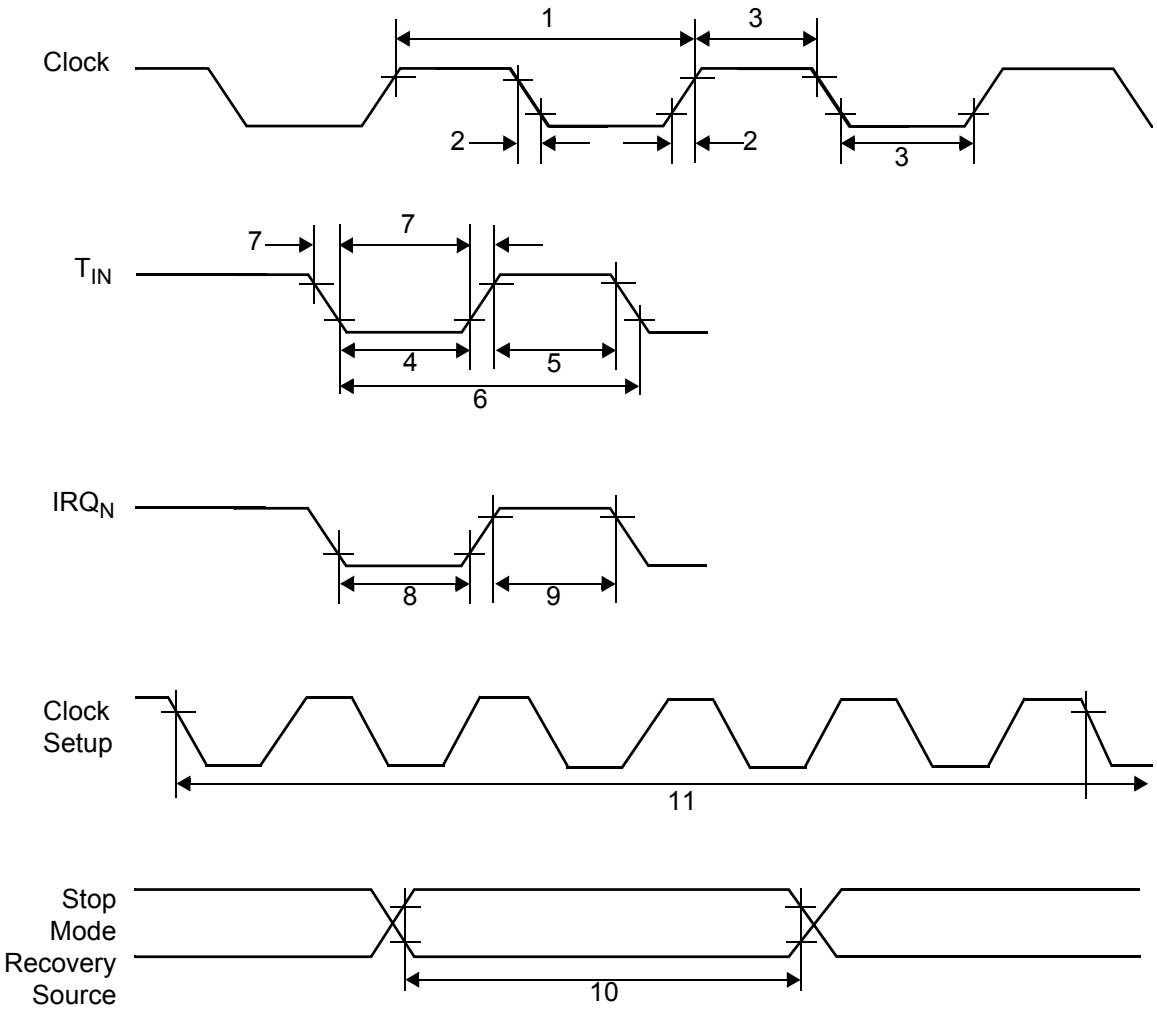


Figure 57. AC Timing Diagram

Device	Part Number	Description
	ZLP32300P2008G	20-pin PDIP 8 K OTP
	ZLP32300S2008G	20-pin SOIC 8 K OTP
	ZLP32300H4804G	48-pin SSOP 4 K OTP
	ZLP32300P4004G	40-pin PDIP 4 K OTP
	ZLP32300H2804G	28-pin SSOP 4 K OTP
	ZLP32300P2804G	28-pin PDIP 4 K OTP
	ZLP32300S2804G	28-pin SOIC 4 K OTP
	ZLP32300H2004G	20-pin SSOP 4 K OTP
	ZLP32300P2004G	20-pin PDIP 4 K OTP
	ZLP32300S2004G	20-pin SOIC 4 K OTP
	ZLP323ICE01ZAC*	40-PDIP/48-SSOP Accessory Kit
	Note: *ZLP323ICE01ZAC has been replaced by an improved version, ZCRMZNICE02ZACG.	
	ZLP128ICE01ZEMG	In-Circuit Emulator
	Note: *ZLP128ICE01ZEMG has been replaced by an improved version, ZCRMZNICE01ZEMG.	
	ZCRMZNICE01ZEMG	Crimzon In-Circuit Emulator
	ZCRMZN00100KITG	Crimzon In-Circuit Emulator Development Kit
	ZCRMZNICE01ZACG	20-Pin Accessory Kit
	ZCRMZNICE02ZACG	40/48-Pin Accessory Kit

Notes
1. Replace C with G for Lead-Free Packaging.
2. Contact www.zilog.com for the die form.

For fast results, contact your local Zilog® sales office for assistance in ordering the part(s) desired.

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