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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, HLVD, POR, WDT |
| Number of I/O | 32 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-BSSOP (0.295", 7.50mm Width) |
| Supplier Device Package | 48-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/zlp32300h4808g |

**Table 5. 40- and 48-Pin Configuration (Continued)**

| 40-Pin PDIP No | 48-Pin SSOP No | Symbol |
|---|---|---|
| 32 | 39 | P12 |
| 33 | 40 | P13 |
| 8 | 9 | P14 |
| 9 | 10 | P15 |
| 12 | 15 | P16 |
| 13 | 16 | P17 |
| 35 | 42 | P20 |
| 36 | 43 | P21 |
| 37 | 44 | P22 |
| 38 | 45 | P23 |
| 39 | 46 | P24 |
| 2 | 2 | P25 |
| 3 | 3 | P26 |
| 4 | 4 | P27 |
| 16 | 19 | P31 |
| 17 | 20 | P32 |
| 18 | 21 | P33 |
| 19 | 22 | P34 |
| 22 | 26 | P35 |
| 24 | 28 | P36 |
| 23 | 27 | P37 |
| 20 | 23 | NC |
| 40 | 47 | NC |
| 1 | 1 | NC |
| 21 | 25 | $\overline{\text{RESET}}$ |
| 15 | 18 | XTAL1 |
| 14 | 17 | XTAL2 |
| 11 | 12, 13 | $V_{DD}$ |
| 31 | 24, 37, 38 | $V_{SS}$ |
| 25 | 29 | Pref1/P30 |
|  | 48 | NC |
|  | 6 | NC |

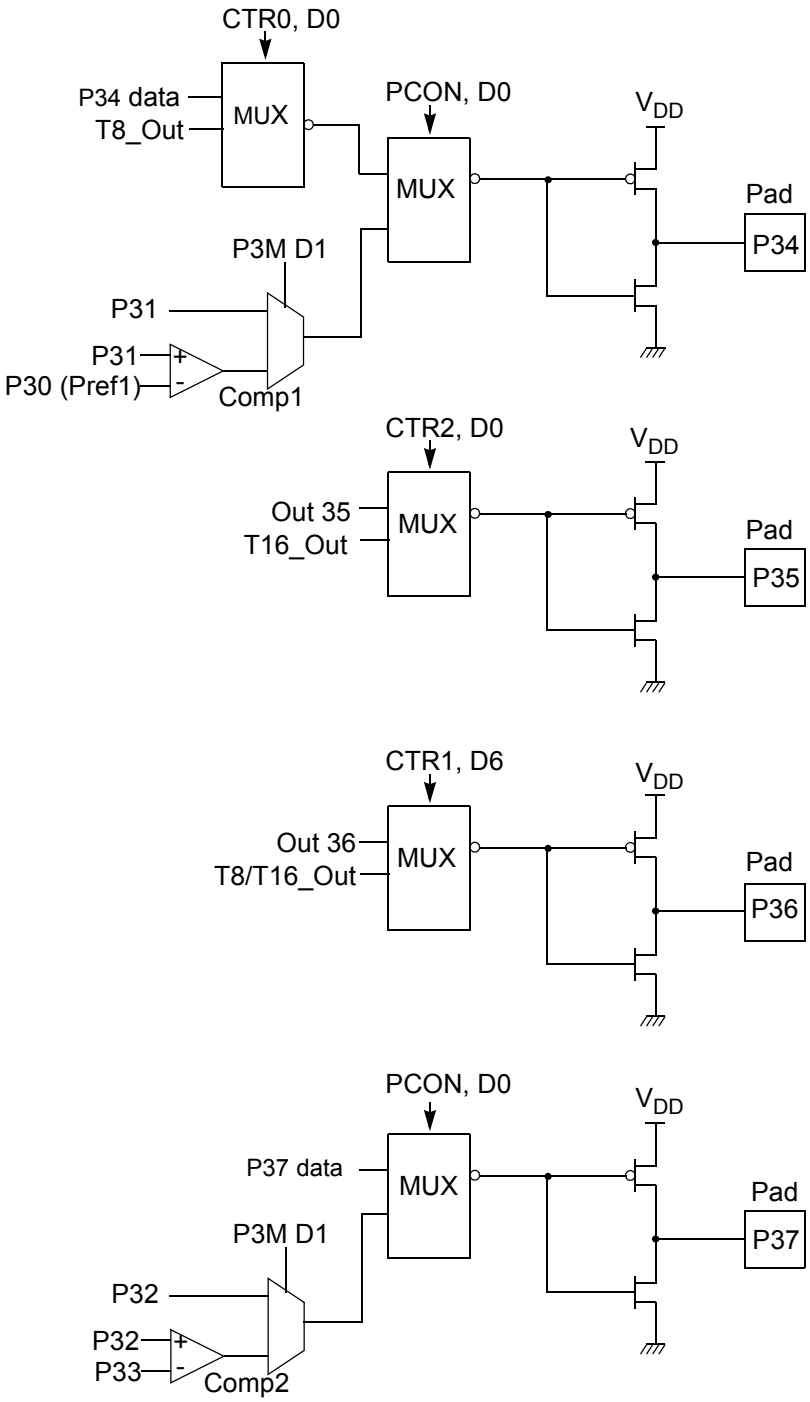



**Figure 11. Port 3 Counter/Timer Output Configuration**

### Comparator Inputs

In ANALOG mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as displayed in Figure 10 on page 15. In DIGITAL mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

**Note:** *Comparators are powered down by entering STOP mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into DIGITAL mode.*

### Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

## $\overline{\text{RESET}}$ (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watchdog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watchdog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the ZLP32300 asserts (Low) the $\overline{\text{RESET}}$ pin, the internal pull-up is disabled. The ZLP32300 does not assert the $\overline{\text{RESET}}$ pin when under VBO.

**Note:** *The external Reset does not initiate an exit from STOP mode.*

register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

**Note:** *An expanded register bank is also referred to as an expanded register group (see* Figure 13*).*

### Counter/Timer8 High Hold Register—TC8H(D)05h

| Field | Bit Position | | Description |
|---|---|---|---|
| T8_Level_HI | [7:0] | R/W | Data |

### Counter/Timer8 Low Hold Register—TC8L(D)04h

| Field | Bit Position | | Description |
|---|---|---|---|
| T8_Level_LO | [7:0] | R/W | Data |

### CTR0 Counter/Timer8 Control Register—CTR0(D)00h

Table 7 lists and briefly describes the fields for this register.

**Table 7. CTR0(D)00h Counter/Timer8 Control Register**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| T8_Enable | 7------- | R/W | 0*<br>1<br>0<br>1 | Counter Disabled<br>Counter Enabled<br>Stop Counter<br>Enable Counter |
| Single/Modulo-N | -6------- | R/W | 0*<br>1 | Modulo-N<br>Single Pass |
| Time_Out | --5------ | R/W | 0**<br>1<br>0<br>1 | No Counter Time-Out<br>Counter Time-Out Occurred<br>No Effect<br>Reset Flag to 0 |
| T8 _Clock | ---43--- | R/W | 0 0**<br>0 1<br>1 0<br>1 1 | SCLK<br>SCLK/2<br>SCLK/4<br>SCLK/8 |
| Capture_INT_Mask | -----2-- | R/W | 0**<br>1 | Disable Data Capture Interrupt<br>Enable Data Capture Interrupt |
| Counter_INT_Mask | ------1- | R/W | 0**<br>1 | Disable Time-Out Interrupt<br>Enable Time-Out Interrupt |
| P34_Out | -------0 | R/W | 0*<br>1 | P34 as Port Output<br>T8 Output on P34 |

*Indicates the value upon Power-On Reset.
**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.

**Table 8. CTR1(0D)01h T8 and T16 Common Functions (Continued)**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| Initial_T16_Out/ Falling_Edge | -------0 | | | TRANSMIT Mode |
| | | R/W | 0* | T16_OUT is 0 Initially |
| | | | 1 | T16_OUT is 1 Initially |
| | | | | DEMODULATION Mode |
| | | R | 0* | No Falling Edge |
| | | | 1 | Falling Edge Detected |
| | | W | 0 | No Effect |
| | | | 1 | Reset Flag to 0 |

*Default at Power-On Reset
**Default at Power-On Reset. Not reset with a Stop Mode Recovery.

### Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

### P36_Out/Demodulator_Input

In TRANSMIT mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

### T8/T16_Logic/Edge _Detect

In TRANSMIT mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION mode, this field defines which edge should be detected by the edge detector.

### Transmit_Submode/Glitch Filter

In TRANSMIT mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to normal operation mode terminates the ‘PING-PONG Mode’ operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION mode, this field defines the width of the glitch that must be filtered out.

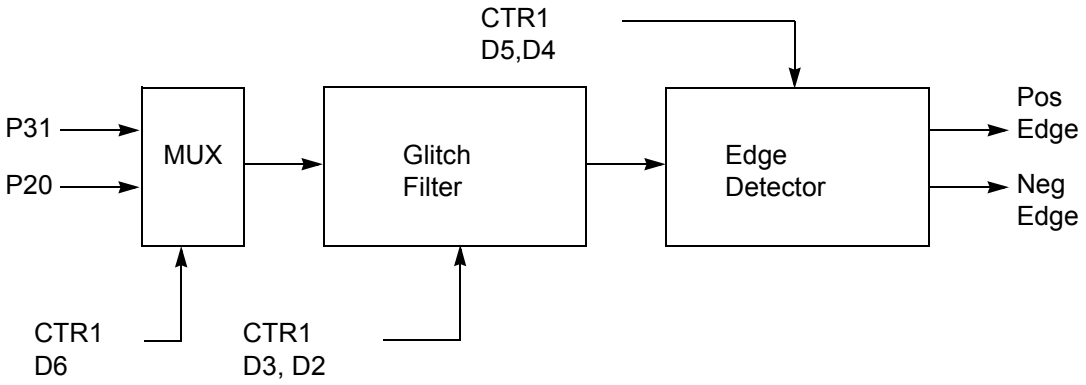



**Figure 16. Glitch Filter Circuitry**

### T8 TRANSMIT Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 17.

**Table 11. Interrupt Types, Sources, and Vectors**

| Name | Source | Vector Location | Comments |
|---|---|---|---|
| IRQ0 | P32 | 0,1 | External (P32), Rising, Falling Edge Triggered |
| IRQ1 | P33 | 2,3 | External (P33), Falling Edge Triggered |
| IRQ2 | P31, $T_{IN}$ | 4,5 | External (P31), Rising, Falling Edge Triggered |
| IRQ3 | T16 | 6,7 | Internal |
| IRQ4 | T8 | 8,9 | Internal |
| IRQ5 | LVD | 10,11 | Internal |

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All Crimzon ZLP32300 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 12.

**Table 12. IRQ Register**

| IRQ | | Interrupt Edge | |
|---|---|---|---|
| **D7** | **D6** | **IRQ2 (P31)** | **IRQ0 (P32)** |
| 0 | 0 | F | F |
| 0 | 1 | F | R |
| 1 | 0 | R | F |
| 1 | 1 | R/F | R/F |

**Note:** F = Falling Edge; R = Rising Edge

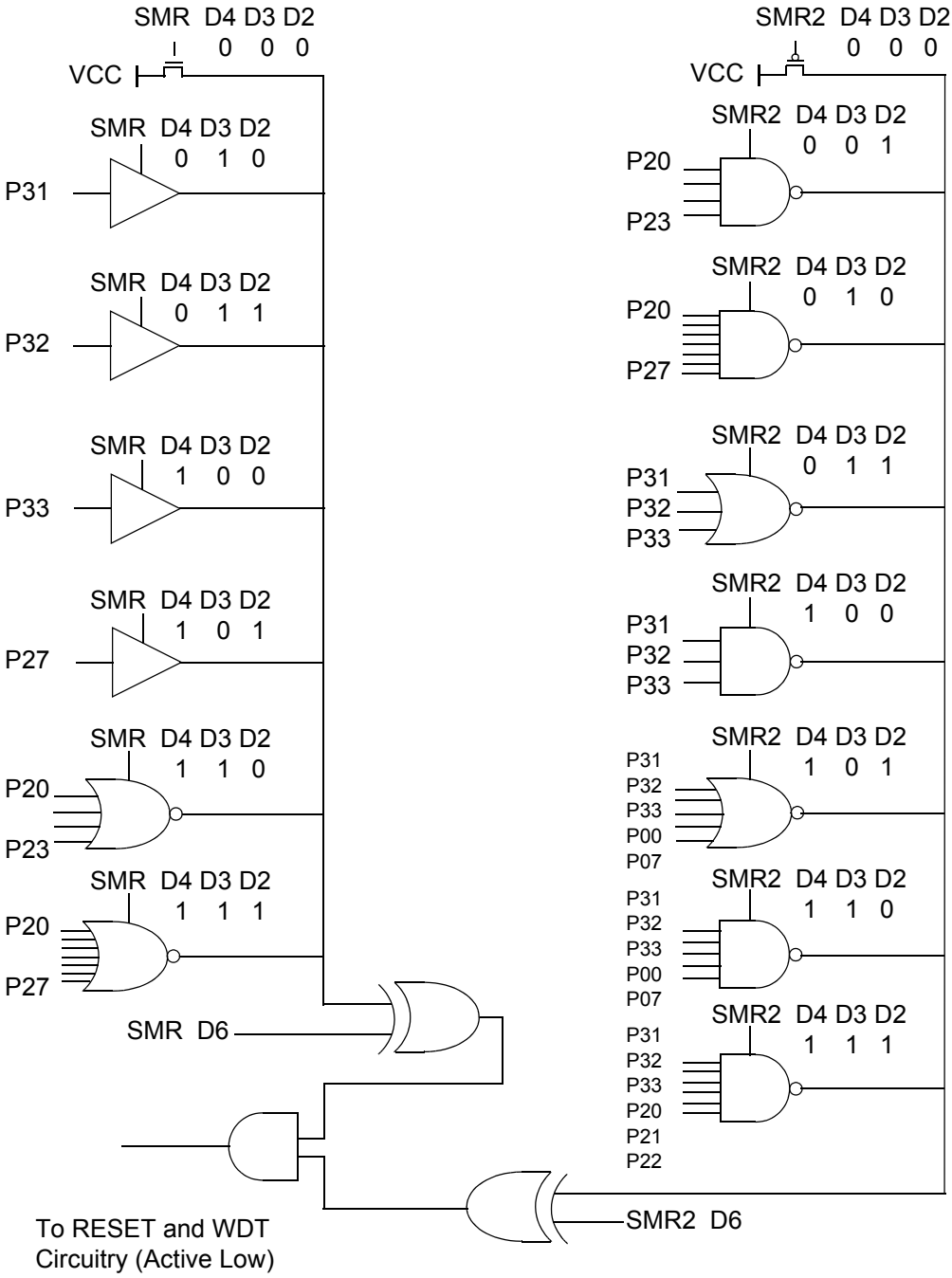
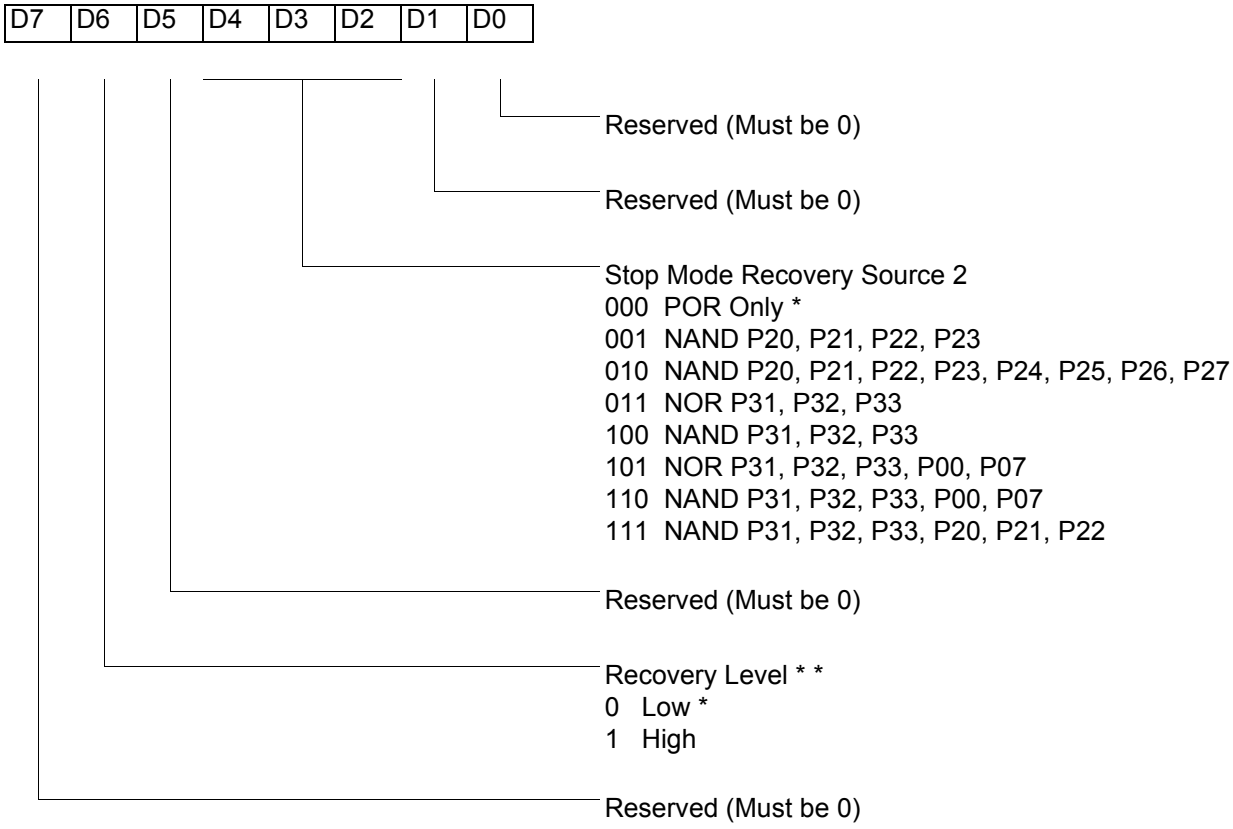



**Figure 33. Stop Mode Recovery Source**

### Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (see Figure 34).

SMR2(0F)Dh



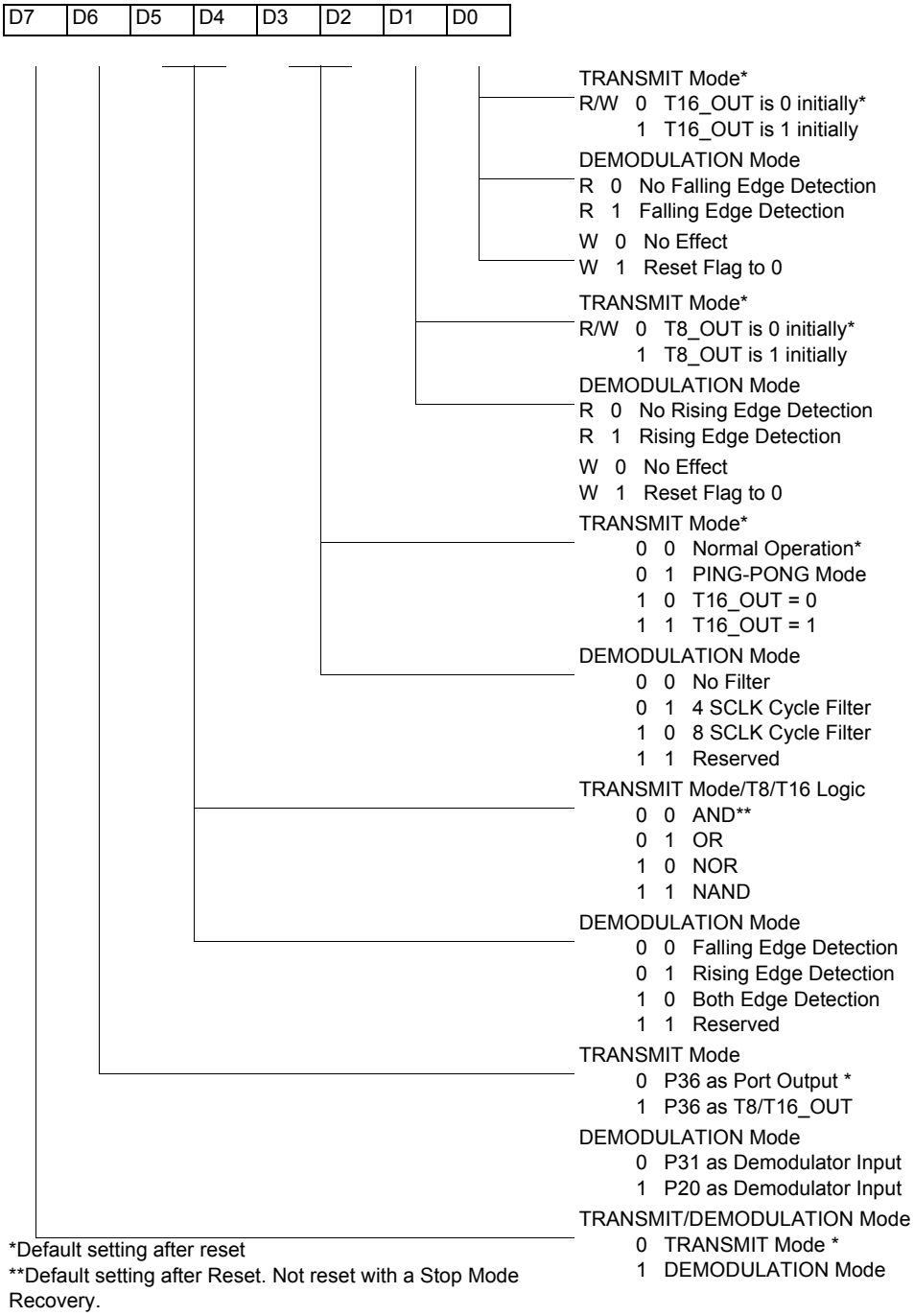

If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.
*Default setting after reset.
* *At the XOR gate input.

**Figure 34. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)**

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

**Note:** *Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.*

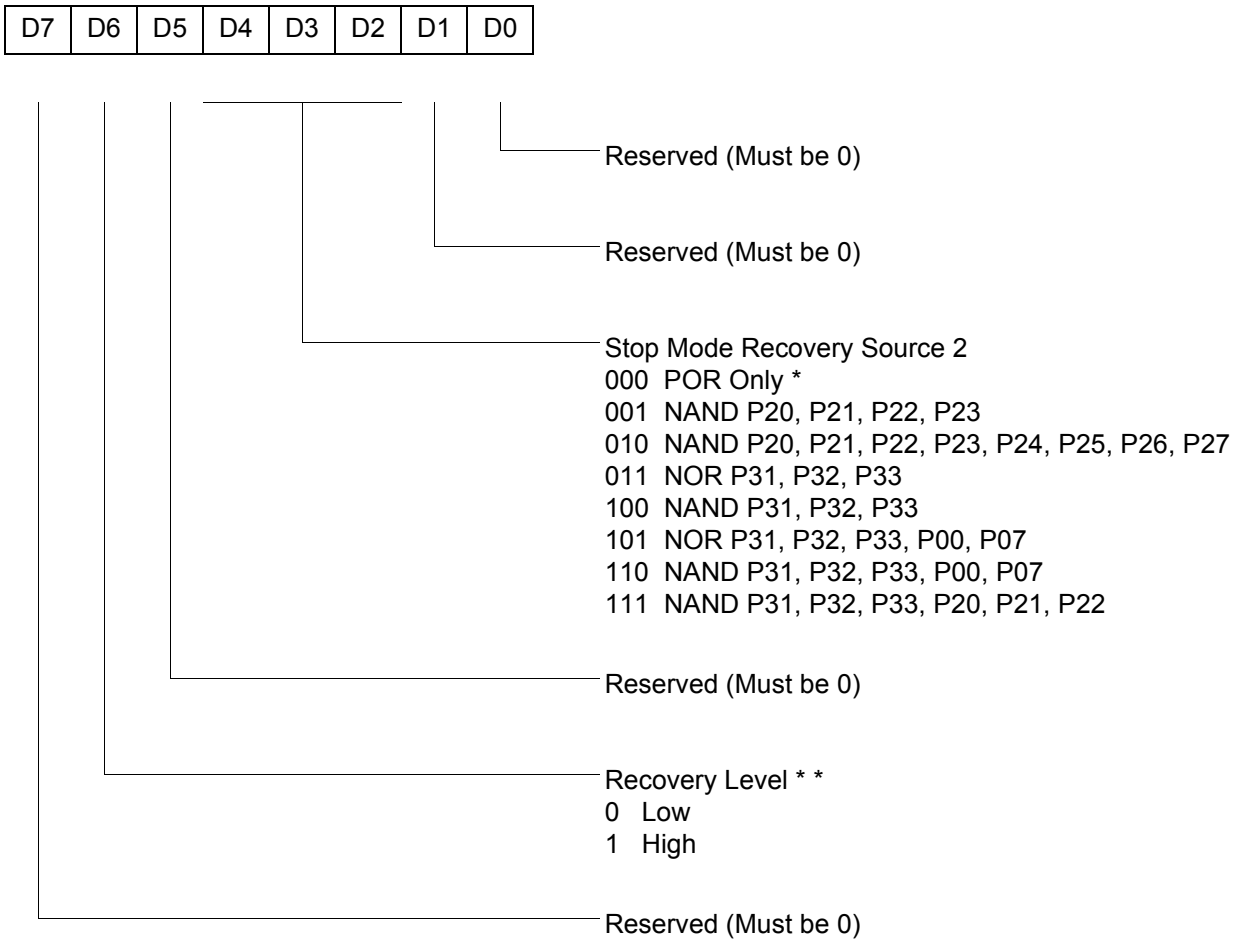
CTR1(0D)01H




*Default setting after reset
**Default setting after Reset. Not reset with a Stop Mode Recovery.

**Figure 38. T8 and T16 Common Control Functions ((0D)01H: Read/Write)**

SMR2(0F)0DH




If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.
*Default setting after reset. Not Reset with a Stop Mode Recovery.
* *At the XOR gate input

**Figure 44. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)**

## Standard Control Registers

The standard control registers are displayed in Figure 46 through Figure 55 on page 74.

R246 P2M(F6H)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

P27–P20 I/O Definition
0 Defines bit as OUTPUT
1 Defines bit as INPUT *

*Default setting after reset. Not Reset with a Stop Mode Recovery.

**Figure 46. Port 2 Mode Register (F6H: Write Only)**

R247 P3M(F7H)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

0: Port 2 Open Drain *
1: Port 2 Push-Pull

0= P31, P32 DIGITAL Mode*
1= P31, P32 ANALOG Mode

Reserved (Must be 0)

*Default setting after reset. Not Reset with a Stop Mode Recovery.

**Figure 47. Port 3 Mode Register (F7H: Write Only)**

R254 SPH(FEH)

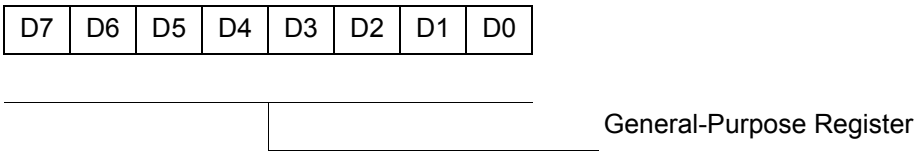



**Figure 54. Stack Pointer High (FEH: Read/Write)**

R255 SPL(FFH)

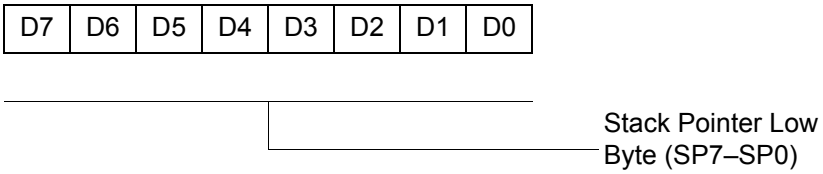



**Figure 55. Stack Pointer Low (FFH: Read/Write)**

# Electrical Characteristics

## Absolute Maximum Ratings

Stresses greater than those listed in Table 18 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

**Table 17. Absolute Maximum Ratings**

| Parameter | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|
| Ambient temperature under bias | 0 | +70 | C | |
| Storage temperature | –65 | +150 | C | |
| Voltage on any pin with respect to $V_{SS}$ | –0.3 | +5.5 | V | 1 |
| Voltage on $V_{DD}$ pin with respect to $V_{SS}$ | –0.3 | +3.6 | V | |
| Maximum current on input and/or inactive output pin | –5 | +5 | µA | |
| Maximum output current from active output pin | –25 | +25 | mA | |
| Maximum current into $V_{DD}$ or out of $V_{SS}$ | | 75 | mA | |

[1]This voltage applies to all pins except the following: $V_{DD}$, P32, P33 and $\overline{\text{RESET}}$.

## Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 56).

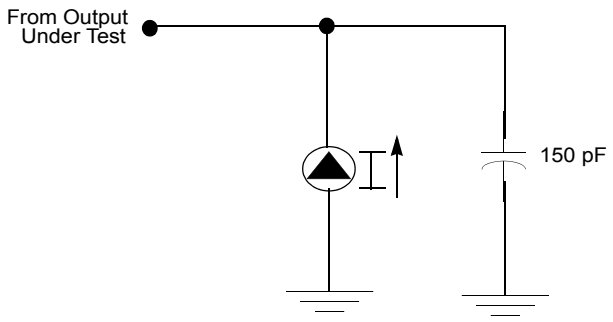



**Figure 56. Test Load Diagram**

**Table 19. DC Characteristics (Continued)**

| | | | $T_A$= 0 °C to +70 °C | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **$V_{CC}$** | **Min** | **Typ(7)** | **Max** | **Units** | **Conditions** | **Notes** |
| $I_{IL}$ | Input Leakage | 2.0-3.6 | –1 | | 1 | µA | $V_{IN}$ = 0 V, $V_{CC}$ Pull-ups disabled | |
| $R_{PU}$ | Pull-Up Resistance | 2.0<br>3.6 | 225<br>75 | | 675<br>275 | kΩ<br>kΩ | $V_{IN}$ = 0 V, Pull-ups selected by mask option | |
| $I_{OL}$ | Output Leakage | 2.0-3.6 | –1 | | 1 | µA | $V_{IN}$ = 0 V, $V_{CC}$ | |
| $I_{CC}$ | Supply Current | 2.0<br>3.6 | | 1<br>5 | 3<br>10 | mA<br>mA | at 8.0 MHz<br>at 8.0 MHz | 1, 2<br>1, 2 |
| $I_{CC1}$ | Standby Current (HALT Mode) | 2.0<br>3.6 | | 0.5<br>0.8 | 1.6<br>2.0 | mA | $V_{IN}$ = 0V, $V_{CC}$ at 8.0 MHz<br>Same as above | 1, 2, 6<br>1, 2, 6 |
| $I_{CC2}$ | Standby Current (STOP Mode) | 2.0<br>3.6<br>2.0<br>3.6 | | 1.6<br>1.8<br>5<br>8 | 8<br>10<br>20<br>30 | µA<br>µA<br>µA<br>µA | $V_{IN}$ = 0 V, $V_{CC}$ WDT is not Running<br>Same as above<br>$V_{IN}$ = 0 V, $V_{CC}$ WDT is Running<br>Same as above | 3<br>3<br>3<br>3 |
| $I_{LV}$ | Standby Current (Low Voltage) | | | 1.2 | 6 | µA | Measured at 1.3 V | 4 |
| $V_{BO}$ | $V_{CC}$ Low Voltage Protection | | | 1.9 | 2.0 | V | 8 MHz maximum Ext. CLK Freq. | |
| $V_{LVD}$ | Vcc Low Voltage Detection | | | 2.4 | | V | | |
| $V_{HVD}$ | Vcc High Voltage Detection | | | 2.7 | | V | | |

**Notes**
1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when $V_{CC}$ falls below $V_{BO}$ limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 µF), physically close to VDD and $V_{SS}$ pins if operating voltage fluctuations are anticipated, such as those resulting from driving an infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 ºC.

# AC Characteristics

Figure 57 and Table 20 describe the Alternating Current (AC) characteristics.

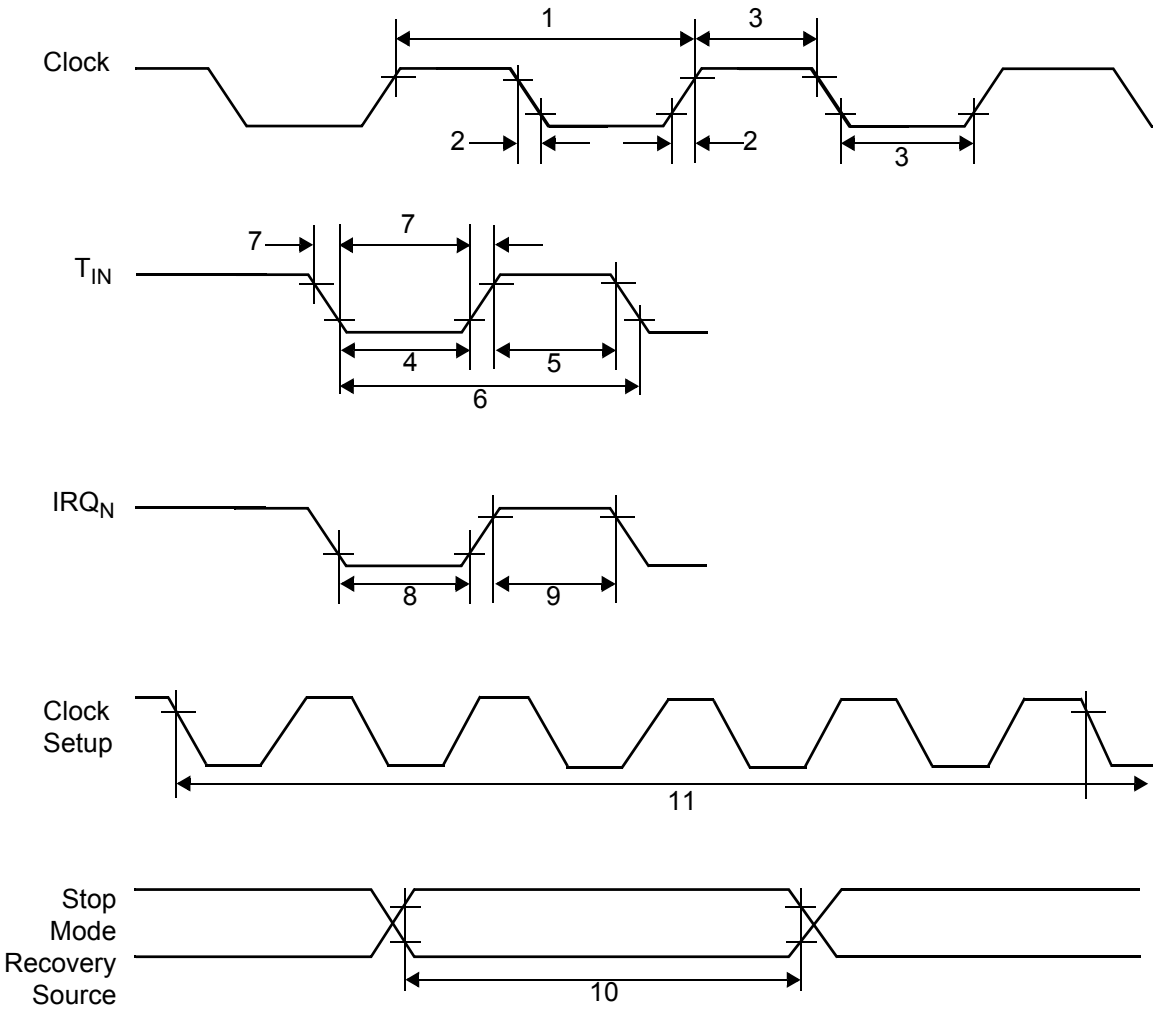



**Figure 57. AC Timing Diagram**

# Index

## Numerics



## A



## B



## C



## D

## S



## T



## V



## W



## X



## Z