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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zlp32300h4816c

Table of Contents

Architectural Overview

Zilog's Crimzon® ZLP32300 is an OTP-based member of the MCU family of infrared microcontrollers. With 237 B of general-purpose RAM and 8 KB to 32 KB of OTP, Zilog's CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Crimzon ZLP32300 architecture (see Figure 1 on page 3) is based on Zilog's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® CPU offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations:

1. Program Memory
2. Register File
3. Expanded Register File

The register file is composed of 256 Bytes of RAM. It includes four I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Crimzon ZLP32300 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2 on page 4). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

Note: *All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.*

Power connections use the conventional descriptions listed in Table 1.

Table 1. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

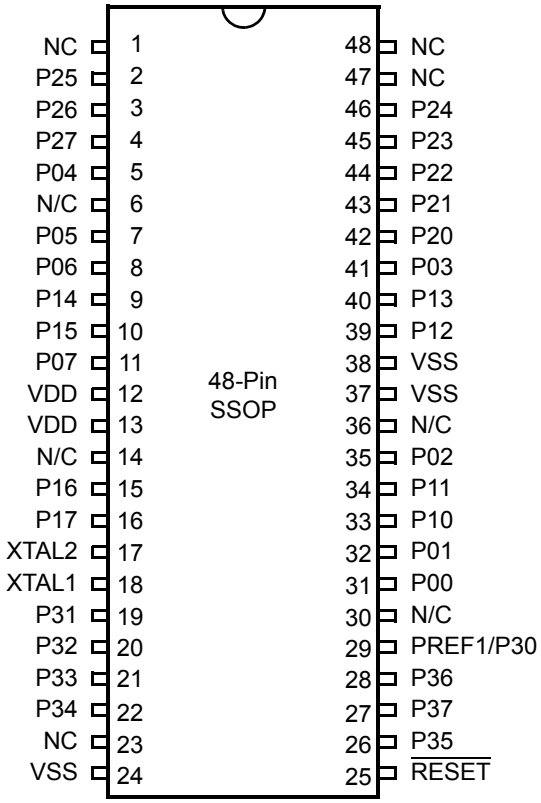


Figure 6. 48-Pin SSOP Pin Configuration

Table 5. 40- and 48-Pin Configuration

40-Pin PDIP No	48-Pin SSOP No	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11

Table 5. 40- and 48-Pin Configuration (Continued)

40-Pin PDIP No	48-Pin SSOP No	Symbol
	14	NC
	30	NC
	36	NC

Pin Functions

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonant to the on-chip oscillator output.

Input/Output Ports

Caution: *The CMOS input buffer for each Port 0, 1, or 2 pin is always connected to the pin, even when the pin is configured as an output. If the pin is configured as an open-drain output and no external signal is applied, a High output state can cause the CMOS input buffer to float. This might lead to excessive leakage current of more than 100 µA. To prevent this leakage, connect the pin to an external signal with a defined logic level or ensure its output state is Low, especially during STOP mode.*

Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

Port 0, 1, and 2 have both input and output capability. The input logic is always present no matter whether the port is configured as input or output. When doing a READ instruction, the MCU reads the actual value at the input logic but not from the output buffer. In addition, the instructions of OR, AND, and XOR have the Read-Modify-Write sequence. The MCU first reads the port, and then modifies the value and load back to the port.

Precaution must be taken if the port is configured as open-drain output or if the port is driving any circuit that makes the voltage different from the desired output logic. For example, pins P00–P07 are not connected to anything else. If it is configured as

open-drain output with output logic as ONE, it is a floating port and reads back as ZERO. The following instruction sets P00-P07 all Low.

```
AND P0,#%F0
```

Port 0 (P00–P07)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 01 mode register (P01M). After a hardware reset or Stop Mode Recovery, Port 0 is configured as an input port.

An optional pull-up transistor is available as a OTP option bit on all Port 0 bits with nibble select.

Note: *The Port 0 direction is reset to be input following an SMR.*

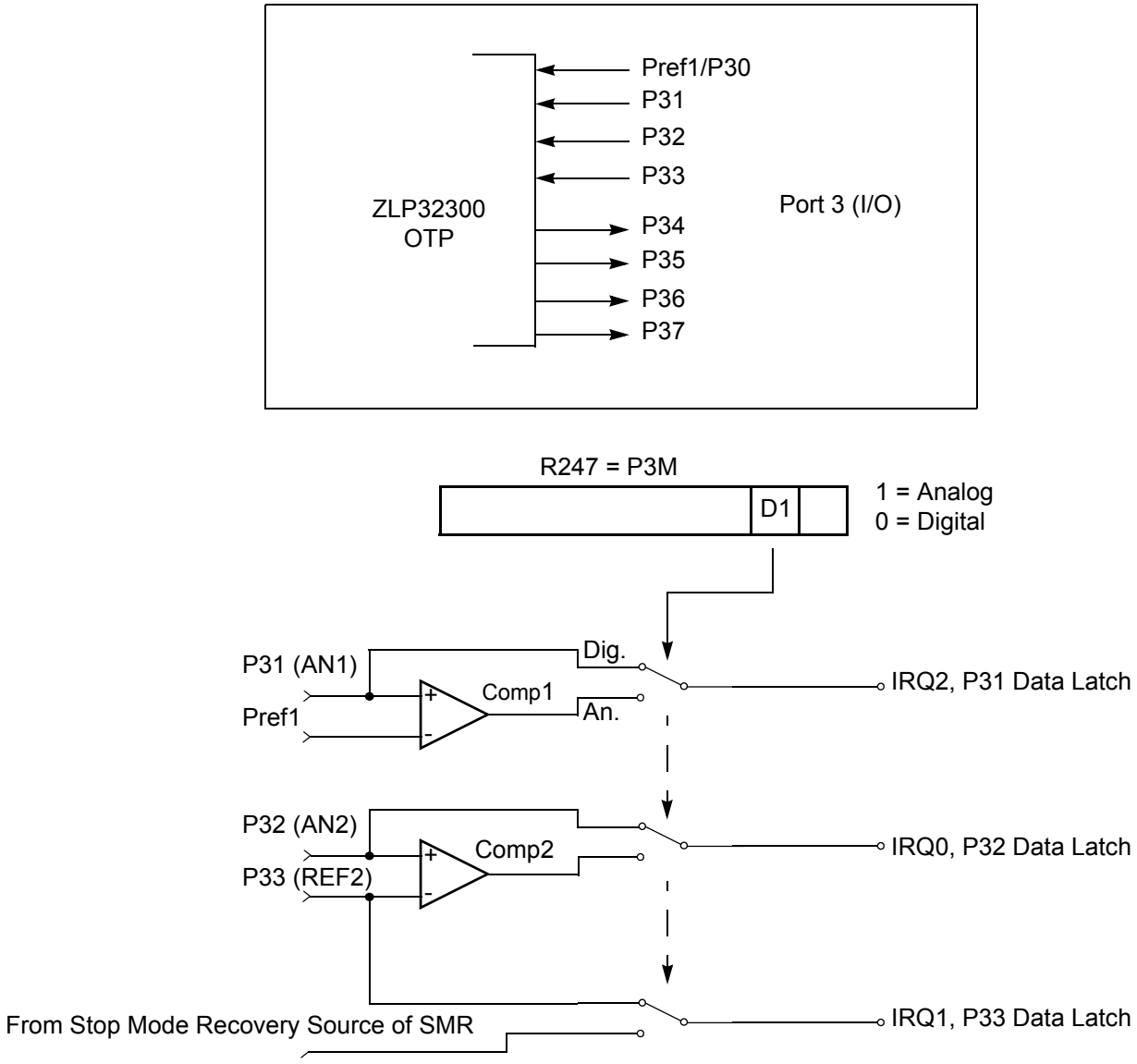


Figure 10. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The Analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20

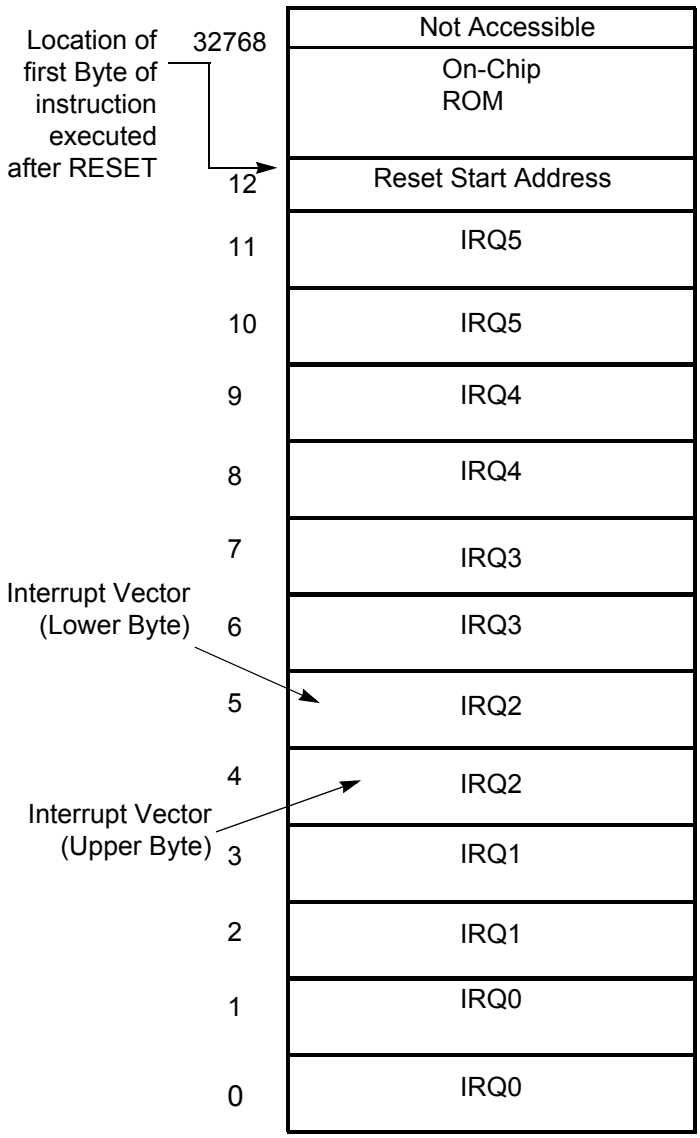


Figure 12. Program Memory Map (32 K OTP)

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8 register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the ERF (Expanded Register File). Bits 7–4 of

register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

Note: *An expanded register bank is also referred to as an expanded register group (see* Figure 13*).*

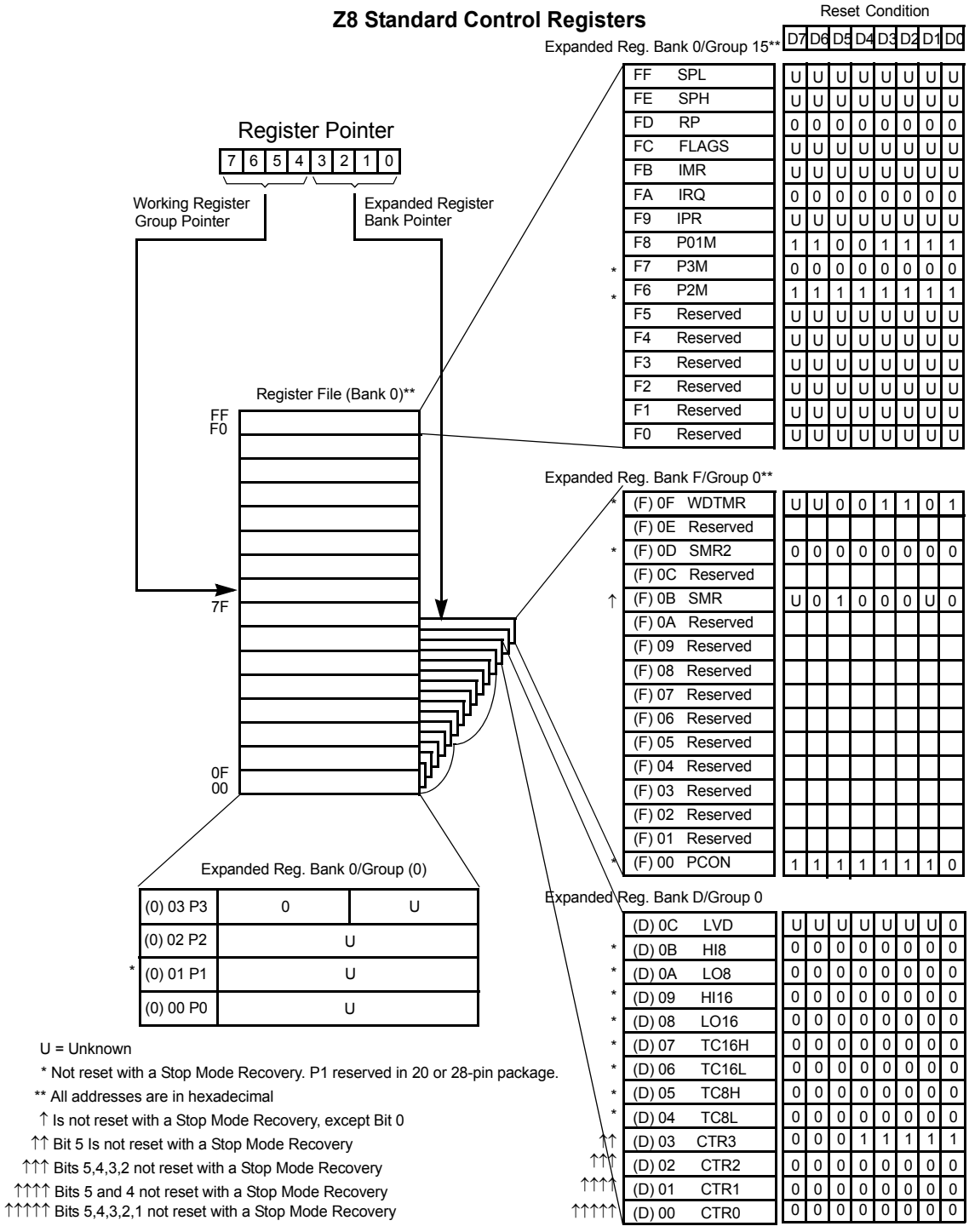


Figure 13. Expanded Register File Architecture

```
LD                      R1, 2                   ; CTR2→CTR1

LD                      RP, #0Dh                ; Select ERF D
for access to bank D
                                                ; (working
register group 0)
LD                      RP, #7Dh                ; Select
expanded register bank D and working            ; register
group 7 of bank 0 for access.
LD                      71h, 2
; CTRL2→register 71h
LD                      R1, 2
; CTRL2→register 71h
```

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 7 on page 27) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (see Figure 15). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note: *Working register group E0–EF can only be accessed through working registers and indirect addressing modes.*

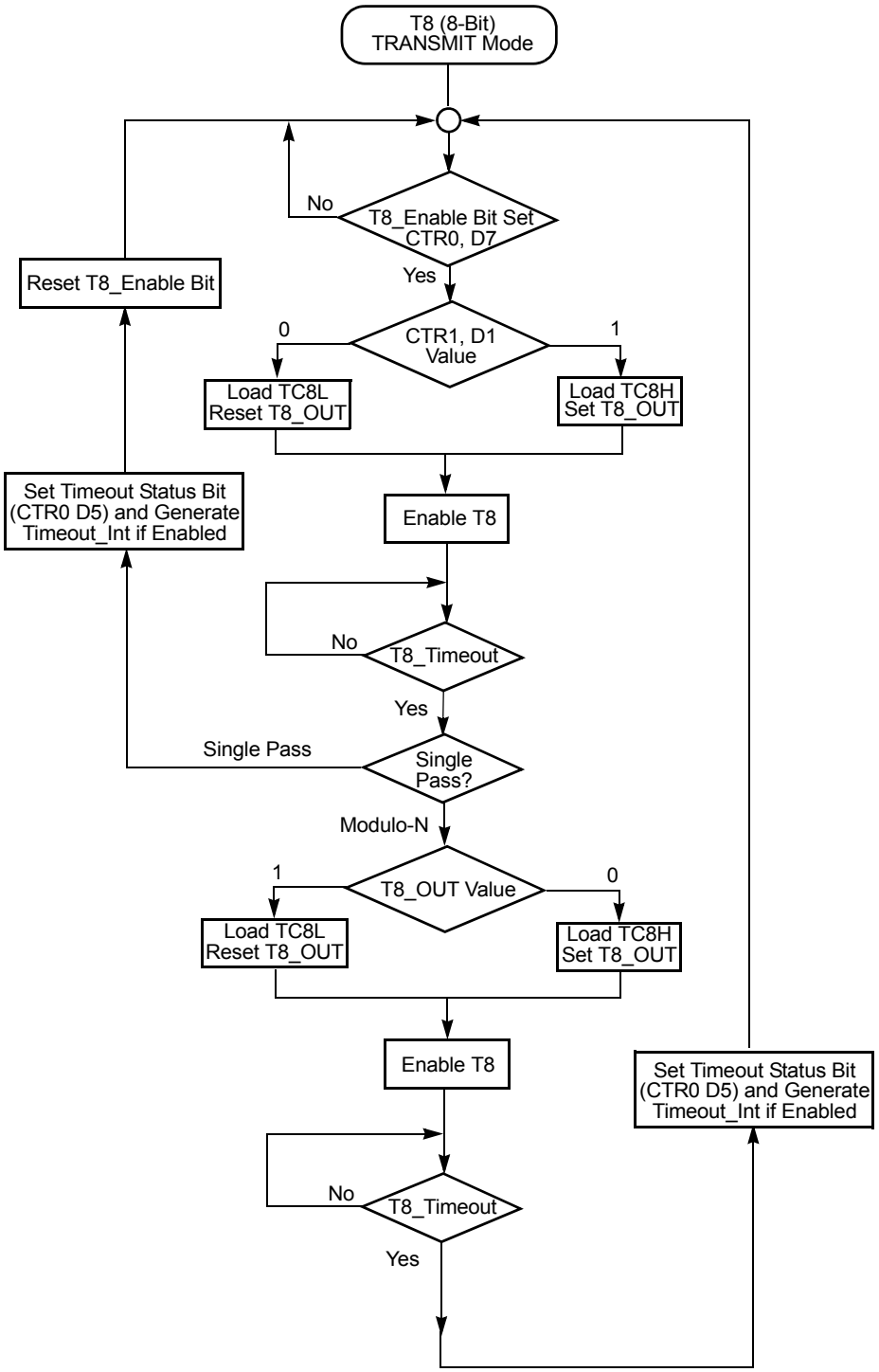


Figure 17. TRANSMIT Mode Flowchart

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0, D5) is set, and a time-out interrupt can be generated if it is enabled (CTR0, D1). In MODULO-N mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the time-out status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle, see Figure 18.

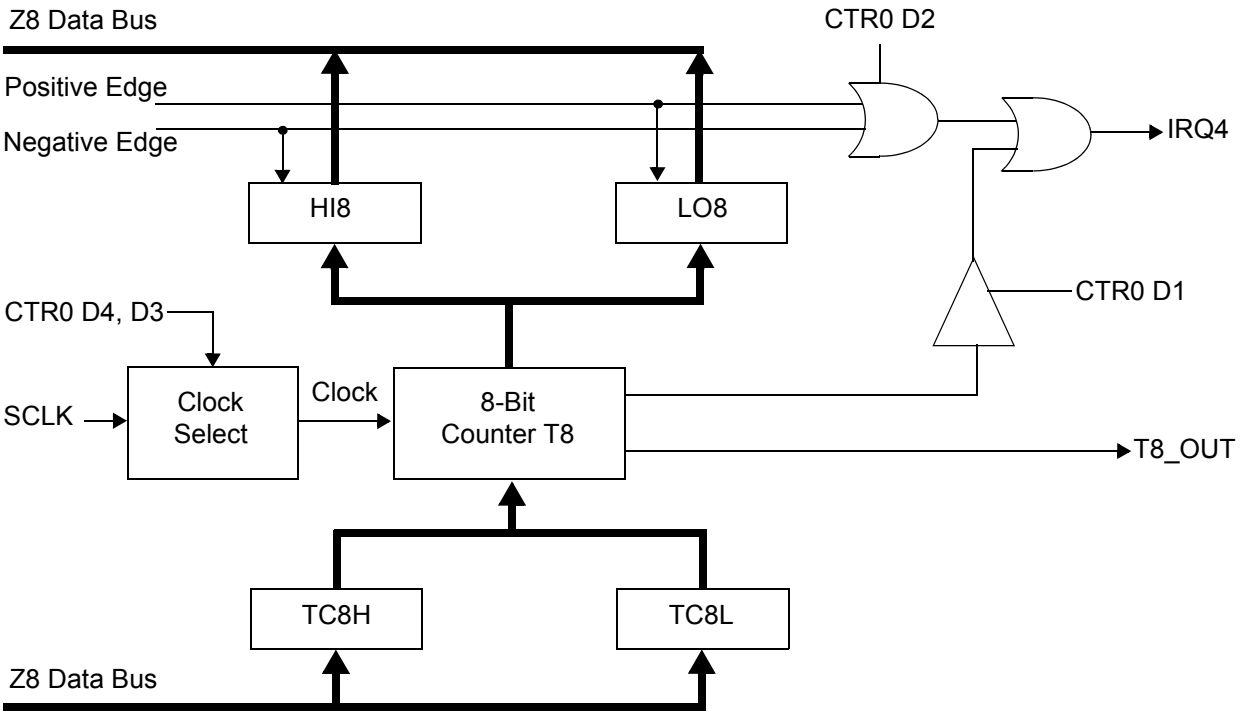


Figure 18. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.

Caution: *To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to* FFh *to* FEh.

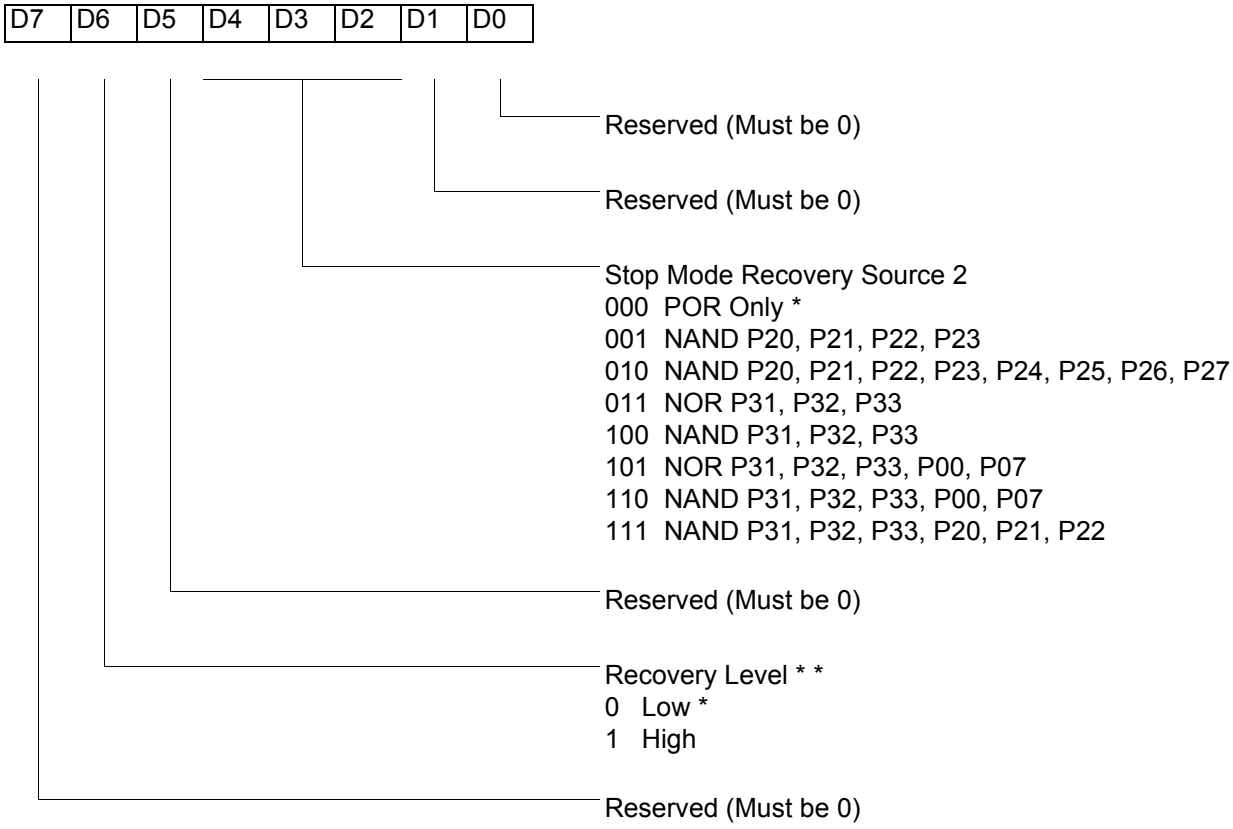
Note: *The letter* h *denotes hexadecimal values.*

Transition from 0 to FFh is not a timeout condition.

Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (see Figure 34).

SMR2(0F)Dh

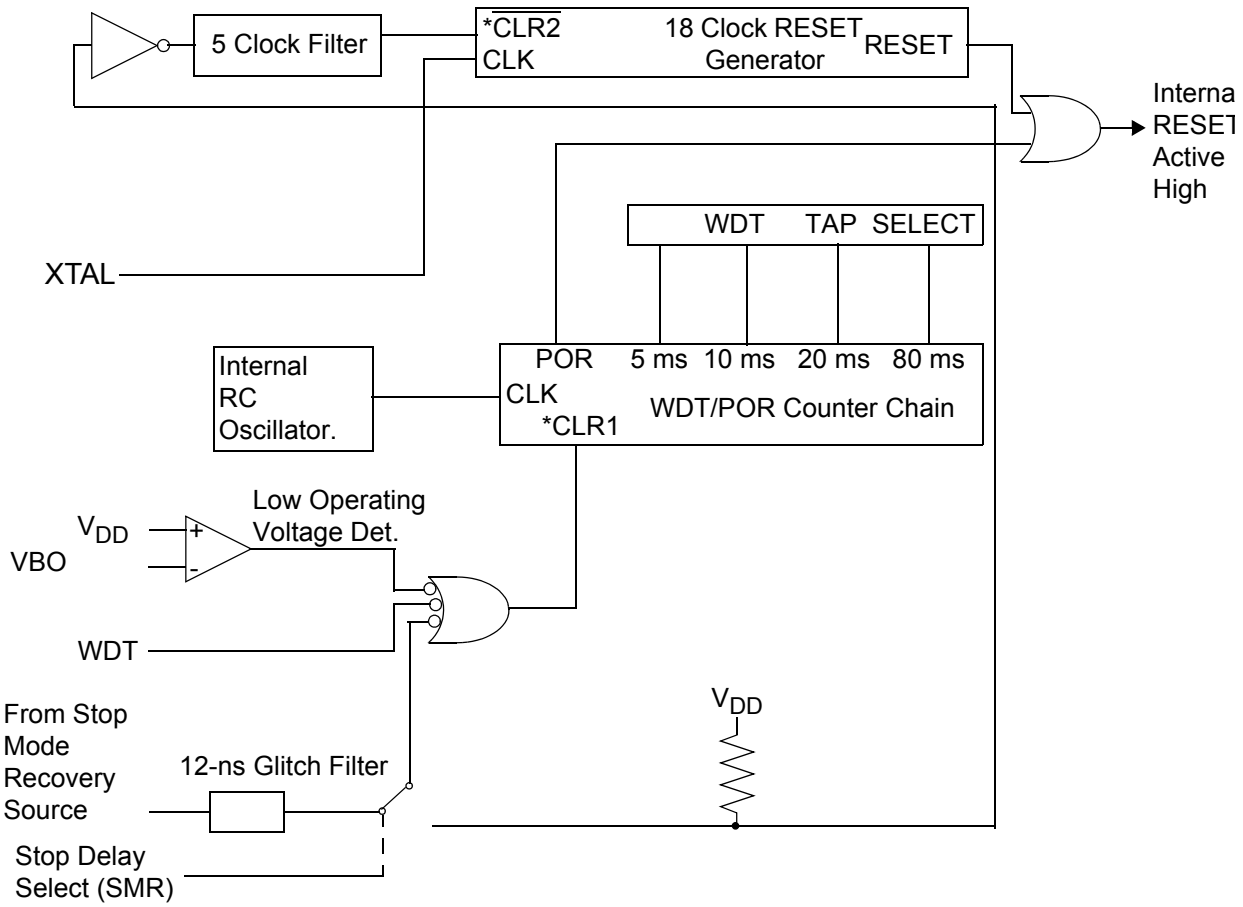


If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.
*Default setting after reset.
* *At the XOR gate input.

Figure 34. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

Note: *Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.*



* CLR1 and $\overline{CLR2}$ enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-High

Figure 36. Resets and WDT

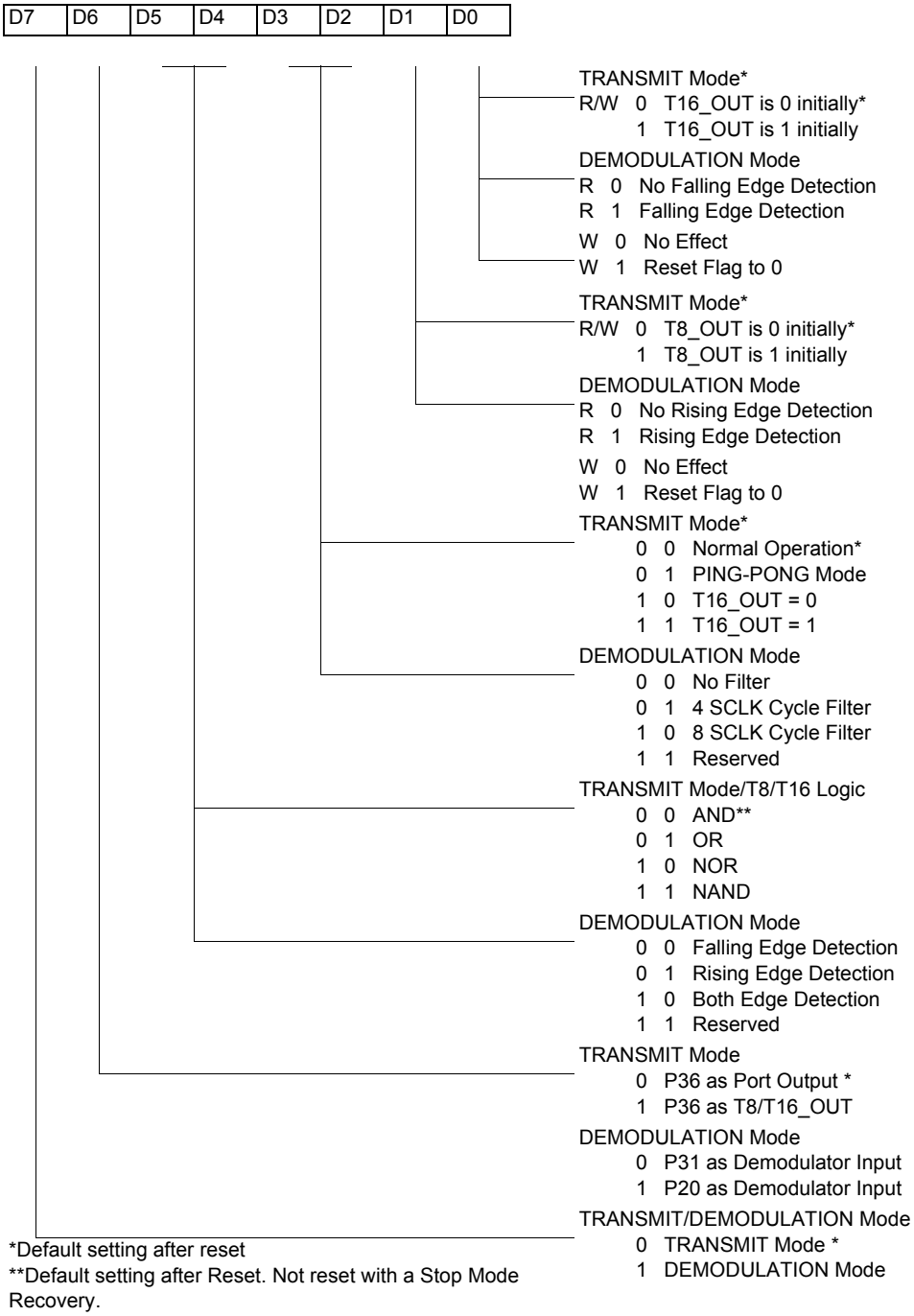
WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP mode. A 1 indicates active during Stop. The default is 1.

EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These are listed in Table 16.

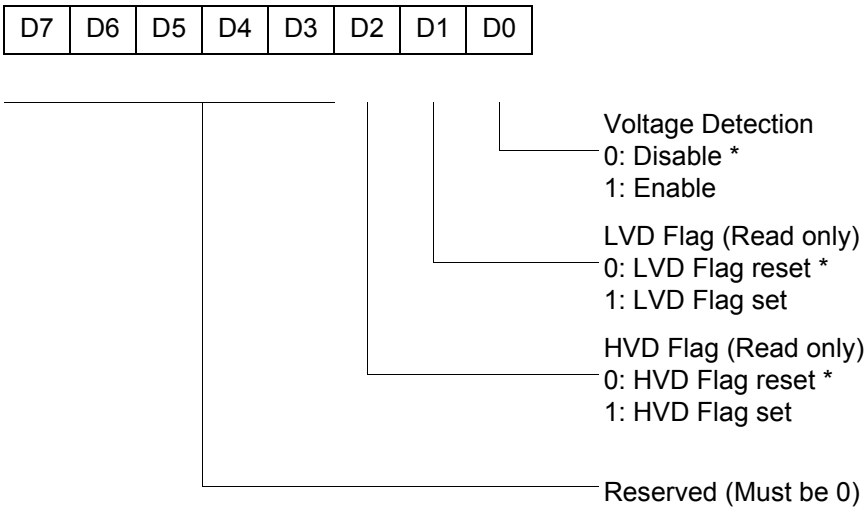
CTR1(0D)01H



*Default setting after reset
**Default setting after Reset. Not reset with a Stop Mode Recovery.

Figure 38. T8 and T16 Common Control Functions ((0D)01H: Read/Write)

LVD(0D)0CH



*Default setting after reset.

Figure 41. Voltage Detection Register

Note: *Do not modify register P01M while checking a low-voltage condition. Switching noise of both Ports 0 and 1 together might trigger the LVD Flag.*

R254 SPH(FEH)

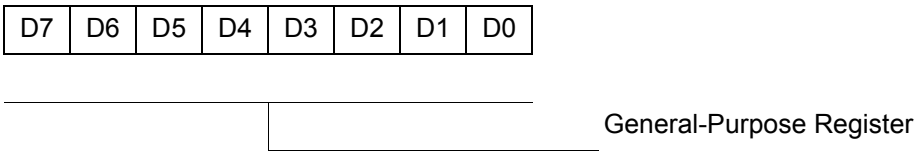


Figure 54. Stack Pointer High (FEH: Read/Write)

R255 SPL(FFH)

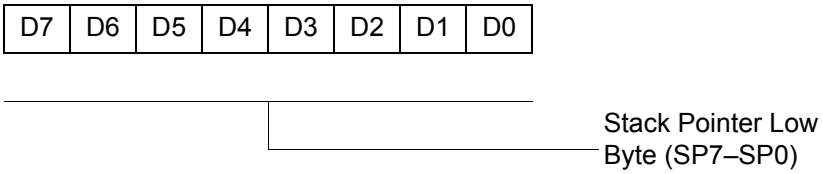
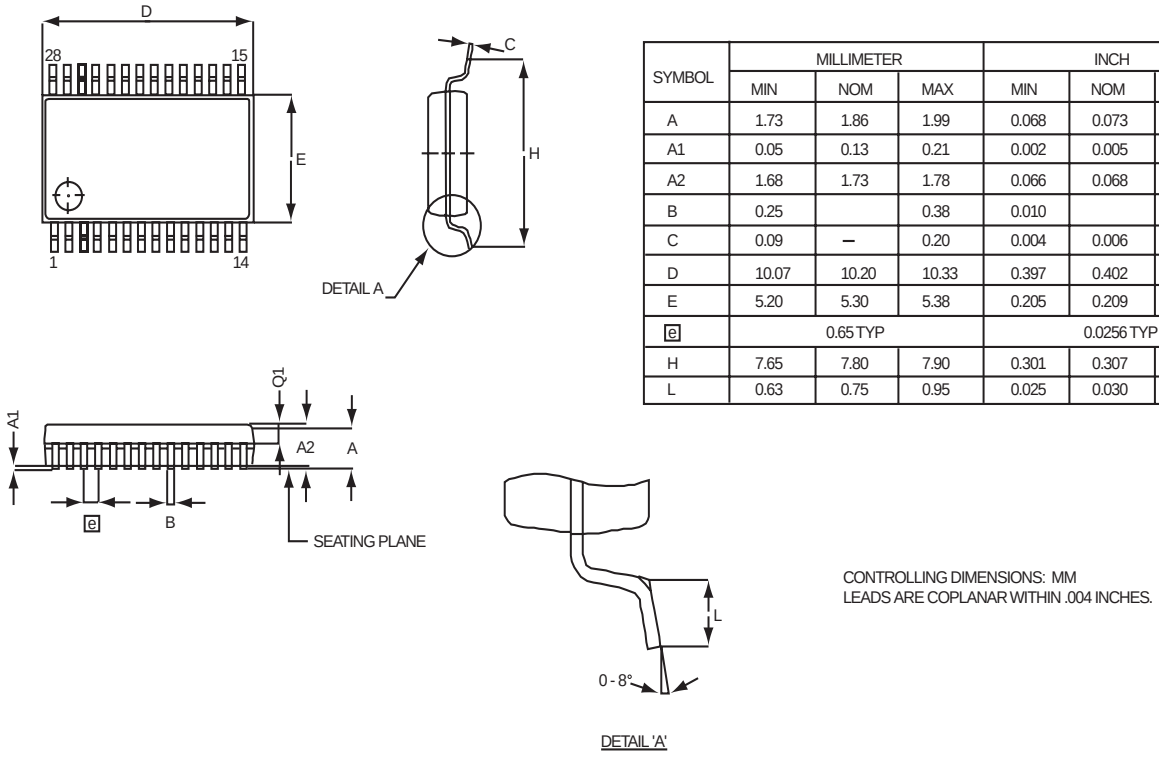


Figure 55. Stack Pointer Low (FFH: Read/Write)

Table 20. AC Characteristics

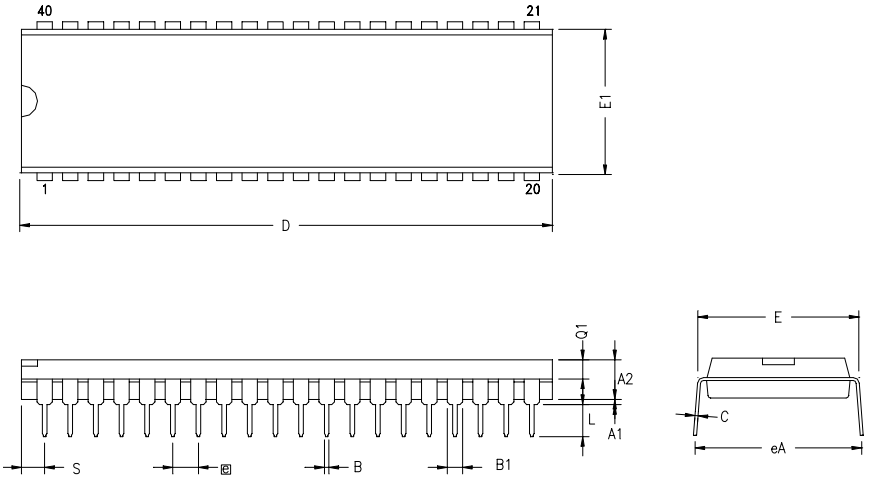
			T_A=0 °C to +70 °C 8.0 MHz					Watchdog Timer Mode Register (D1, D0)
No	**Symbol**	**Parameter**	**V_{CC}**	**Minimum**	**Maximum**	**Units**	**Notes**	
1	TpC	Input Clock Period	2.0–3.6	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1	
3	TwC	Input Clock Width	2.0–3.6	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–3.6	3TpC			1	
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–3.6	5TpC			1, 2	
10	Twsm	Stop Mode Recovery Width Spec	2.0–3.6	12 10TpC		ns	3 4	
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4	
12	Twdt	Watchdog Timer Delay Time	2.0–3.6 2.0–3.6 2.0–3.6 2.0–3.6	5 10 20 80		ms ms ms ms		0, 0 0, 1 1, 0 1, 1
13	T_{POR}	Power-on reset	2.0–3.6	2.5	10	ms		

Notes
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR–D5 = 1.
4. SMR–D5 = 0.



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.86	1.99	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.78	0.066	0.068	0.070
B	0.25		0.38	0.010		0.015
C	0.09	–	0.20	0.004	0.006	0.008
D	10.07	10.20	10.33	0.397	0.402	0.407
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.63	0.75	0.95	0.025	0.030	0.037

Figure 63. 28-Pin SSOP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

Figure 64. 40-Pin PDIP Package Diagram

Device	Part Number	Description
	ZLP32300P2008G	20-pin PDIP 8 K OTP
	ZLP32300S2008G	20-pin SOIC 8 K OTP
	ZLP32300H4804G	48-pin SSOP 4 K OTP
	ZLP32300P4004G	40-pin PDIP 4 K OTP
	ZLP32300H2804G	28-pin SSOP 4 K OTP
	ZLP32300P2804G	28-pin PDIP 4 K OTP
	ZLP32300S2804G	28-pin SOIC 4 K OTP
	ZLP32300H2004G	20-pin SSOP 4 K OTP
	ZLP32300P2004G	20-pin PDIP 4 K OTP
	ZLP32300S2004G	20-pin SOIC 4 K OTP
	ZLP323ICE01ZAC*	40-PDIP/48-SSOP Accessory Kit
	Note: *ZLP323ICE01ZAC has been replaced by an improved version, ZCRMZNICE02ZACG.	
	ZLP128ICE01ZEMG	In-Circuit Emulator
	Note: *ZLP128ICE01ZEMG has been replaced by an improved version, ZCRMZNICE01ZEMG.	
	ZCRMZNICE01ZEMG	Crimzon In-Circuit Emulator
	ZCRMZN00100KITG	Crimzon In-Circuit Emulator Development Kit
	ZCRMZNICE01ZACG	20-Pin Accessory Kit
	ZCRMZNICE02ZACG	40/48-Pin Accessory Kit

Notes
1. Replace C with G for Lead-Free Packaging.
2. Contact www.zilog.com for the die form.

For fast results, contact your local Zilog® sales office for assistance in ordering the part(s) desired.