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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zlp32300h4816c00tr

Revision History

Each instance in the Revision History table reflects a change to this document from its previous revision. For more details, refer to the corresponding pages or appropriate link in the table.

Date	Revision Level	Description	Page Number
February 2008	23	Updated Ordering Information section.	87
January 2008	22	Updated Ordering Information section.	87
July 2007	21	Updated Disclaimer section and implemented style guide.	All
February 2007	20	Updated Low-Voltage Detection.	58
May 2006	19	Updated Figure 33 with pin P22 in SMR block input.	52
December 2005	18	Updated Clock and Input/Output Ports sections.	15 and 51

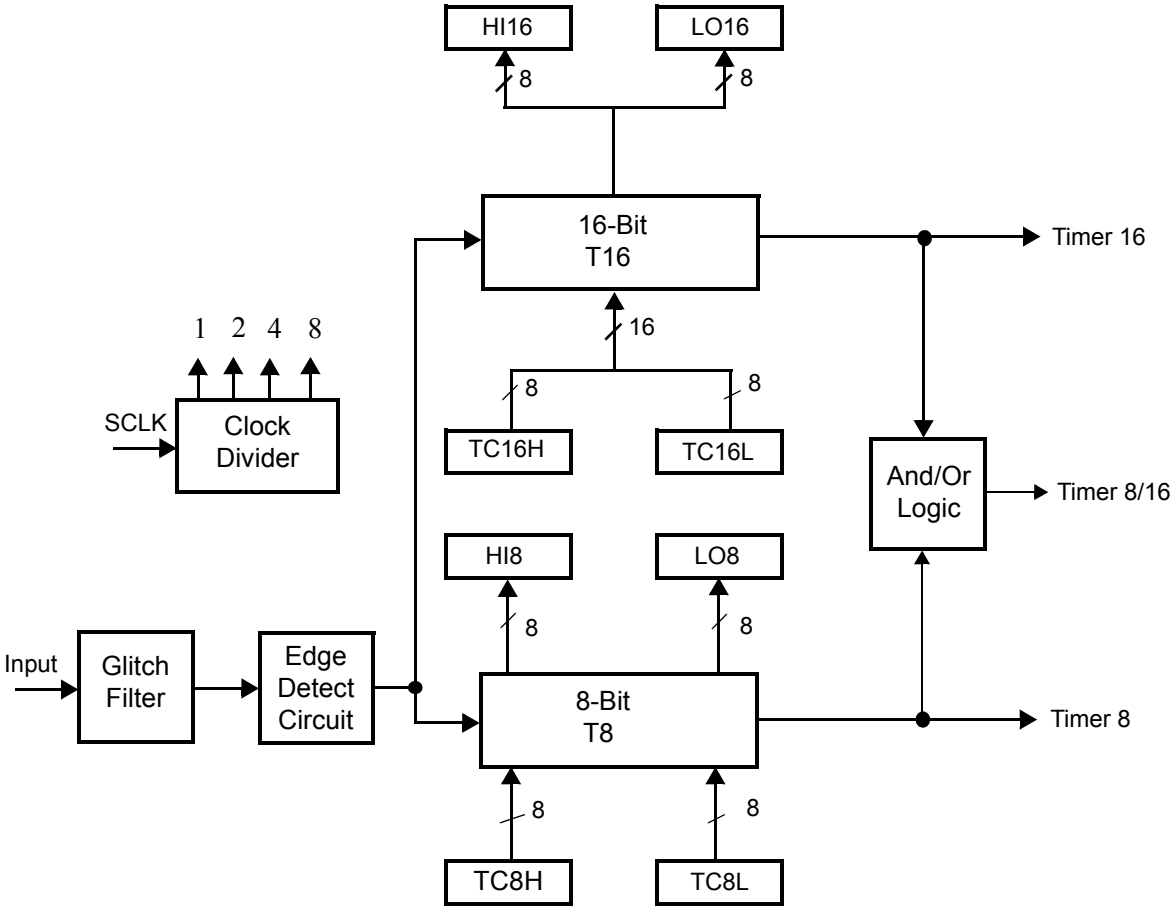


Figure 2. Counter/Timers Diagram

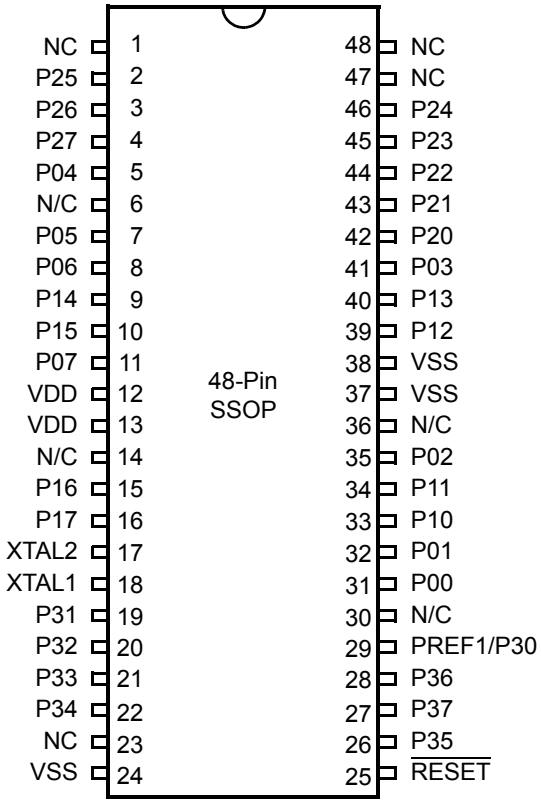


Figure 6. 48-Pin SSOP Pin Configuration

Table 5. 40- and 48-Pin Configuration

40-Pin PDIP No	48-Pin SSOP No	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11

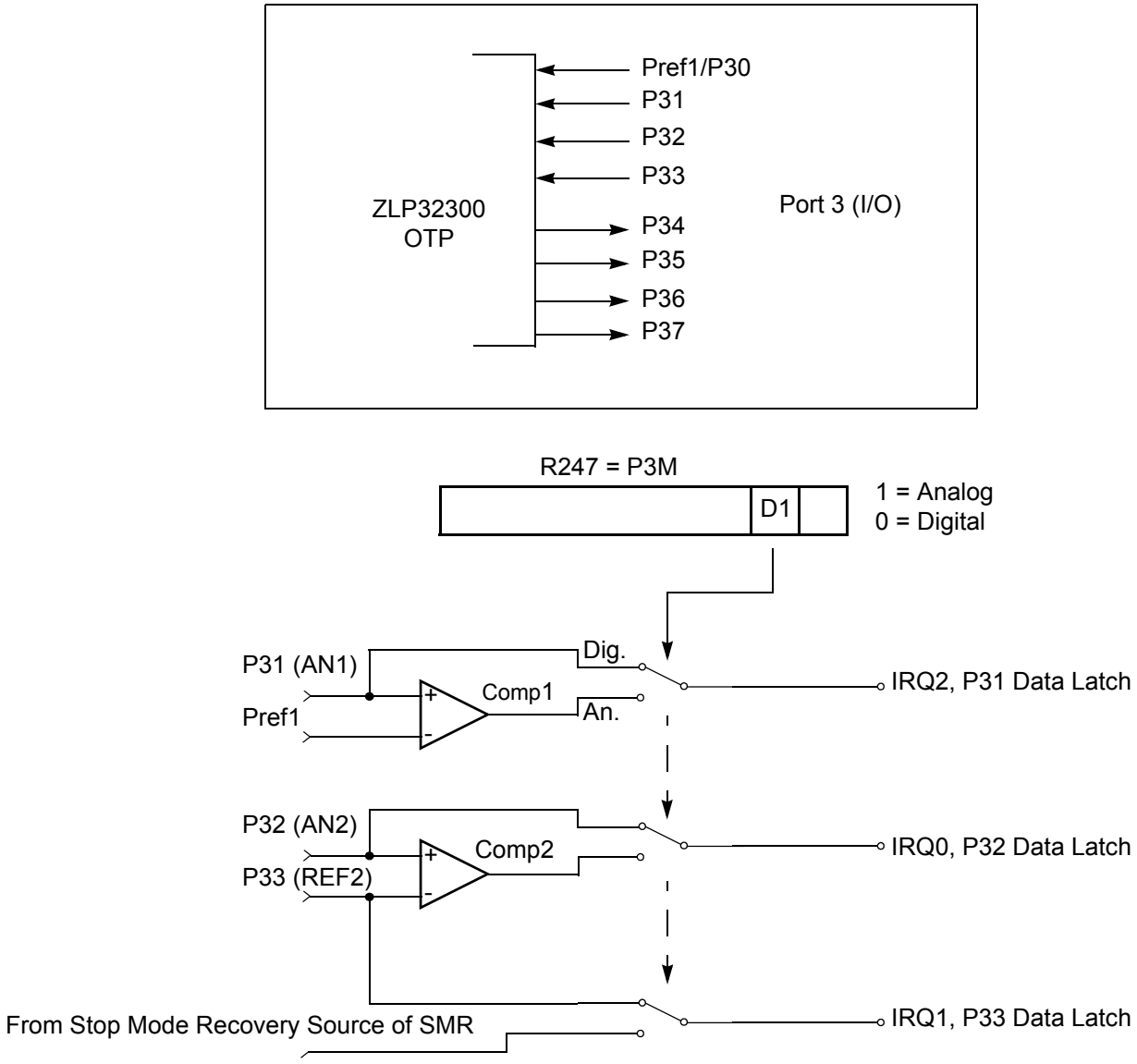


Figure 10. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The Analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20

register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

Note: *An expanded register bank is also referred to as an expanded register group (see* Figure 13*).*

Counter/Timer8 High Hold Register—TC8H(D)05h

Field	Bit Position		Description
T8_Level_HI	[7:0]	R/W	Data

Counter/Timer8 Low Hold Register—TC8L(D)04h

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

CTR0 Counter/Timer8 Control Register—CTR0(D)00h

Table 7 lists and briefly describes the fields for this register.

Table 7. CTR0(D)00h Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R/W	0* 1 0 1	Counter Disabled Counter Enabled Stop Counter Enable Counter
Single/Modulo-N	-6-------	R/W	0* 1	Modulo-N Single Pass
Time_Out	--5------	R/W	0** 1 0 1	No Counter Time-Out Counter Time-Out Occurred No Effect Reset Flag to 0
T8 _Clock	---43---	R/W	0 0** 0 1 1 0 1 1	SCLK SCLK/2 SCLK/4 SCLK/8
Capture_INT_Mask	-----2--	R/W	0** 1	Disable Data Capture Interrupt Enable Data Capture Interrupt
Counter_INT_Mask	------1-	R/W	0** 1	Disable Time-Out Interrupt Enable Time-Out Interrupt
P34_Out	-------0	R/W	0* 1	P34 as Port Output T8 Output on P34

*Indicates the value upon Power-On Reset.
**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

CTR3 T8/T16 Control Register—CTR3(D)03h

Table 10 lists and briefly describes the fields for this register. This register allows the T_8 and T_{16} counters to be synchronized.

Table 10.CTR3 (D)03h: T8/T16 Control Register

Field	Bit Position		Value	Description
T_{16} Enable	7-------	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T_8 Enable	-6------	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	--5-----	R/W	0**	Disable Sync Mode
			1	Enable Sync Mode
Reserved	---43210	R	1	Always reads 11111
		W	x	No Effect

*Indicates the value upon Power-On Reset.
**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 16).

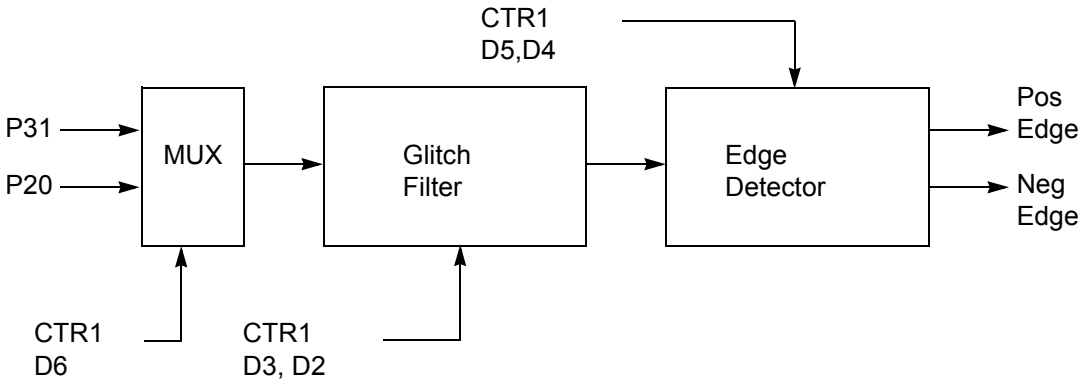


Figure 16. Glitch Filter Circuitry

T8 TRANSMIT Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 17.

interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 21 and Figure 22).

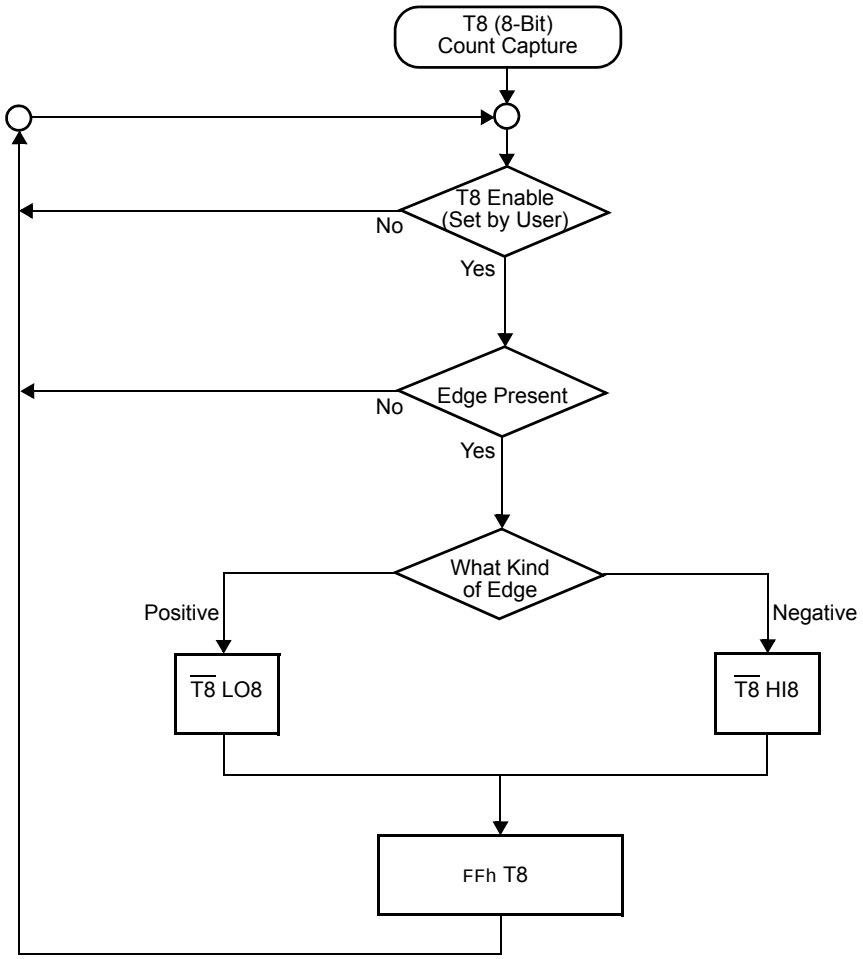


Figure 21. DEMODULATION Mode Count Capture Flowchart

T16 TRANSMIT Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set, see Figure 23.

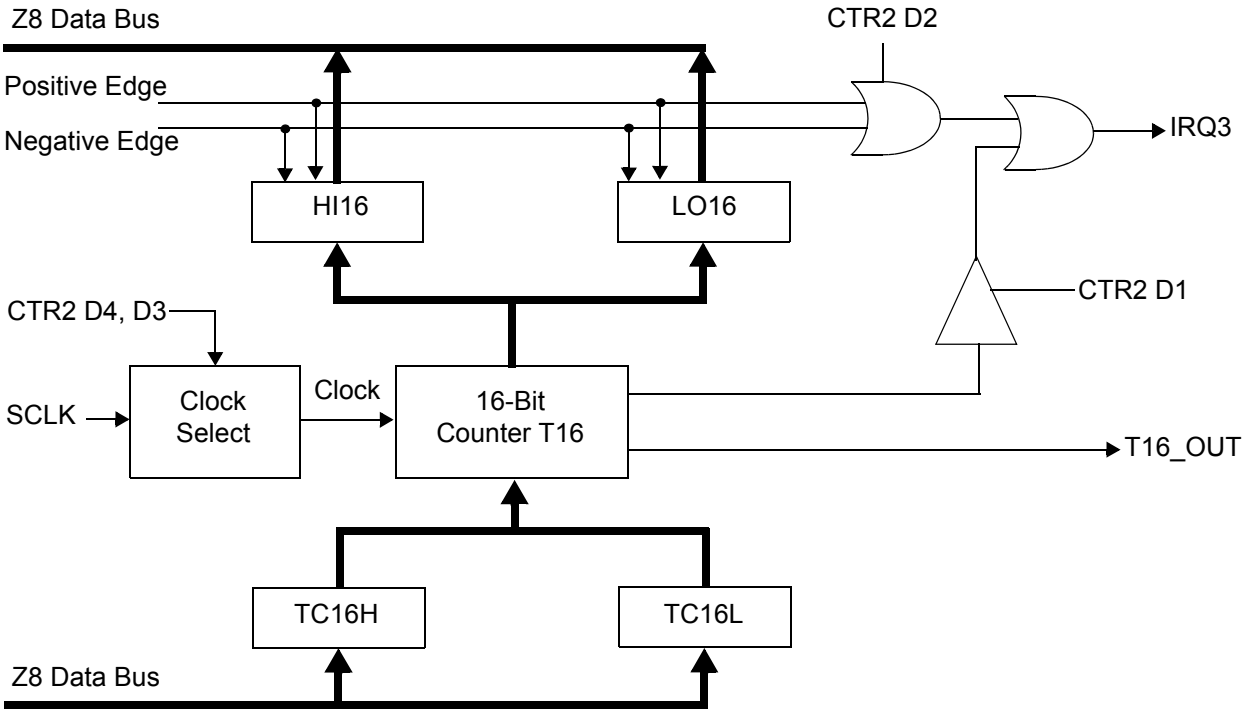


Figure 23. 16-Bit Counter/Timer Circuits

Note: *Global interrupts override this function as described in* Interrupts on page 43.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 24). If it is in MODULO-N mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 25).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.

Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into SINGLE-PASS mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the PING-PONG mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7), see Figure 26.

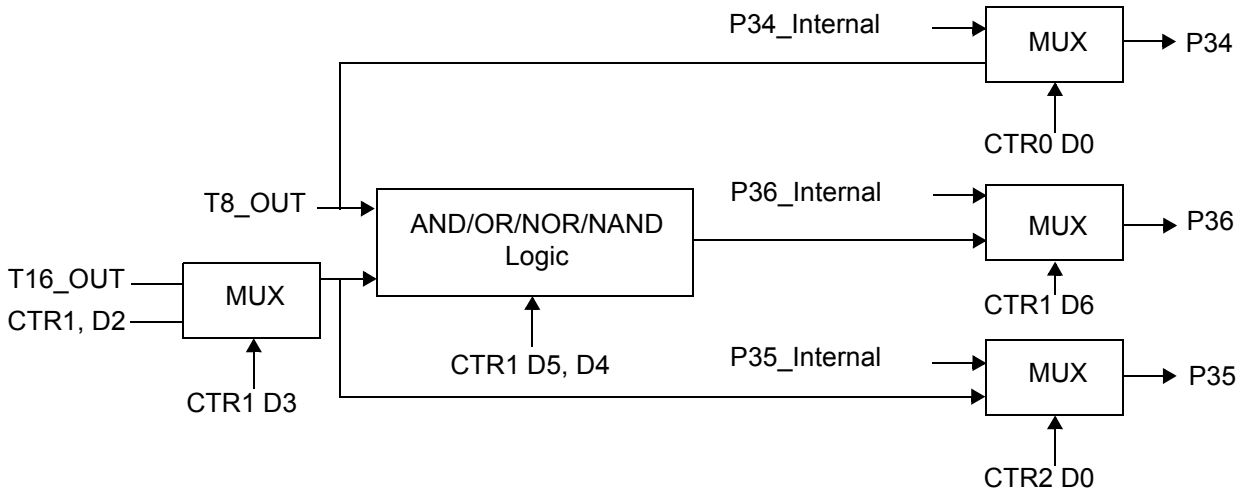


Figure 27. Output Circuit

The initial value of T8 or T16 must not be `1`. If you stop the timer and restart the timer, reload the initial value to avoid an unknown previous value.

During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

Timer Output

The output logic for the timers is displayed in Figure 27. P34 is used to output T8-OUT when D0 of CTR0 is set. P35 is used to output the value of TI6-OUT when D0 of CTR2 is set. When D6 of CTR1 is set, P36 outputs the logic combination of T8-OUT and T16-OUT determined by D5 and D4 of CTR1.

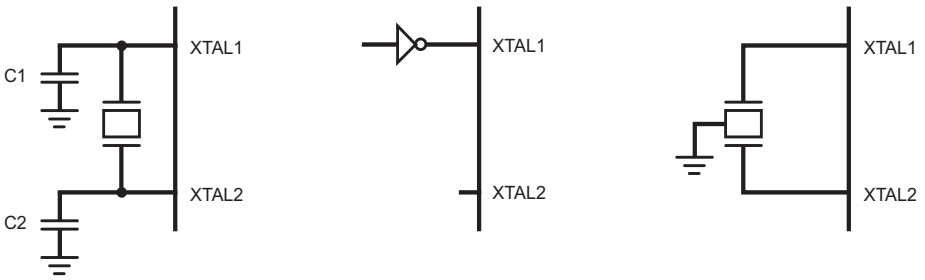
Interrupts

The Crimzon ZLP32300 features six different interrupts (see Table 11 on page 45). The interrupts are maskable and prioritized (see Figure 28). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the

Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω. The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors from each pin to ground. The typical capacitor value is 10 pF for 8 MHz. Also check with the crystal supplier for the optimum capacitance.



Crystal
C1, C2 = 10 pF *
f = 8 MHz

External Clock

Ceramic Resonator f = 8 MHz

*Note: preliminary value.

Figure 29. Oscillator Configuration

Zilog's IR MCU supports crystal, resonator, and oscillator. Most resonators have a frequency tolerance of less than ±0.5%, which is enough for remote control application. Resonator has a very fast startup time, which is around few hundred microseconds. Most crystals have a frequency tolerance of less than 50 ppm (±0.005%). However, crystal needs longer startup time than the resonator. The large loading capacitance slows down the oscillation startup time. Zilog® suggests not to use more than 10 pF loading capacitor for the crystal. If the stray capacitance of the PCB or the crystal is high, the loading capacitance C1 and C2 must be reduced further to ensure stable oscillation before the T_{POR} (Power-On Reset time is typically 5-6 ms, see Table 20 on page 79).

For Stop Mode Recovery operation, bit 5 of SMR register allows you to select the Stop Mode Recovery delay, which is the T_{POR}. If Stop Mode Recovery delay is not selected, the MCU executes instruction immediately after it wakes up from the STOP mode. If resonator or crystal is used as a clock source then Stop Mode Recovery delay needs to be selected (bit 5 of SMR = 1).

Table 14. Stop Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Note: *Any Port 2 bit defined as an output drives the corresponding input to the default state. For example, if the NOR of P23-P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23-P21) form the NOR equation. This condition allows the remaining inputs to control the AND/OR function, refer to SMR2 register* on page 54 *for other recover sources.*

Stop Mode Recovery Delay Select (D5)

This bit, if low, disables the T_{POR} delay after Stop Mode Recovery. The default configuration of this bit is 1. If the 'fast' wake up is selected, the Stop Mode Recovery source must be kept active for at least 10 TpC.

Note: *This bit must be set to 1 if a crystal or resonator clock source is used. The T_{POR} delay allows the clock source to stabilize before executing instructions.*

Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Crimzon ZLP32300 from STOP mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from STOP mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery.

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 15.

Table 15. Watchdog Timer Time Select

D1	D0	Timeout of Internal RC-Oscillator
0	0	5 ms min
0	1	10 ms min
1	0	20 ms min
1	1	80 ms min

WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1, see Figure 36.

Voltage Detection and Flags

The Voltage Detection register (LVD, register 0Ch at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the V_{CC} level is monitored in real time. The HVD Flag (bit 2 of the LVD register) is set only if V_{CC} is higher than $V_{HVD.}$ The LVD Flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD}. When Voltage Detection is enabled, the LVD Flag also triggers IRQ5. The IRQ bit 5 latches the low-voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a Flag only.

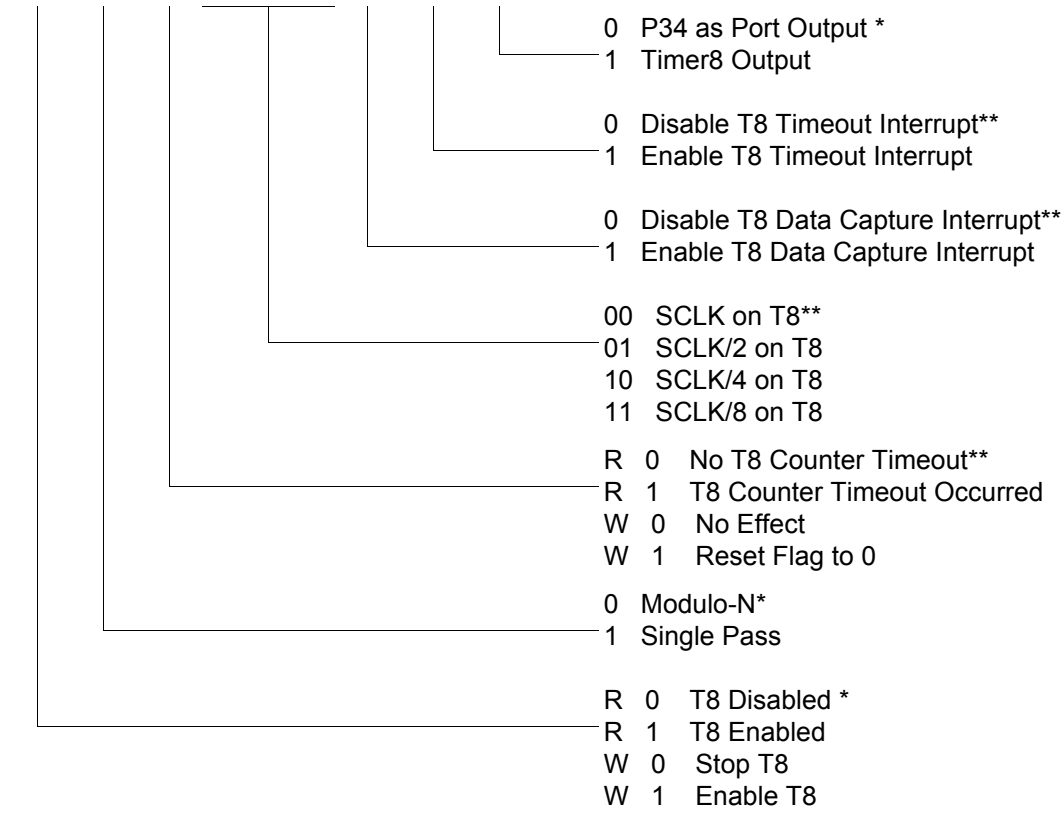
Note: *If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt (EI) instruction prior to enabling the voltage detection.*

Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are displayed in Figure 37 through Figure 41.

CTR0(0D)00H

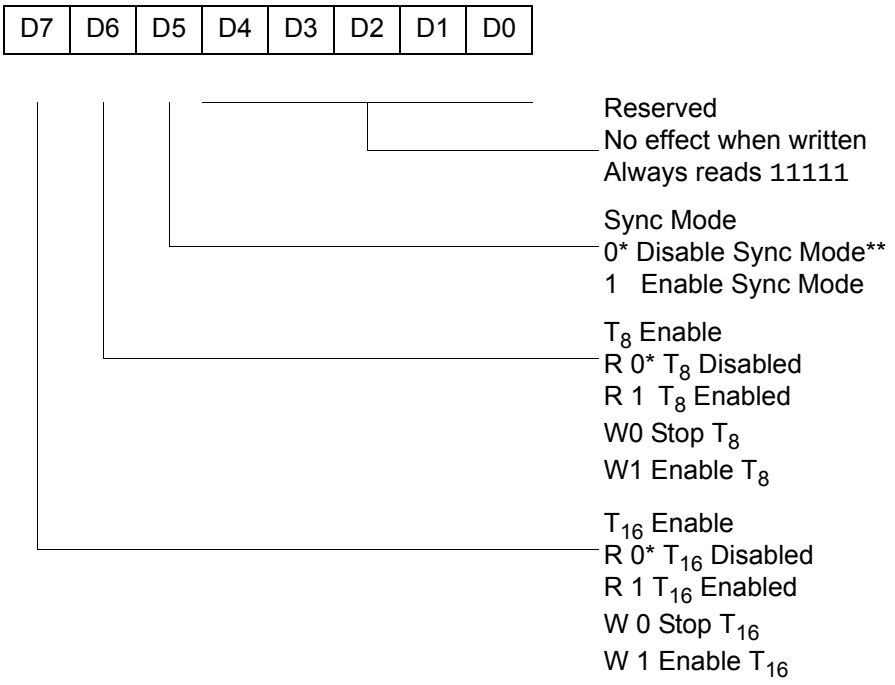
D7	D6	D5	D4	D3	D2	D1	D0



*Default setting after reset.
**Default setting after reset. Not reset with a Stop Mode Recovery.

Figure 37. TC8 Control Register ((0D)O0H: Read/Write Except Where Noted)

CTR3(0D)03H



*Default setting after reset.
**Default setting after reset. Not reset with a Stop Mode Recovery.

Figure 40. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)

Note: *If Sync Mode is enabled, the first pulse of T8 carrier is always synchronized with T16 (demodulated signal). It can always provide a full carrier pulse.*

Standard Control Registers

The standard control registers are displayed in Figure 46 through Figure 55 on page 74.

R246 P2M(F6H)

D7	D6	D5	D4	D3	D2	D1	D0

P27–P20 I/O Definition
0 Defines bit as OUTPUT
1 Defines bit as INPUT *

*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 46. Port 2 Mode Register (F6H: Write Only)

R247 P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0

0: Port 2 Open Drain *
1: Port 2 Push-Pull

0= P31, P32 DIGITAL Mode*
1= P31, P32 ANALOG Mode

Reserved (Must be 0)

*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 47. Port 3 Mode Register (F7H: Write Only)

Table 20. AC Characteristics

			T_A=0 °C to +70 °C 8.0 MHz					Watchdog Timer Mode Register (D1, D0)
No	**Symbol**	**Parameter**	**V_{CC}**	**Minimum**	**Maximum**	**Units**	**Notes**	
1	TpC	Input Clock Period	2.0–3.6	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1	
3	TwC	Input Clock Width	2.0–3.6	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–3.6	3TpC			1	
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–3.6	5TpC			1, 2	
10	Twsm	Stop Mode Recovery Width Spec	2.0–3.6	12 10TpC		ns	3 4	
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4	
12	Twdt	Watchdog Timer Delay Time	2.0–3.6 2.0–3.6 2.0–3.6 2.0–3.6	5 10 20 80		ms ms ms ms		0, 0 0, 1 1, 0 1, 1
13	T_{POR}	Power-on reset	2.0–3.6	2.5	10	ms		

Notes
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR–D5 = 1.
4. SMR–D5 = 0.

Ordering Information

The Crimzon ZLP32300 is available for the following parts:

Device	Part Number	Description
Crimzon ZLP32300	ZLP32300H4832G	48-pin SSOP 32 K OTP
	ZLP32300P4032G	40-pin PDIP 32 K OTP
	ZLP32300H2832G	28-pin SSOP 32 K OTP
	ZLP32300P2832G	28-pin PDIP 32 K OTP
	ZLP32300S2832G	28-pin SOIC 32 K OTP
	ZLP32300H2032G	20-pin SSOP 32 K OTP
	ZLP32300P2032G	20-pin PDIP 32 K OTP
	ZLP32300S2032G	20-pin SOIC 32 K OTP
	ZLP32300H4816G	48-pin SSOP 16 K OTP
	ZLP32300P4016G	40-pin PDIP 16 K OTP
	ZLP32300H2816G	28-pin SSOP 16 K OTP
	ZLP32300P2816G	28-pin PDIP 16 K OTP
	ZLP32300S2816G	28-pin SOIC 16 K OTP
	ZLP32300H2016G	20-pin SSOP 16 K OTP
	ZLP32300P2016G	20-pin PDIP 16 K OTP
	ZLP32300S2016G	20-pin SOIC 16 K OTP
	ZLP32300H4808G	48-pin SSOP 8 K OTP
	ZLP32300P4008G	40-pin PDIP 8 K OTP
	ZLP32300H2808G	28-pin SSOP 8 K OTP
	ZLP32300P2808G	28-pin PDIP 8 K OTP
	ZLP32300S2808G	28-pin SOIC 8 K OTP
	ZLP32300H2008G	20-pin SSOP 8 K OTP