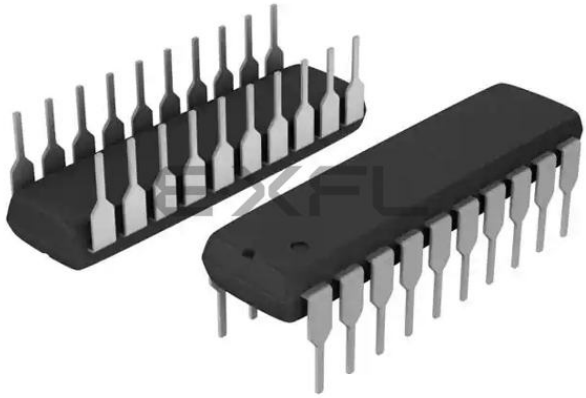

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlp32300p2004g

Revision History

Each instance in the Revision History table reflects a change to this document from its previous revision. For more details, refer to the corresponding pages or appropriate link in the table.

Date	Revision Level	Description	Page Number
February 2008	23	Updated Ordering Information section.	87
January 2008	22	Updated Ordering Information section.	87
July 2007	21	Updated Disclaimer section and implemented style guide.	All
February 2007	20	Updated Low-Voltage Detection.	58
May 2006	19	Updated Figure 33 with pin P22 in SMR block input.	52
December 2005	18	Updated Clock and Input/Output Ports sections.	15 and 51

Table of Contents

Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is displayed in Figure 3 and described in Table 3. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 4. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are displayed in Figure 5, Figure 6, and described in Table 5.

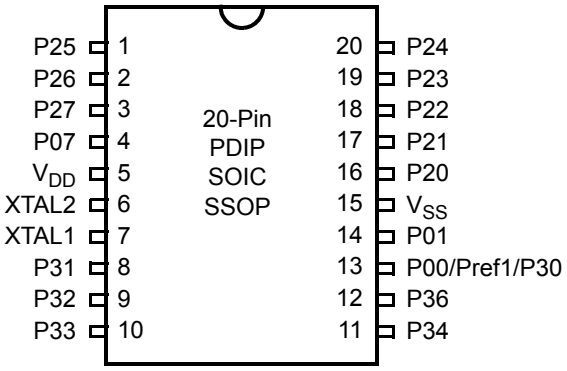


Figure 3. 20-Pin PDIP/SOIC/SSOP Pin Configuration

Table 3. 20-Pin PDIP/SOIC/SSOP Pin Identification

Pin No	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V_{DD}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34, P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V_{SS}	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output

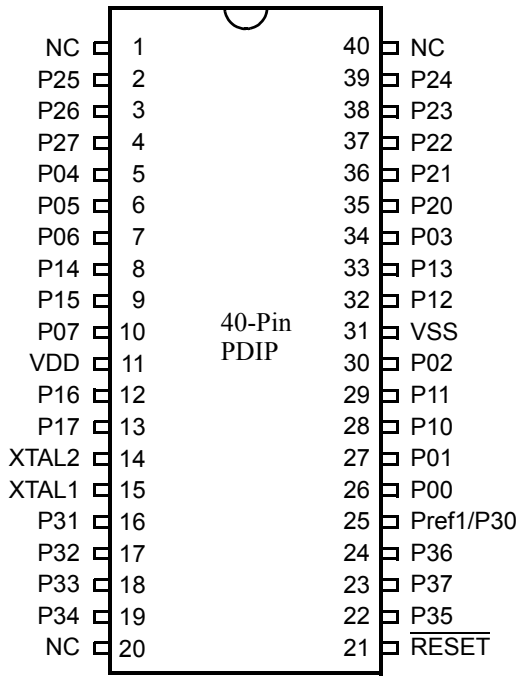


Figure 5. 40-Pin PDIP Pin Configuration

T8_Capture_LO—L08(D)0Ah

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_L0	[7:0]	R/W	Captured Data—No Effect

T16_Capture_HI—HI16(D)09h

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data—No Effect

T16_Capture_LO—L016(D)08h

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	[7:0]	R/W	Captured Data—No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07h

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data

Counter/Timer2 LS-Byte Hold Register—TC16L(D)06h

Field	Bit Position		Description
T16_Data_LO	[7:0]	R/W	Data

Table 8. CTR1(0D)01h T8 and T16 Common Functions (Continued)

Field	Bit Position		Value	Description
Initial_T16_Out/ Falling_Edge	-------0			TRANSMIT Mode
		R/W	0*	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				DEMODULATION Mode
		R	0*	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

*Default at Power-On Reset
**Default at Power-On Reset. Not reset with a Stop Mode Recovery.

Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

P36_Out/Demodulator_Input

In TRANSMIT mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

T8/T16_Logic/Edge _Detect

In TRANSMIT mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter

In TRANSMIT mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to normal operation mode terminates the ‘PING-PONG Mode’ operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION mode, this field defines the width of the glitch that must be filtered out.

Caution: *Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to* FFFFh *to* FFFEh. *Transition from 0 to* FFFFh *is not a timeout condition.*

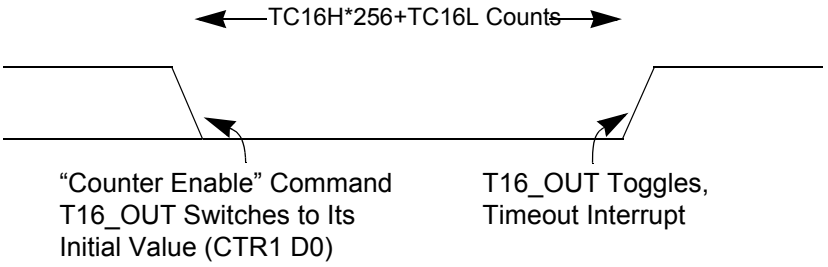


Figure 24. T16_OUT in SINGLE-PASS Mode

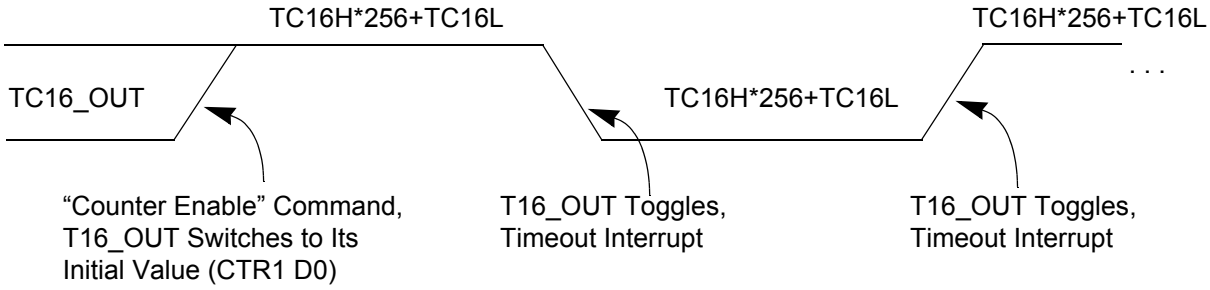


Figure 25. T16_OUT in MODULO-N Mode

T16 DEMODULATION Mode

You must program TC16L and TC16H to FFh. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFh and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

PING-PONG Mode

This operation mode is only valid in TRANSMIT mode. T8 and T16 must be programmed in SINGLE-PASS mode (CTR0, D6; CTR2, D6), and PING-PONG mode must be programmed in CTR1, D3; D2. You can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1, see Figure 26.

Note: *Enabling Ping-Pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status Flags before instituting this operation.*

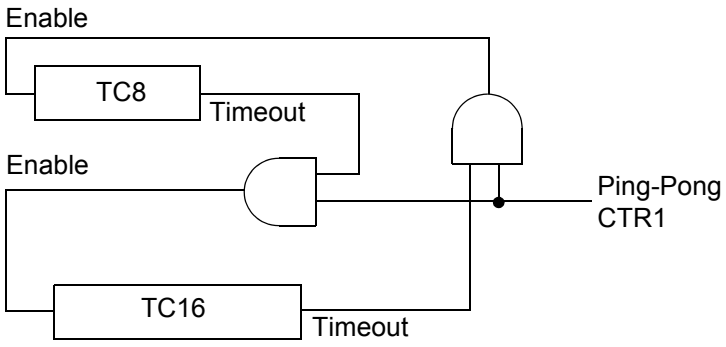


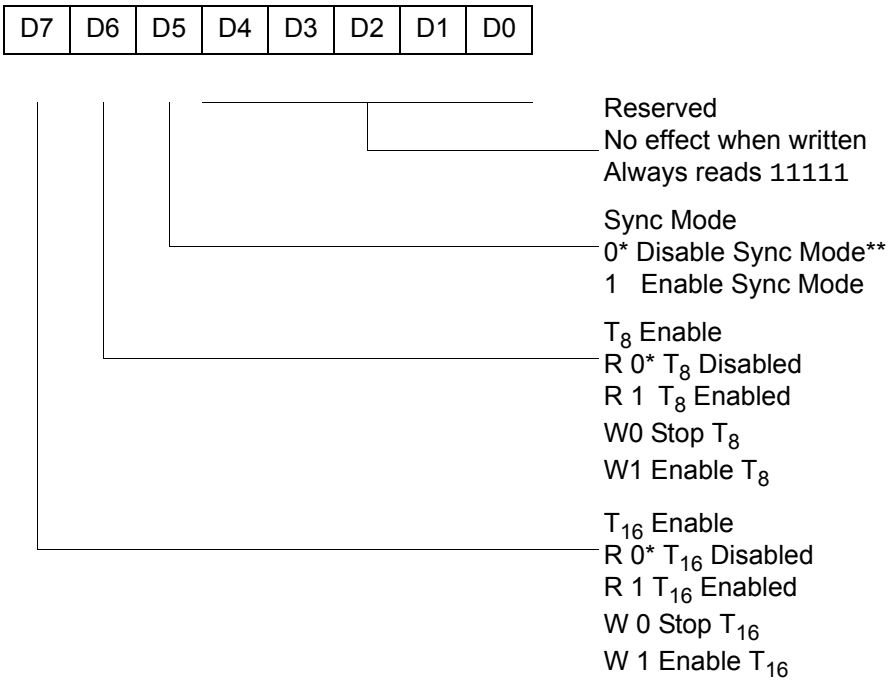
Figure 26. PING-PONG Mode Diagram

Voltage Detection and Flags

The Voltage Detection register (LVD, register 0Ch at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the V_{CC} level is monitored in real time. The HVD Flag (bit 2 of the LVD register) is set only if V_{CC} is higher than $V_{HVD.}$ The LVD Flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD}. When Voltage Detection is enabled, the LVD Flag also triggers IRQ5. The IRQ bit 5 latches the low-voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a Flag only.

Note: *If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt (EI) instruction prior to enabling the voltage detection.*

CTR3(0D)03H

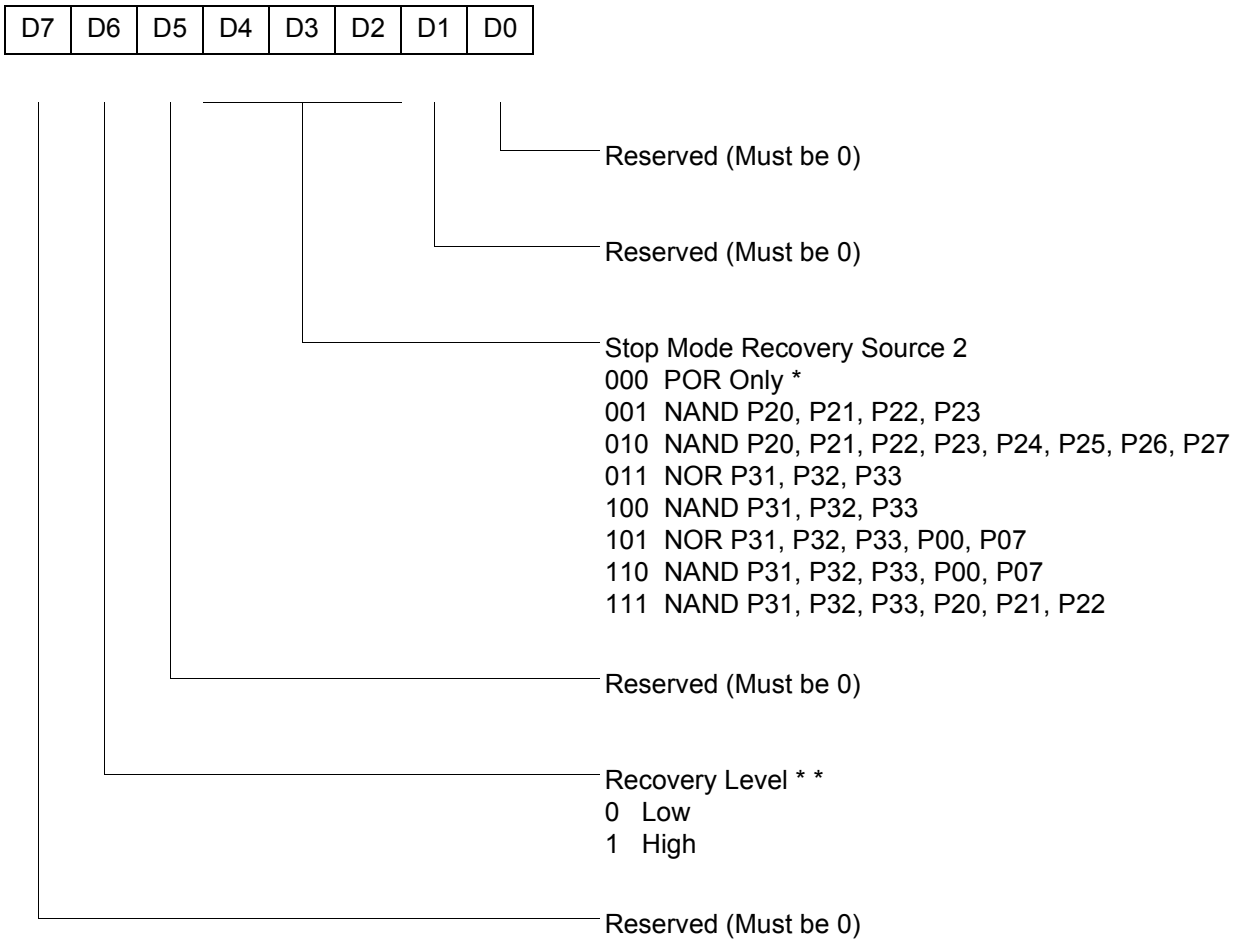


*Default setting after reset.
**Default setting after reset. Not reset with a Stop Mode Recovery.

Figure 40. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)

Note: *If Sync Mode is enabled, the first pulse of T8 carrier is always synchronized with T16 (demodulated signal). It can always provide a full carrier pulse.*

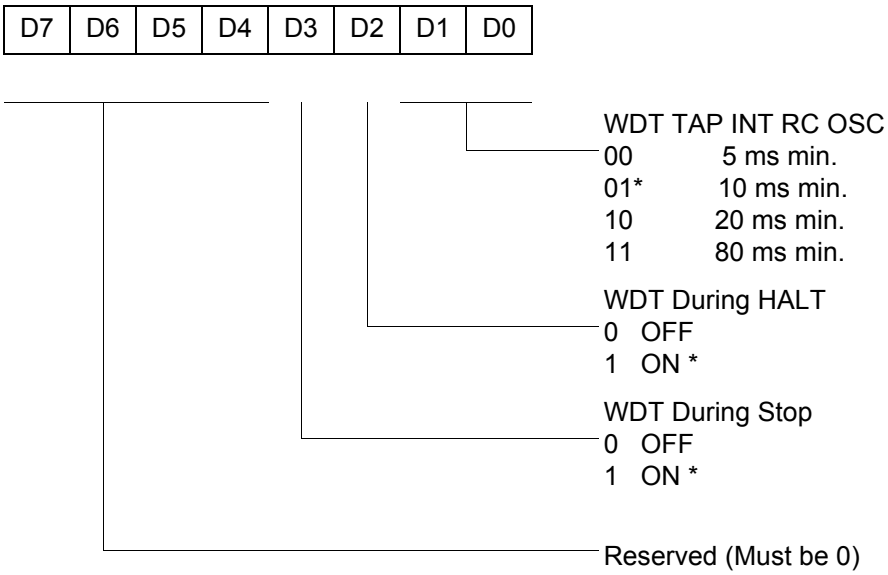
SMR2(0F)0DH



If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.
*Default setting after reset. Not Reset with a Stop Mode Recovery.
* *At the XOR gate input

Figure 44. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)

WDTMR(0F)0FH



*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 45. Watchdog Timer Register ((0F) 0FH: Write Only)

Standard Control Registers

The standard control registers are displayed in Figure 46 through Figure 55 on page 74.

R246 P2M(F6H)

D7	D6	D5	D4	D3	D2	D1	D0

P27–P20 I/O Definition
0 Defines bit as OUTPUT
1 Defines bit as INPUT *

*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 46. Port 2 Mode Register (F6H: Write Only)

R247 P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0

0: Port 2 Open Drain *
1: Port 2 Push-Pull

0= P31, P32 DIGITAL Mode*
1= P31, P32 ANALOG Mode

Reserved (Must be 0)

*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 47. Port 3 Mode Register (F7H: Write Only)

R249 IPR(F9H)

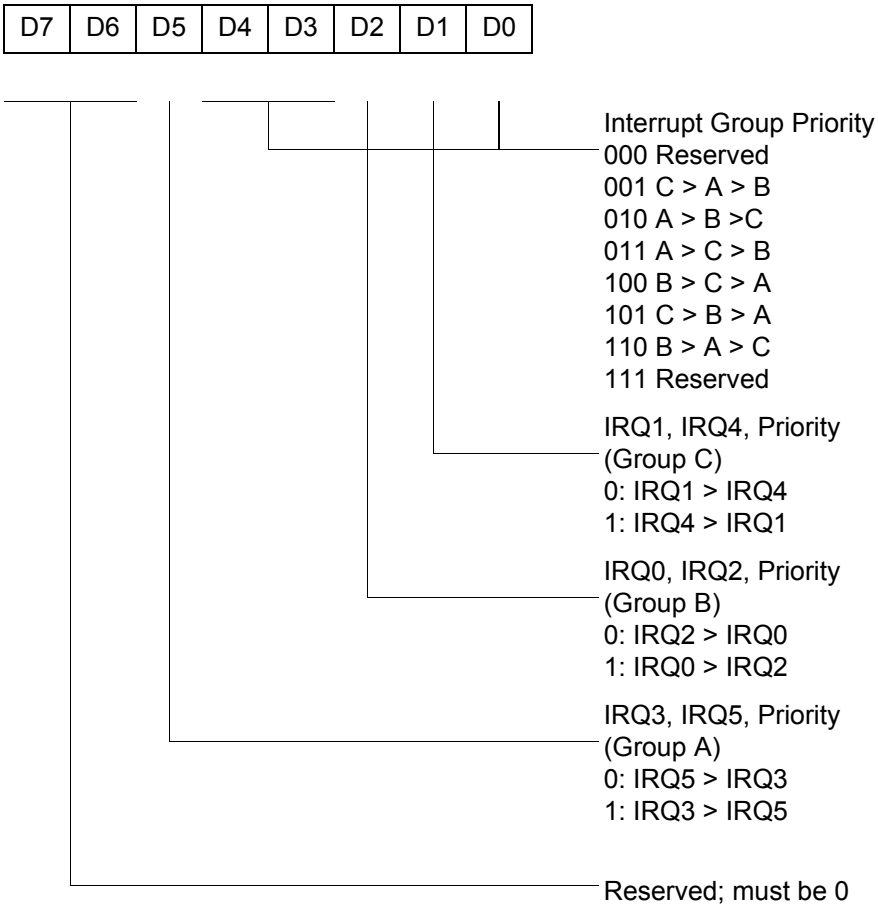


Figure 49. Interrupt Priority Register (F9H: Write Only)

R254 SPH(FEH)

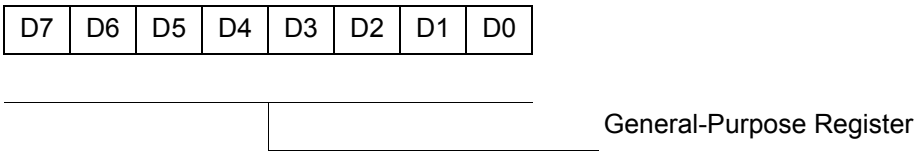


Figure 54. Stack Pointer High (FEH: Read/Write)

R255 SPL(FFH)

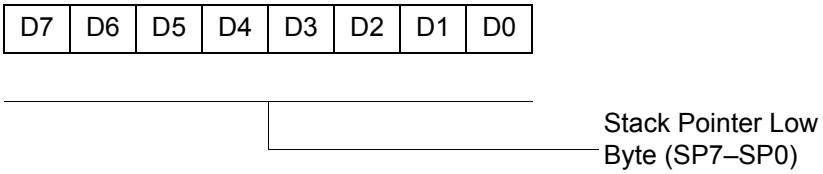


Figure 55. Stack Pointer Low (FFH: Read/Write)

Capacitance

Table 18 lists the capacitances.

Table 18. Capacitance

Parameter	Maximum
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF
T_A = 25 °C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND	

DC Characteristics

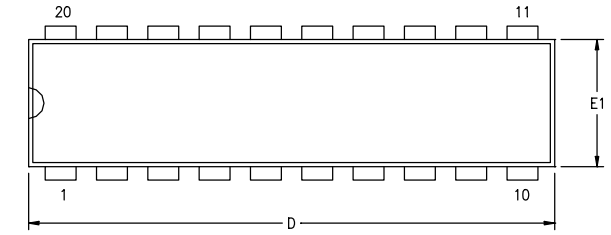
Table 19 describes the DC characteristics.

Table 19. DC Characteristics

			T_A= 0 °C to +70 °C					
Symbol	Parameter	V_{CC}	Min	Typ(7)	Max	Units	Conditions	Notes
V_{CC}	Supply Voltage		2.0		3.6	V	See Notes	5
V_{CH}	Clock Input High Voltage	2.0-3.6	0.8 V_{CC}		V_{CC}+0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-3.6	V_{SS}–0.3		0.4	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-3.6	0.7 V_{CC}		V_{CC}+0.3	V		
V_{IL}	Input Low Voltage	2.0-3.6	V_{SS}–0.3		0.2 V_{CC}	V		
V_{OH1}	Output High Voltage	2.0-3.6	V_{CC}–0.4			V	I_{OH} = –0.5 mA	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-3.6	V_{CC}–0.8			V	I_{OH} = –7 mA	
V_{OL1}	Output Low Voltage	2.0-3.6			0.4	V	I_{OL} = 4.0 mA	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-3.6			0.8	V	I_{OL} = 10 mA	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-3.6			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-3.6	0		V_{CC} -1.75	V		

Packaging

Package information for all versions of Crimzon ZLP32300 is displayed in Figure 58 through Figure 65.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	0.81	.015	.032
A2	3.25	3.68	.128	.145
B	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
e	2.54 BSC		.100 BSC	
eA	7.87	9.14	.310	.360
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

CONTROLLING DIMENSIONS : INCH

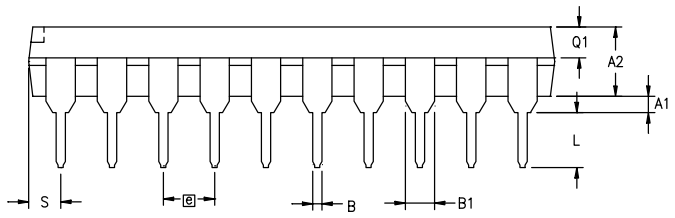


Figure 58. 20-Pin PDIP Package Diagram

Ordering Information

The Crimzon ZLP32300 is available for the following parts:

Device	Part Number	Description
Crimzon ZLP32300	ZLP32300H4832G	48-pin SSOP 32 K OTP
	ZLP32300P4032G	40-pin PDIP 32 K OTP
	ZLP32300H2832G	28-pin SSOP 32 K OTP
	ZLP32300P2832G	28-pin PDIP 32 K OTP
	ZLP32300S2832G	28-pin SOIC 32 K OTP
	ZLP32300H2032G	20-pin SSOP 32 K OTP
	ZLP32300P2032G	20-pin PDIP 32 K OTP
	ZLP32300S2032G	20-pin SOIC 32 K OTP
	ZLP32300H4816G	48-pin SSOP 16 K OTP
	ZLP32300P4016G	40-pin PDIP 16 K OTP
	ZLP32300H2816G	28-pin SSOP 16 K OTP
	ZLP32300P2816G	28-pin PDIP 16 K OTP
	ZLP32300S2816G	28-pin SOIC 16 K OTP
	ZLP32300H2016G	20-pin SSOP 16 K OTP
	ZLP32300P2016G	20-pin PDIP 16 K OTP
	ZLP32300S2016G	20-pin SOIC 16 K OTP
	ZLP32300H4808G	48-pin SSOP 8 K OTP
	ZLP32300P4008G	40-pin PDIP 8 K OTP
	ZLP32300H2808G	28-pin SSOP 8 K OTP
	ZLP32300P2808G	28-pin PDIP 8 K OTP
	ZLP32300S2808G	28-pin SOIC 8 K OTP
	ZLP32300H2008G	20-pin SSOP 8 K OTP

S

T

V

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