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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	·
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlp32300p2016g

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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- EPROM Protection
- WDT enabled at POR

Functional Block Diagram

Figure 1 displays the Crimzon ZLP32300 MCU functional block diagram.



Note: Refer to the specific package for available pins.

Figure 1. Crimzon ZLP32300 MCU Functional Block Diagram

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Figure 2. Counter/Timers Diagram

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Figure 5. 40-Pin PDIP Pin Configuration



40-Pin PDIP No	48-Pin SSOP No	Symbol
32	39	P12
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V _{DD}
31	24, 37, 38	V _{SS}
25	29	Pref1/P30
	48	NC
	6	NC

Table 5. 40- and 48-Pin Configuration (Continued)



open-drain output with output logic as ONE, it is a floating port and reads back as ZERO. The following instruction sets P00-P07 all Low.

AND P0,#%F0

Port 0 (P00–P07)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or opendrain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 01 mode register (P01M). After a hardware reset or Stop Mode Recovery, Port 0 is configured as an input port.

An optional pull-up transistor is available as a OTP option bit on all Port 0 bits with nibble select.

Note: *The Port 0 direction is reset to be input following an SMR.*





Figure 11. Port 3 Counter/Timer Output Configuration

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Comparator Inputs

In ANALOG mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as displayed in Figure 10 on page 15. In DIGITAL mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

Note: Comparators are powered down by entering STOP mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into DIGITAL mode.

Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

RESET (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watchdog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watchdog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the ZLP32300 asserts (Low) the RESET pin, the internal pull-up is disabled. The ZLP32300 does not assert the RESET pin when under VBO.

Note: *The external Reset does not initiate an exit from STOP mode.*



Functional Description

This device incorporates special functions to enhance the Z8 functionality in consumer and battery-operated applications.

Program Memory

This device addresses 32 KB of OTP memory. The first 12 bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts. See Figure 12.

RAM

This device features 256 B of RAM.



Counter/Timer8 High Hold Register—TC8H(D)05h

Field	Id Bit Position Description		Description
T8_Level_HI	[7:0]	R/W	Data

Counter/Timer8 Low Hold Register—TC8L(D)04h

Field	Id Bit Position		eld Bit Position Description		Description
T8_Level_LO	[7:0]	R/W	Data		

CTR0 Counter/Timer8 Control Register—CTR0(D)00h

Table 7 lists and briefly describes the fields for this register.

Table 7. CTR0(D)00h Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6	R/W	0*	Modulo-N
			1	Single Pass
Time_Out	5	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8 _Clock	43	R/W	0 0**	SCLK
			0 1	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	2	R/W	0**	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt
Counter_INT_Mask	1-	R/W	0**	Disable Time-Out Interrupt
			1	Enable Time-Out Interrupt
P34_Out	0	R/W	0*	P34 as Port Output
			1	T8 Output on P34

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.





Figure 17. TRANSMIT Mode Flowchart



* CLR1 and CLR2 enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-High

Figure 36. Resets and WDT

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP mode. A 1 indicates active during Stop. The default is 1.

EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These are listed in Table 16.

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Table 16. EPROM Selectable Options

Port 00–03 Pull-Ups	ON/OFF
Port 04–07 Pull-Ups	ON/OFF
Port 10–13 Pull-Ups	ON/OFF
Port 14–17 Pull-Ups	ON/OFF
Port 20–27 Pull-Ups	ON/OFF
EPROM Protection	ON/OFF
Watchdog Timer at Power-On Reset	ON/OFF

Voltage Brownout/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO} . A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM} , the RAM content is preserved. When the power level is returned to above V_{BO} , the device performs a POR and functions normally.

Low-Voltage Detection

Low-Voltage Detection Register—LVD(D)0Ch

Note: *Voltage detection does not work at STOP mode.*

Field	Bit Position			Description
LVD	76543			Reserved No Effect
	2	R	1 0*	HVD Flag set HVD Flag reset
	1-	R	1 0*	LVD Flag set LVD Flag reset
	0	R/W	1 0*	Enable VD Disable VD
*Default a	fter POR			

Note: Do not modify register P01M while checking a low-voltage condition. Switching noise of both Ports 0 and 1 together might trigger the LVD Flag.



CTR3(0D)03H



**Default setting after reset. Not reset with a Stop Mode Recovery.

Figure 40. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)

Note: If Sync Mode is enabled, the first pulse of T8 carrier is always synchronized with T16 (demodulated signal). It can always provide a full carrier pulse.

SMR2(0F)0DH D7 D6 D5 D4 D3 D2 D1 D0 Reserved (Must be 0) Reserved (Must be 0) Stop Mode Recovery Source 2 000 POR Only * 001 NAND P20, P21, P22, P23 010 NAND P20, P21, P22, P23, P24, P25, P26, P27 011 NOR P31, P32, P33 100 NAND P31, P32, P33 101 NOR P31, P32, P33, P00, P07 110 NAND P31, P32, P33, P00, P07 111 NAND P31, P32, P33, P20, P21, P22 Reserved (Must be 0) Recovery Level * * 0 Low 1 High Reserved (Must be 0)

If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.

*Default setting after reset. Not Reset with a Stop Mode Recovery.

* *At the XOR gate input

Figure 44. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)

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R250 IRQ(FAH)



Figure 50. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)



*Default setting after reset

* *Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 51. Interrupt Mask Register (FBH: Read/Write)

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Packaging

Package information for all versions of Crimzon ZLP32300 is displayed in Figure 58 through Figure 65.



SYMBOL	MILLIMETER		INC	н
STWDOL	MIN	MAX	MIN	MAX
A1	0.38	0.81	.015	.032
A2	3.25	3.68	.128	.145
В	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
С	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
e	2.54 BSC		.100	BSC
eA	7.87	9.14	.310	.360
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

F

L___



CONTROLLING	DIMENSIONS	:	INCH







Note: ZiLOG supplies both options for production. Component layout PCB design should cover bigger option 01.



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Device	Part Number	Description
	ZLP32300P2008G	20-pin PDIP 8 K OTP
	ZLP32300S2008G	20-pin SOIC 8 K OTP
	ZLP32300H4804G	48-pin SSOP 4 K OTP
	ZLP32300P4004G	40-pin PDIP 4 K OTP
	ZLP32300H2804G	28-pin SSOP 4 K OTP
	ZLP32300P2804G	28-pin PDIP 4 K OTP
	ZLP32300S2804G	28-pin SOIC 4 K OTP
	ZLP32300H2004G	20-pin SSOP 4 K OTP
	ZLP32300P2004G	20-pin PDIP 4 K OTP
	ZLP32300S2004G	20-pin SOIC 4 K OTP
	ZLP323ICE01ZAC*	40-PDIP/48-SSOP Accessory Kit
	Note: *ZLP323ICE01ZAC h ZCRMZNICE02ZAC	as been replaced by an improved version, G.
	ZLP128ICE01ZEMG	In-Circuit Emulator
	Note: *ZLP128ICE01ZEMG ZCRMZNICE01ZEM	has been replaced by an improved version, G.
	ZCRMZNICE01ZEMG	Crimzon In-Circuit Emulator
	ZCRMZN00100KITG	Crimzon In-Circuit Emulator Development Kit
	ZCRMZNICE01ZACG	20-Pin Accessory Kit
	ZCRMZNICE02ZACG	40/48-Pin Accessory Kit
Notos		

Not

1. Replace C with G for Lead-Free Packaging.

2. Contact <u>www.zilog.com</u> for the die form.

For fast results, contact your local Zilog[®] sales office for assistance in ordering the part(s) desired.



Part Number Description

Zilog[®] part numbers consist of a number of components, as shown below. ZLP32300H2832G is a Crimzon ZLP32300 OTP product in a 28-pin SSOP package, with 32 KB of OTP and built with lead-free solder.

