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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlp32300p2032c

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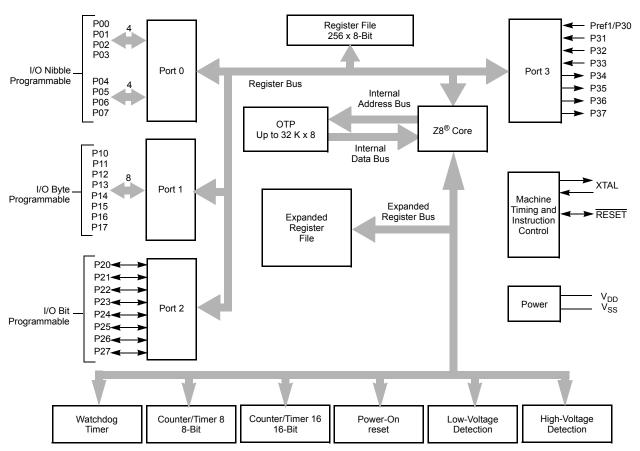
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- EPROM Protection
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Functional Block Diagram

Figure 1 displays the Crimzon ZLP32300 MCU functional block diagram.



Note: Refer to the specific package for available pins.

Figure 1. Crimzon ZLP32300 MCU Functional Block Diagram

PS020823-0208 Architectural Overview

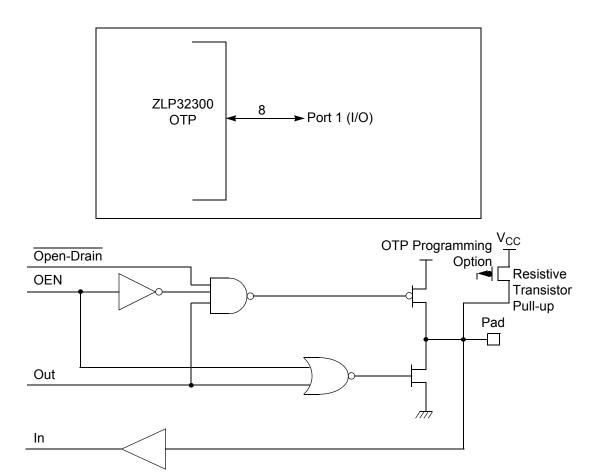


Figure 8. Port 1 Configuration

Port 2 (P27-P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 9). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A EPROM option bit is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in DEMODULATION mode.

PS020823-0208 Pin Description

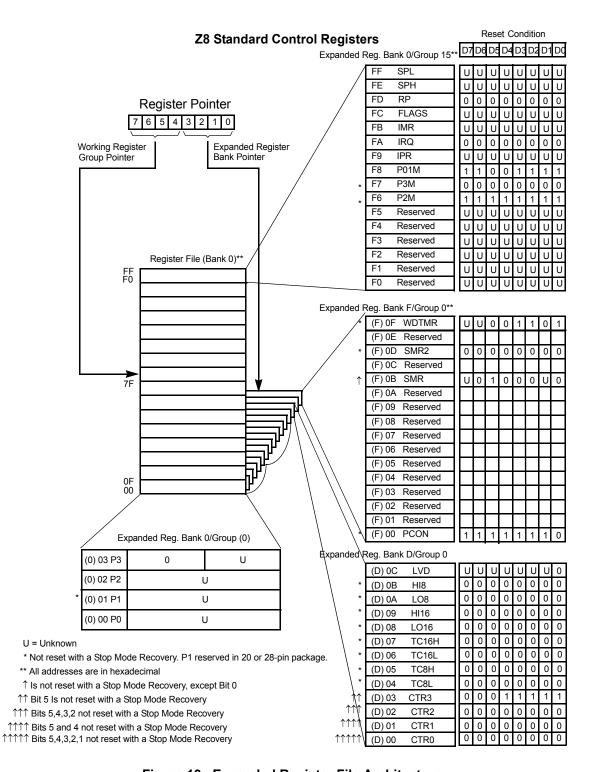


Figure 13. Expanded Register File Architecture



```
R1, 2
LD
                                                 ; CTR2→CTR1
LD
                        RP, #0Dh
                                                 ; Select ERF D
for access to bank D
                                                 ; (working
register group 0)
                                                 ; Select
                        RP, #7Dh
expanded register bank D and working
                                                 ; register
group 7 of bank 0 for access.
                        71h, 2
; CTRL2→register 71h
                        R1, 2
; CTRL2→register 71h
```

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 7 on page 27) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (see Figure 15). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note:

Working register group E0–EF can only be accessed through working registers and indirect addressing modes.

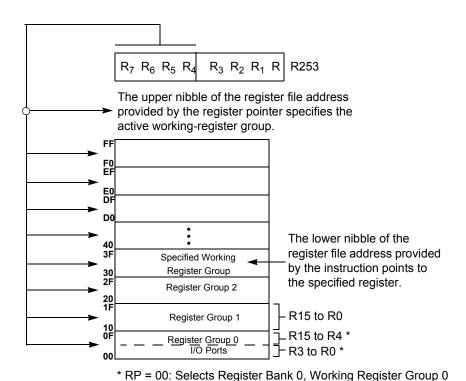


Figure 15. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

Timers

T8_Capture_HI—HI8(D)0Bh

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description		
T8_Capture_HI	[7:0]	R/W	Captured Data—No Effect		

Counter/Timer8 High Hold Register—TC8H(D)05h

Field	Bit Position		Description
T8_Level_HI	[7:0]	R/W	Data

Counter/Timer8 Low Hold Register—TC8L(D)04h

Field	Bit Position	Description		
T8_Level_LO	[7:0]	R/W	Data	

CTR0 Counter/Timer8 Control Register—CTR0(D)00h

Table 7 lists and briefly describes the fields for this register.

Table 7. CTR0(D)00h Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7	R/W	0* 1 0 1	Counter Disabled Counter Enabled Stop Counter Enable Counter
Single/Modulo-N	-6	R/W	0* 1	Modulo-N Single Pass
Time_Out	5	R/W	0** 1 0 1	No Counter Time-Out Counter Time-Out Occurred No Effect Reset Flag to 0
T8 _Clock	43	R/W	0 0** 0 1 1 0 1 1	SCLK SCLK/2 SCLK/4 SCLK/8
Capture_INT_Mask	2	R/W	0** 1	Disable Data Capture Interrupt Enable Data Capture Interrupt
Counter_INT_Mask	1-	R/W	0** 1	Disable Time-Out Interrupt Enable Time-Out Interrupt
P34_Out	0	R/W	0* 1	P34 as Port Output T8 Output on P34

^{*}Indicates the value upon Power-On Reset.

^{**}Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.



Table 9. CTR2(D)02h: Counter/Timer16 Control Register (Continued)

Field	Bit Position		Value	Description SCLK		
T16 _Clock	43	R/W	00**			
			01	SCLK/2		
			10	SCLK/4		
			11	SCLK/8		
Capture_INT_Mask	2	R/W	0**	Disable Data Capture Int.		
			1	Enable Data Capture Int.		
Counter_INT_Mask	1-	R/W	0	Disable Timeout Int.		
			1	Enable Timeout Int.		
P35_Out	0	R/W	0*	P35 as Port Output		
_			1	T16 Output on P35		

^{*}Indicates the value upon Power-On Reset.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In TRANSMIT mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.

In DEMODULATION mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see T16 DEMODULATION Mode on page 41.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

T16 Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture INT Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

Set this bit to allow an interrupt when T16 times out.

^{**}Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.



Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur, see Figure 19 and Figure 20.

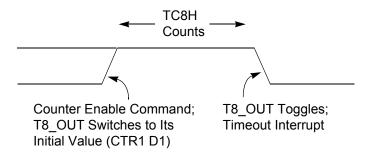


Figure 19. T8_OUT in SINGLE-PASS Mode

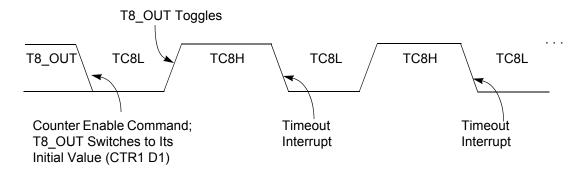


Figure 20. T8_OUT in MODULO-N Mode

T8 DEMODULATION Mode

You must program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the time-out status bit (CTR0, D5) is set, and an

T16 TRANSMIT Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NOR-MAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set, see Figure 23.

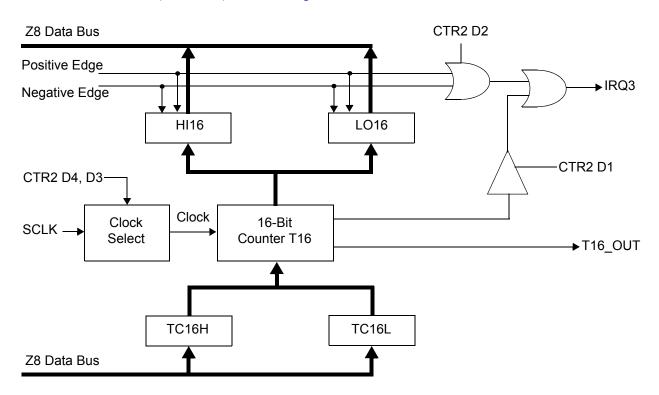


Figure 23. 16-Bit Counter/Timer Circuits

Note: Global interrupts override this function as described in Interrupts on page 43.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 24). If it is in MODULO-N mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 25).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.



Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to ffffh to ffffh. Transition from 0 to ffffh is not a timeout condition.

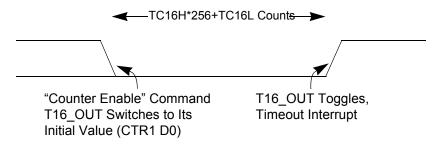


Figure 24. T16_OUT in SINGLE-PASS Mode

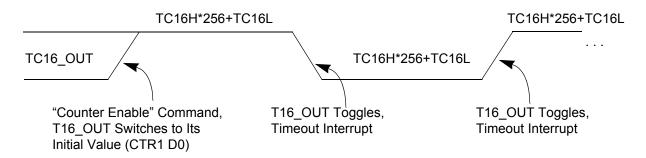


Figure 25. T16_OUT in MODULO-N Mode

T16 DEMODULATION Mode

You must program TC16L and TC16H to FFh. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFh and starts again.

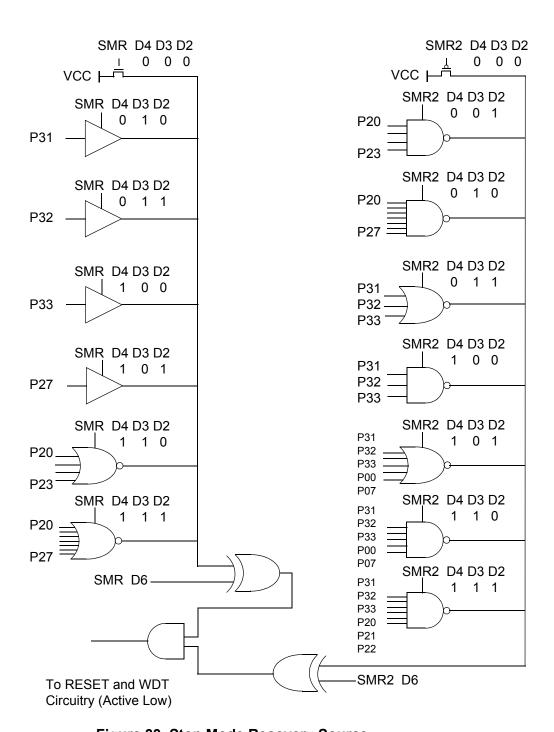


Figure 33. Stop Mode Recovery Source

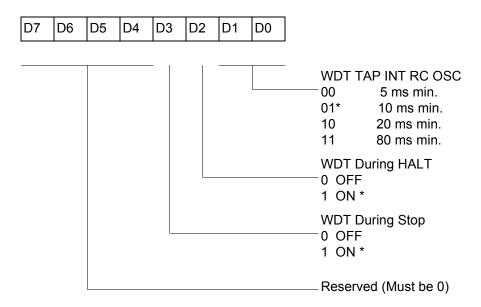
Watchdog Timer Mode

Watchdog Timer Mode Register (WDTMR)

The Watchdog Timer is a retriggerable one-shot timer that resets the $Z8^{\textcircled{R}}$ if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) Flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum time-out period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (see Figure 35). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-on reset, Watchdog Reset, or a Stop Mode Recovery (see Figure 34). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 35.

WDTMR(0F)0Fh



^{*}Default setting after reset

Figure 35. Watchdog Timer Mode Register (Write Only)

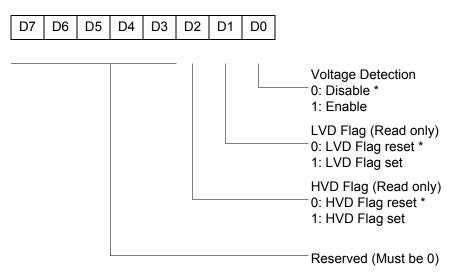
Voltage Detection and Flags

The Voltage Detection register (LVD, register 0Ch at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the V_{CC} level is monitored in real time. The HVD Flag (bit 2 of the LVD register) is set only if V_{CC} is higher than V_{HVD} . The LVD Flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD} . When Voltage Detection is enabled, the LVD Flag also triggers IRQ5. The IRQ bit 5 latches the low-voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a Flag only.

Note:

If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt (EI) instruction prior to enabling the voltage detection.

LVD(0D)0CH



^{*}Default setting after reset.

Figure 41. Voltage Detection Register

Note: Do not modify register P01M while checking a low-voltage condition. Switching noise of both Ports 0 and 1 together might trigger the LVD Flag.

D7 D6 D5 D4 D3 D2 D1 D0 Reserved (Must be 0) Reserved (Must be 0) Stop Mode Recovery Source 2 000 POR Only * 001 NAND P20, P21, P22, P23 010 NAND P20, P21, P22, P23, P24, P25, P26, P27 011 NOR P31, P32, P33 100 NAND P31, P32, P33 101 NOR P31, P32, P33, P00, P07 110 NAND P31, P32, P33, P00, P07 111 NAND P31, P32, P33, P20, P21, P22 Reserved (Must be 0) Recovery Level * * 0 Low 1 High Reserved (Must be 0)

If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.

SMR2(0F)0DH

Figure 44. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)

^{*}Default setting after reset. Not Reset with a Stop Mode Recovery.

^{* *}At the XOR gate input

Table 20. AC Characteristics

		T _A =0 °C to +70 °C 8.0 MHz					Watchdog Timer Mode	
No	Symbol	Parameter	V _{CC}	Minimum	Maximum	Units	Notes	Register (D1, D0)
1	ТрС	Input Clock Period	2.0-3.6	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1	
3	TwC	Input Clock Width	2.0-3.6	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0-3.6	3ТрС			1	
6	TpTin	Timer Input Period	2.0-3.6	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0-3.6		100	ns	1	
8	TwlL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2	
9	TwlH	Interrupt Request Input High Time	2.0-3.6	5TpC			1, 2	
10	Twsm	Stop Mode Recovery Width Spec	2.0-3.6	12		ns	3	
		•		10TpC			4	
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4	
12	Twdt	Watchdog Timer Delay Time	2.0–3.6 2.0–3.6 2.0–3.6 2.0–3.6	5 10 20 80		ms ms ms ms		0, 0 0, 1 1, 0 1, 1
13	T _{POR}	Power-on reset	2.0–3.6	2.5	10	ms		

Notes

- 1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0. 2. Interrupt request through Port 3 (P33–P31).
- 3. SMR-D5 = 1.
- 4. SMR-D5 = 0.

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