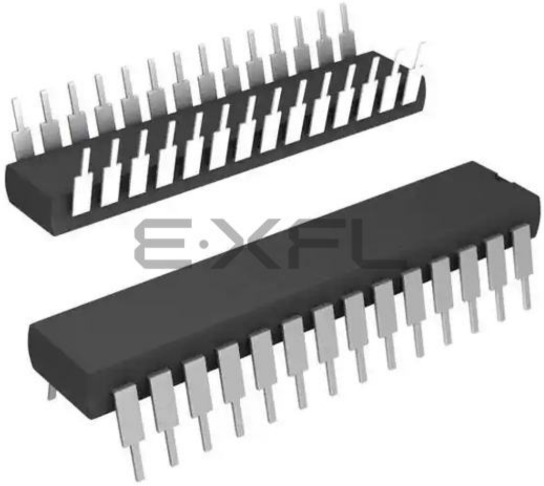

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlp32300p2832c

Revision History

Each instance in the Revision History table reflects a change to this document from its previous revision. For more details, refer to the corresponding pages or appropriate link in the table.

Date	Revision Level	Description	Page Number
February 2008	23	Updated Ordering Information section.	87
January 2008	22	Updated Ordering Information section.	87
July 2007	21	Updated Disclaimer section and implemented style guide.	All
February 2007	20	Updated Low-Voltage Detection.	58
May 2006	19	Updated Figure 33 with pin P22 in SMR block input.	52
December 2005	18	Updated Clock and Input/Output Ports sections.	15 and 51

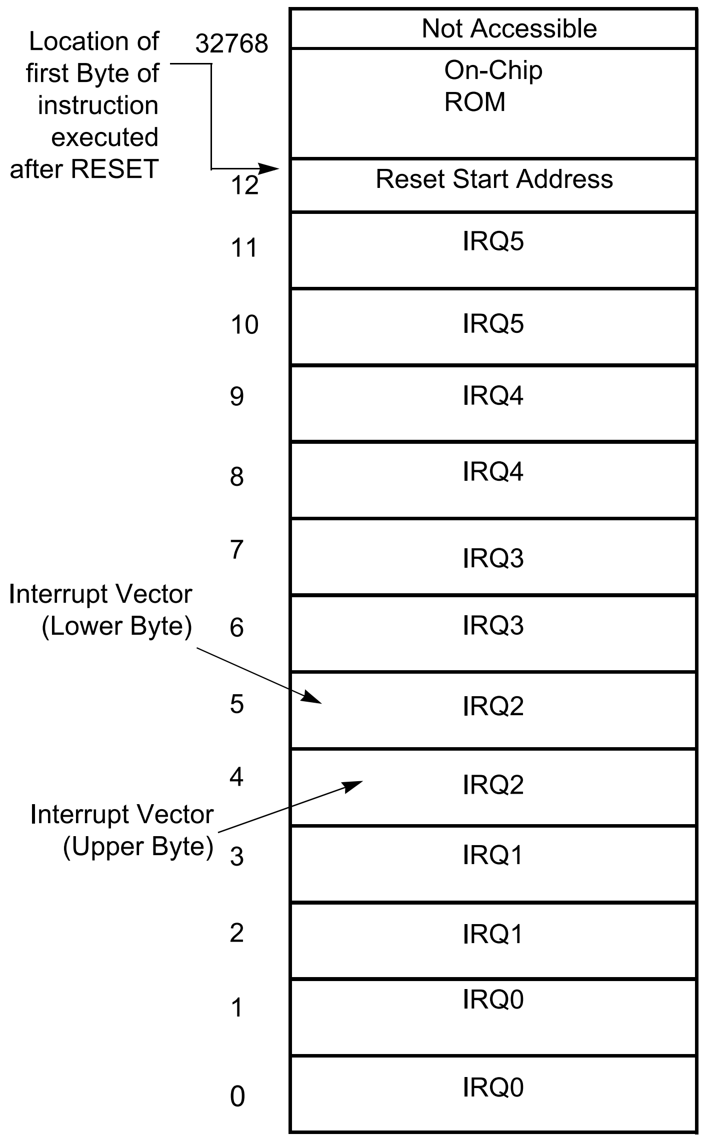


Figure 12. Program Memory Map (32 K OTP)

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8 register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the ERF (Expanded Register File). Bits 7–4 of

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.

Caution: *Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers. The first clock of T8 might not have complete clock width and can occur any time when enabled.*

Note: *Ensure to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (DEMODULATION mode) when using the OR or AND commands. These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.*

T8 Clock

These bits define the frequency of the input signal to T8.

Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in DEMODULATION mode.

Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

T8 and T16 Common Functions—CTR1(0D)01h

This register controls the functions in common with the T8 and T16.

Table 8 lists and briefly describes the fields for this register.

Table 8. CTR1(0D)01h T8 and T16 Common Functions

Field	Bit Position		Value	Description
Mode	7 - - - - - - -	R/W	0*	TRANSMIT Mode
			1	DEMODULATION Mode
P36_Out/	- 6 - - - - - -	R/W		TRANSMIT Mode
Demodulator_Input			0*	Port Output
			1	T8/T16 Output
				DEMODULATION Mode
			0*	P31
			1	P20
T8/T16_Logic/	- - 5 4 - - - -	R/W		TRANSMIT Mode
Edge _Detect			00**	AND
			01	OR
			10	NOR
			11	NAND
				DEMODULATION Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved
Transmit_Submode/	- - - - 3 2 - -	R/W		TRANSMIT Mode
Glitch_Filter			00*	Normal Operation
			01	PING-PONG Mode
			10	T16_Out = 0
			11	T16_Out = 1
				DEMODULATION Mode
			00*	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/	- - - - - - 1 -			TRANSMIT Mode
Rising Edge		R/W	0*	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				DEMODULATION Mode
		R	0*	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Caution: *Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.*

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur, see Figure 19 and Figure 20.

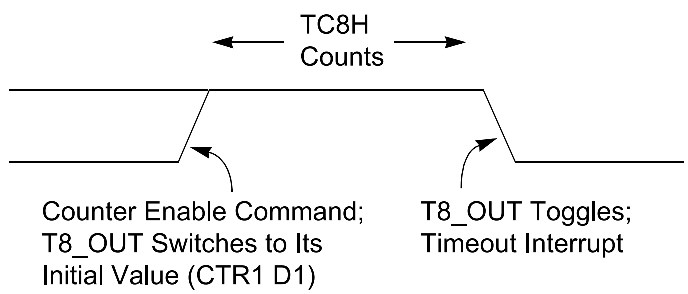


Figure 19. T8_OUT in SINGLE-PASS Mode

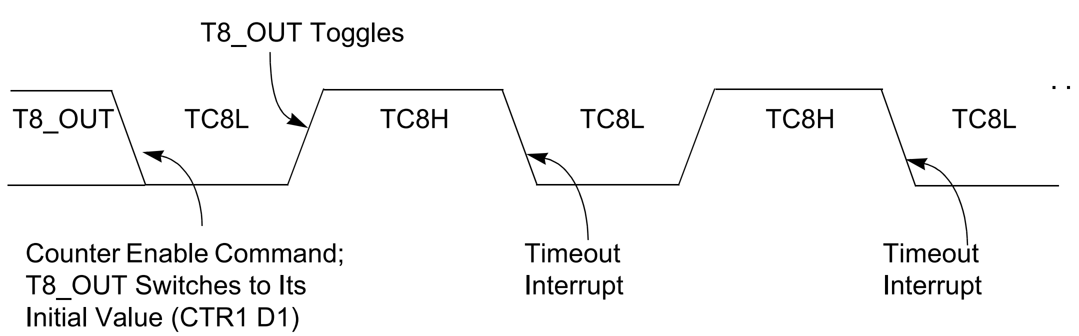


Figure 20. T8_OUT in MODULO-N Mode

T8 DEMODULATION Mode

You must program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the time-out status bit (CTR0, D5) is set, and an

Table 11. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T_{IN}	4,5	External (P31), Rising, Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal
IRQ5	LVD	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All Crimzon ZLP32300 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 12.

Table 12. IRQ Register

IRQ		Interrupt Edge	
D7	**D6**	**IRQ2 (P31)**	**IRQ0 (P32)**
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Note: F = Falling Edge; R = Rising Edge

For both resonator and crystal oscillator, the oscillation ground must go directly to the ground pin of the microcontroller. The oscillation ground must use the shortest distance from the microcontroller ground pin and it must be isolated from other connections.

Power Management

Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset timer function. The POR time allows V_{DD} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from V_{BO} Standby
- Stop Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop Mode Register determines whether the POR timer is bypassed after Stop Mode Recovery (typical for external clock).

HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

STOP Mode

This instruction turns OFF the internal clock and external crystal oscillation, reducing the standby current to 10 µA or less. STOP mode is terminated only by a reset, such as WDT time-out, POR or SMR. This condition causes the processor to restart the application program at address `000Ch`. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = `FFh`) immediately before the appropriate sleep instruction, as follows:

```
FF          NOP         ; clear the pipeline
6F          STOP        ; enter Stop Mode
```

or

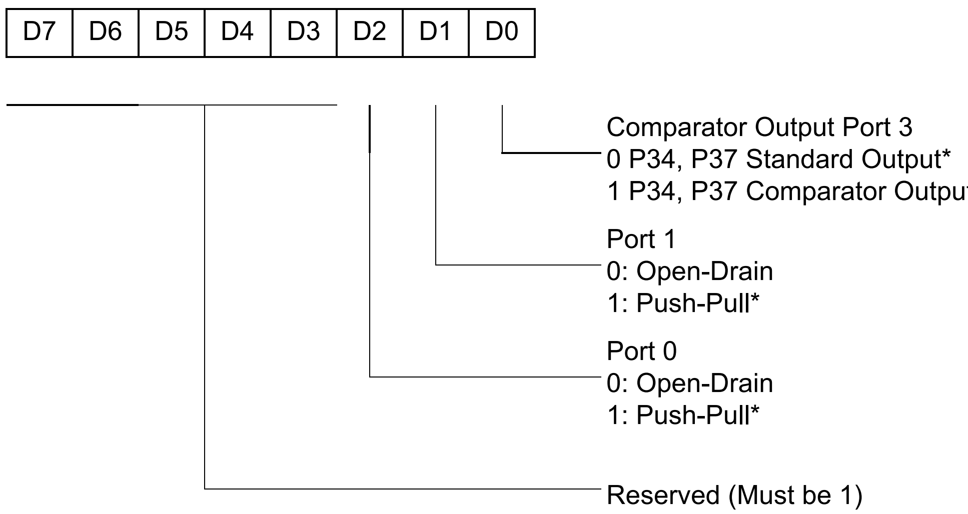
```
FF          NOP         ; clear the pipeline
7F          HALT        ; enter HALT Mode
```

Port Configuration

Port Configuration Register

The Port Configuration (PCON) register (see Figure 30) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

PCON(FH)00h



* Default setting after reset

Figure 30. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

Port 1 Output Mode (D1)

Bit 1 controls the output mode of Port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Port 0 Output Mode (D2)

Bit 2 controls the output mode of Port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Table 14. Stop Mode Recovery Source

SMR:432			Operation
D4	**D3**	**D2**	**Description of Action**
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Note: *Any Port 2 bit defined as an output drives the corresponding input to the default state. For example, if the NOR of P23-P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23-P21) form the NOR equation. This condition allows the remaining inputs to control the AND/OR function, refer to SMR2 register* on page 54 *for other recover sources.*

Stop Mode Recovery Delay Select (D5)

This bit, if low, disables the T_{POR} delay after Stop Mode Recovery. The default configuration of this bit is 1. If the 'fast' wake up is selected, the Stop Mode Recovery source must be kept active for at least 10 TpC.

Note: *This bit must be set to 1 if a crystal or resonator clock source is used. The T_{POR} delay allows the clock source to stabilize before executing instructions.*

Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Crimzon ZLP32300 from STOP mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from STOP mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery.

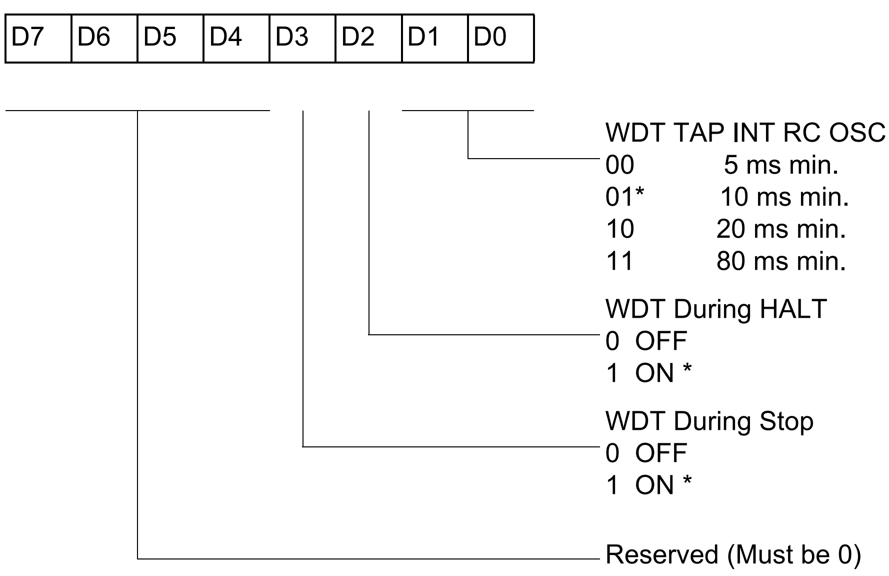
Watchdog Timer Mode

Watchdog Timer Mode Register (WDTMR)

The Watchdog Timer is a retriggerable one-shot timer that resets the Z8® if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) Flags.

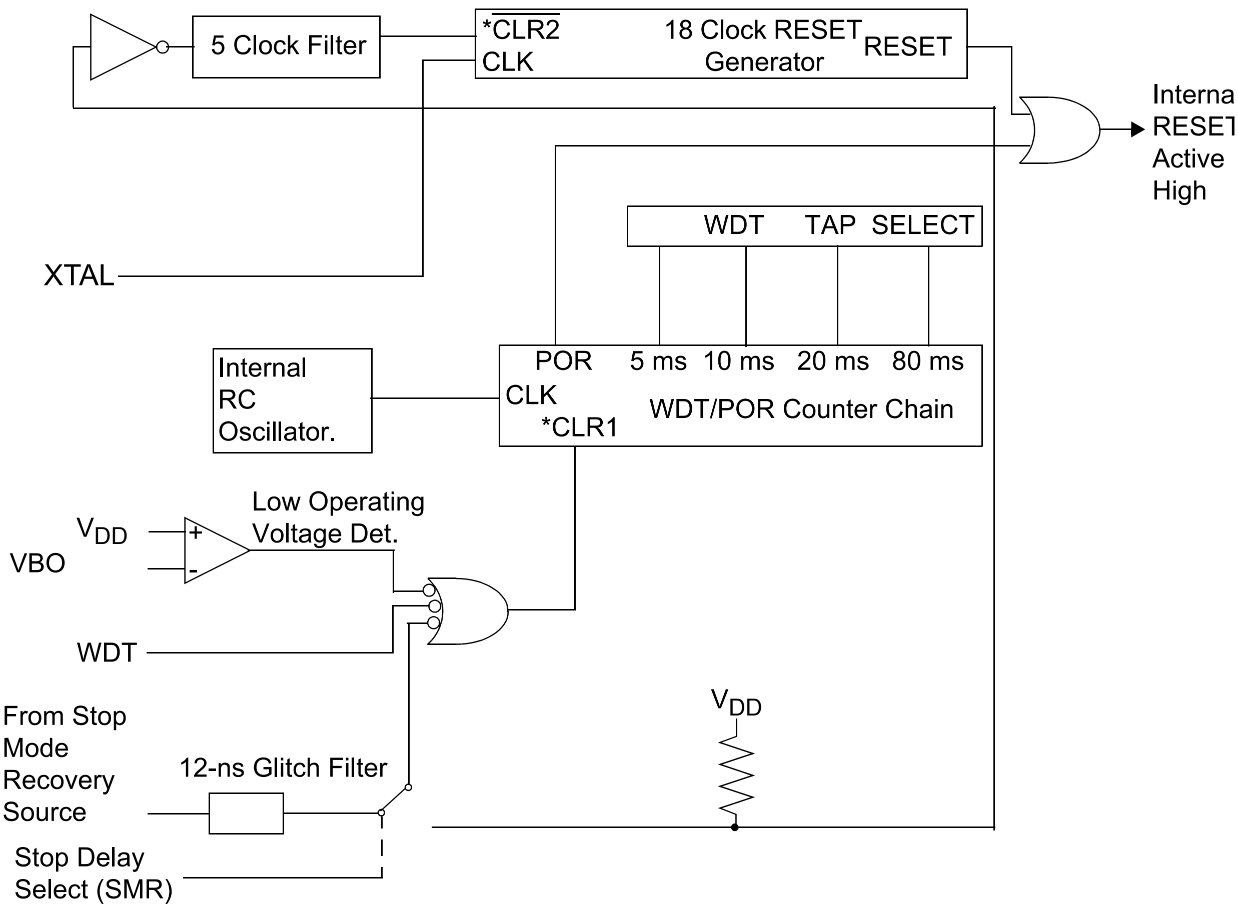
The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum time-out period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (see Figure 35). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-on reset, Watchdog Reset, or a Stop Mode Recovery (see Figure 34). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location `0Fh`. It is organized as shown in Figure 35.

WDTMR(0F)0Fh



*Default setting after reset

Figure 35. Watchdog Timer Mode Register (Write Only)



* CLR1 and CLR2 enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-High

Figure 36. Resets and WDT

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP mode. A 1 indicates active during Stop. The default is 1.

EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These are listed in Table 16.

Table 16. EPROM Selectable Options

Port 00–03 Pull-Ups	ON/OFF
Port 04–07 Pull-Ups	ON/OFF
Port 10–13 Pull-Ups	ON/OFF
Port 14–17 Pull-Ups	ON/OFF
Port 20–27 Pull-Ups	ON/OFF
EPROM Protection	ON/OFF
Watchdog Timer at Power-On Reset	ON/OFF

Voltage Brownout/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO}. A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM}, the RAM content is preserved. When the power level is returned to above V_{BO}, the device performs a POR and functions normally.

Low-Voltage Detection

Low-Voltage Detection Register—LVD(D)0Ch

Note: *Voltage detection does not work at STOP mode.*

Field	Bit Position			Description
LVD	76543---			Reserved No Effect
	-----2--	R	1 0*	HVD Flag set HVD Flag reset
	------1-	R	1 0*	LVD Flag set LVD Flag reset
	-------0	R/W	1 0*	Enable VD Disable VD
*Default after POR				

Note: *Do not modify register P01M while checking a low-voltage condition. Switching noise of both Ports 0 and 1 together might trigger the LVD Flag.*

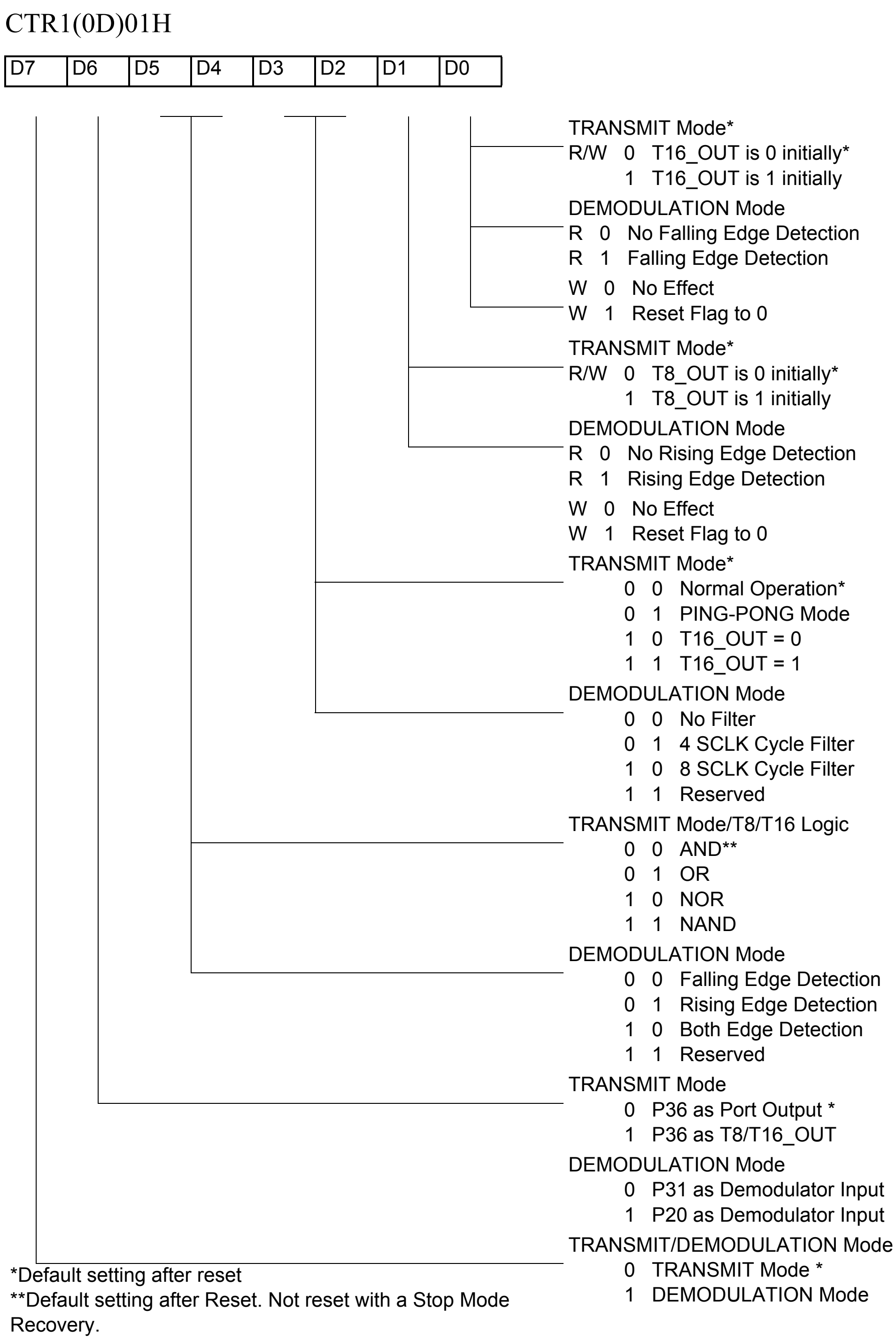
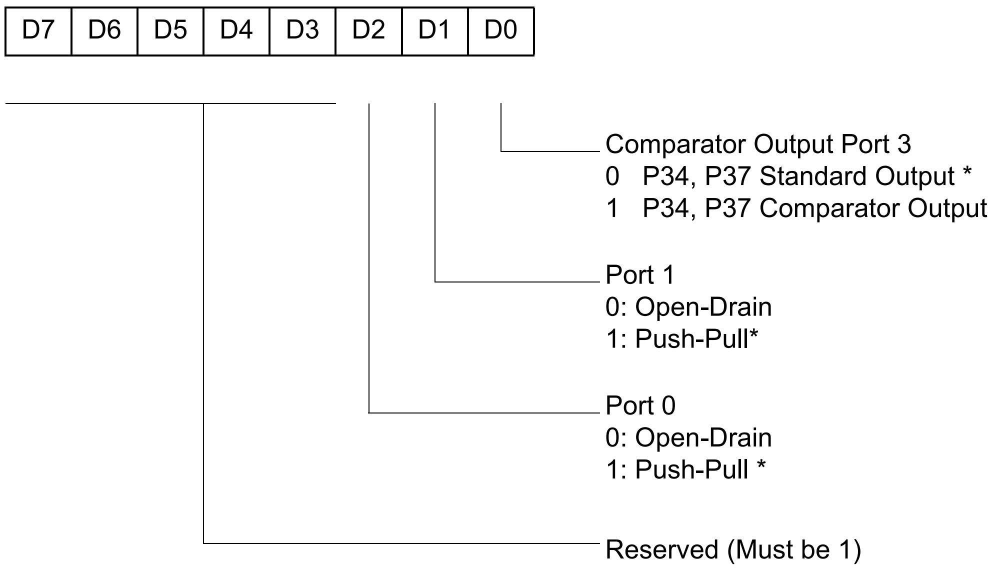


Figure 38. T8 and T16 Common Control Functions ((0D)01H: Read/Write)

Expanded Register File Control Registers (0F)

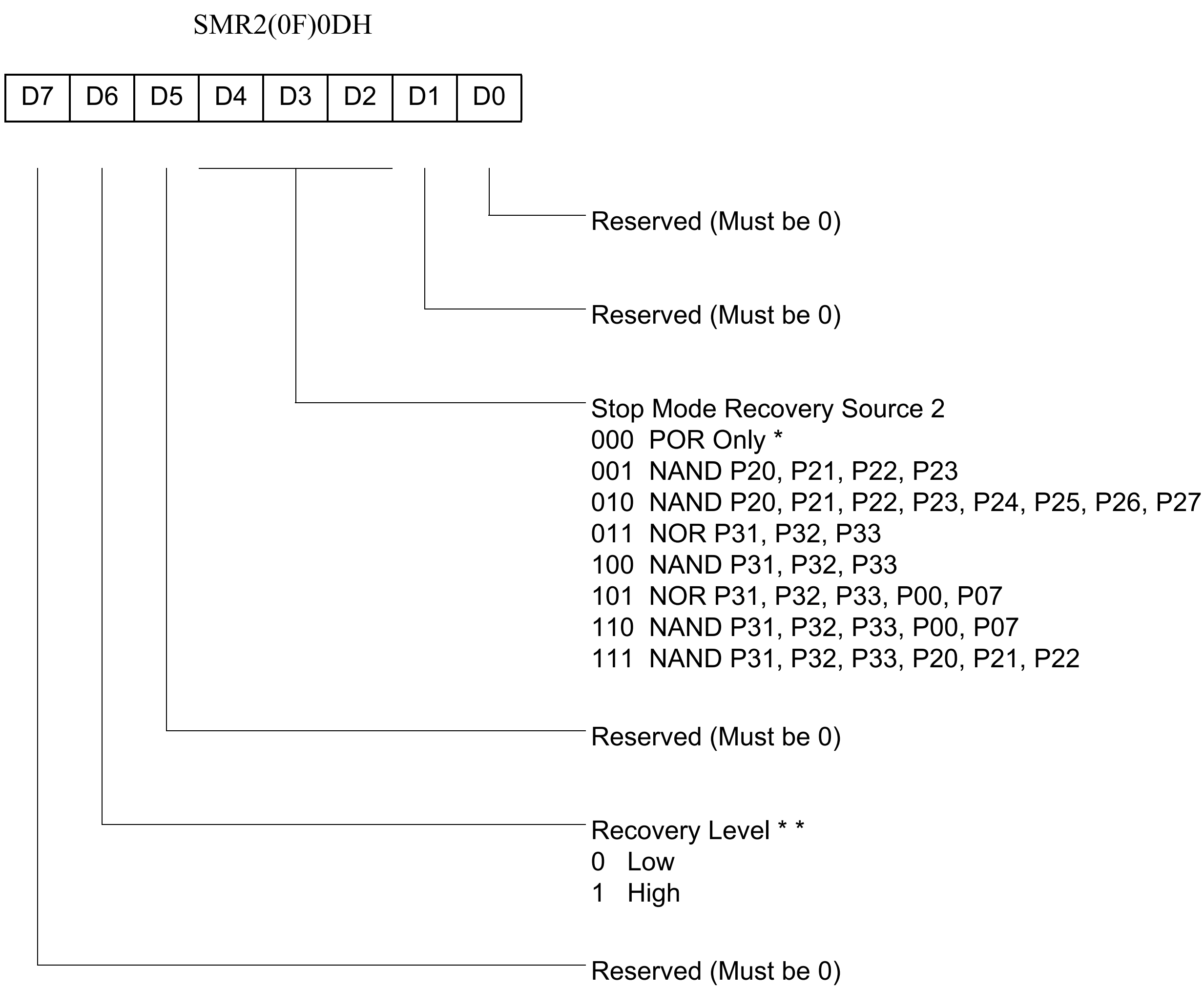
The expanded register file control registers (0F) are displayed in Figure 42 through Figure 55 on page 74.

PCON(0F)00H



*Default setting after reset

Figure 42. Port Configuration Register (PCON)(0F)00H: Write Only)



If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.
*Default setting after reset. Not Reset with a Stop Mode Recovery.
* *At the XOR gate input

Figure 44. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)

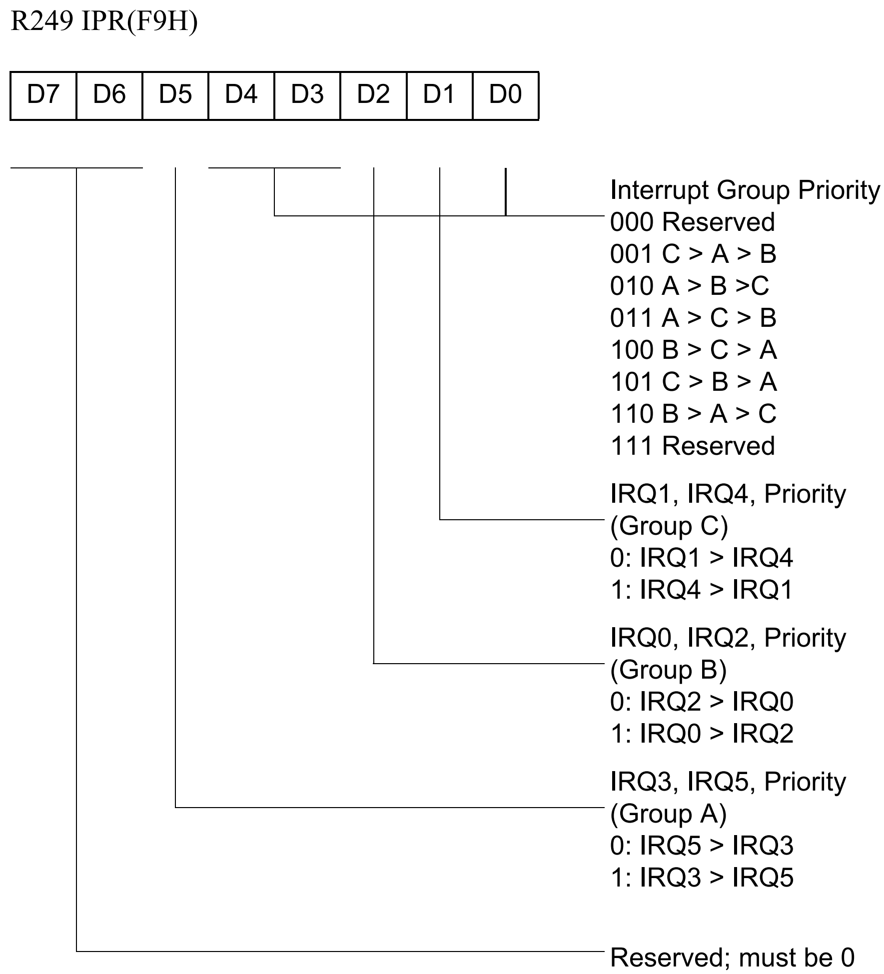


Figure 49. Interrupt Priority Register (F9H: Write Only)

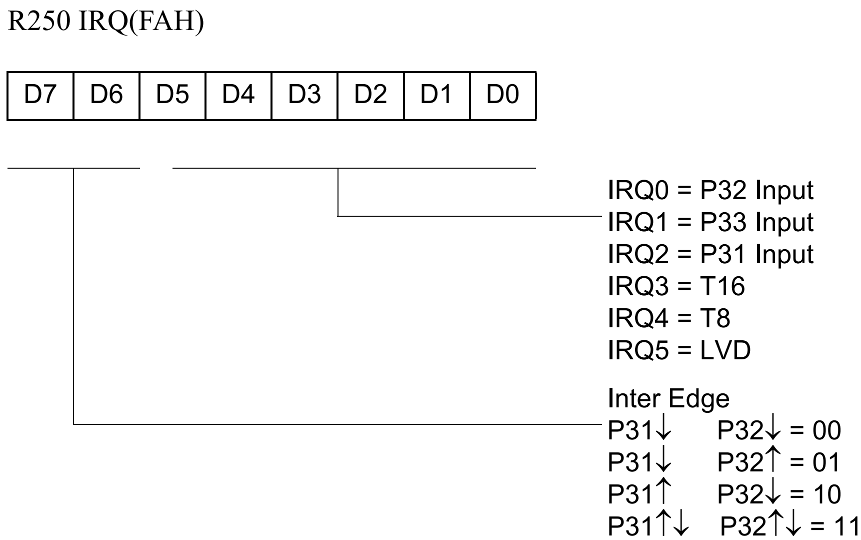
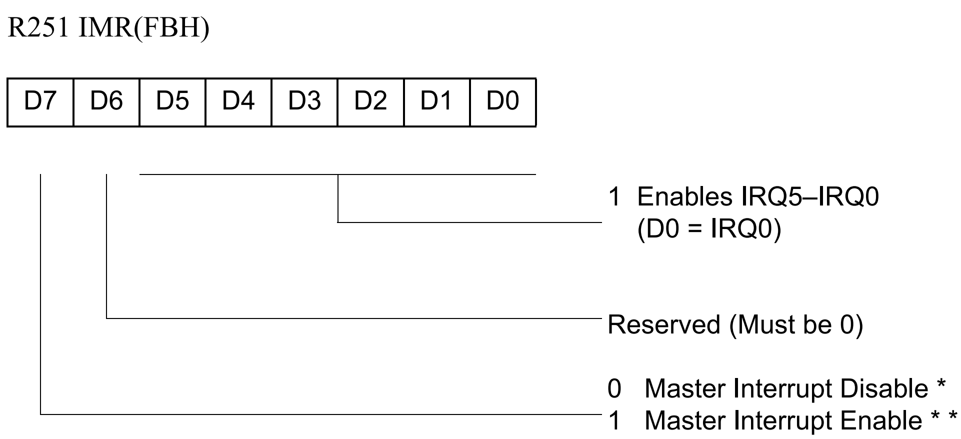


Figure 50. Interrupt Request Register (FAH: Read/Write)



*Default setting after reset
* *Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 51. Interrupt Mask Register (FBH: Read/Write)

R252 Flags(FCH)

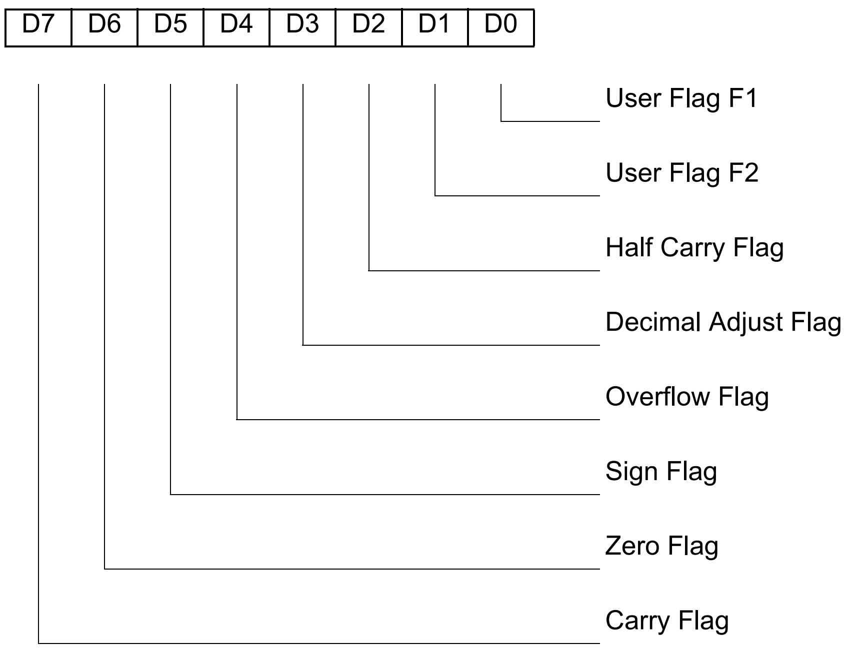
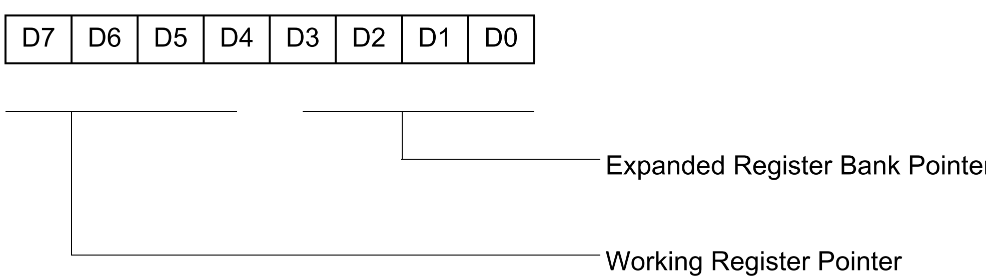


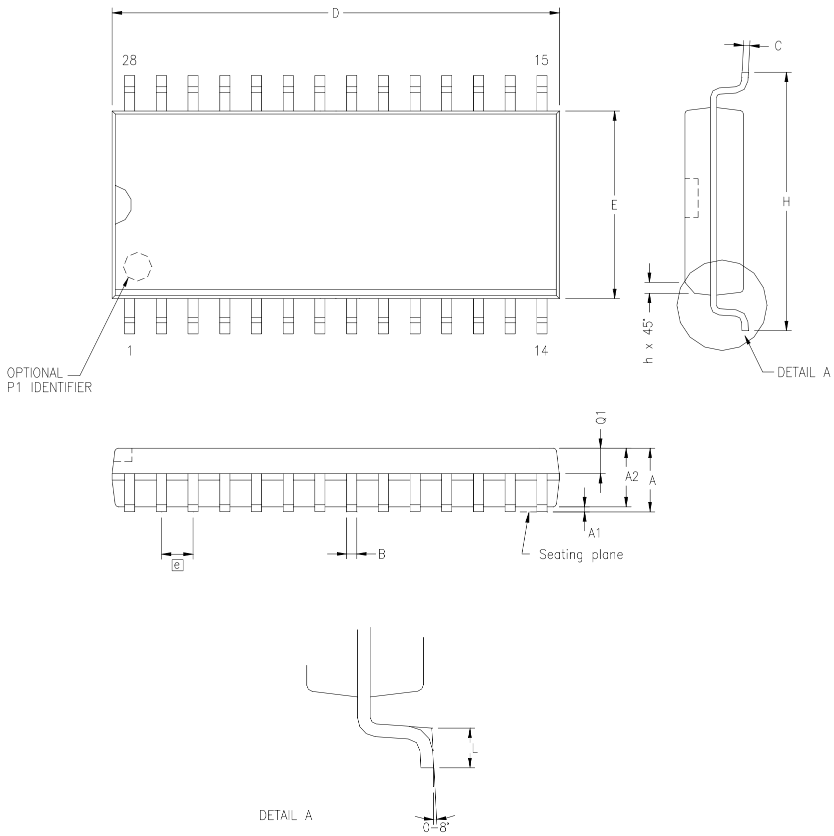
Figure 52. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 53. Register Pointer (FDH: Read/Write)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

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Figure 61. 28-Pin SOIC Package Diagram