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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlp32300p4004g

Architectural Overview

Zilog's Crimzon® ZLP32300 is an OTP-based member of the MCU family of infrared microcontrollers. With 237 B of general-purpose RAM and 8 KB to 32 KB of OTP, Zilog's CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Crimzon ZLP32300 architecture (see Figure 1 on page 3) is based on Zilog's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® CPU offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations:

1. Program Memory
2. Register File
3. Expanded Register File

The register file is composed of 256 Bytes of RAM. It includes four I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Crimzon ZLP32300 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2 on page 4). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

Note: *All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.*

Power connections use the conventional descriptions listed in Table 1.

Table 1. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

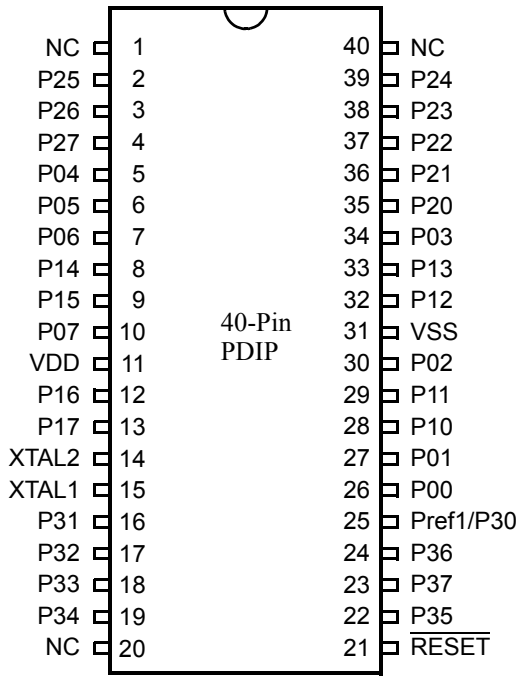


Figure 5. 40-Pin PDIP Pin Configuration

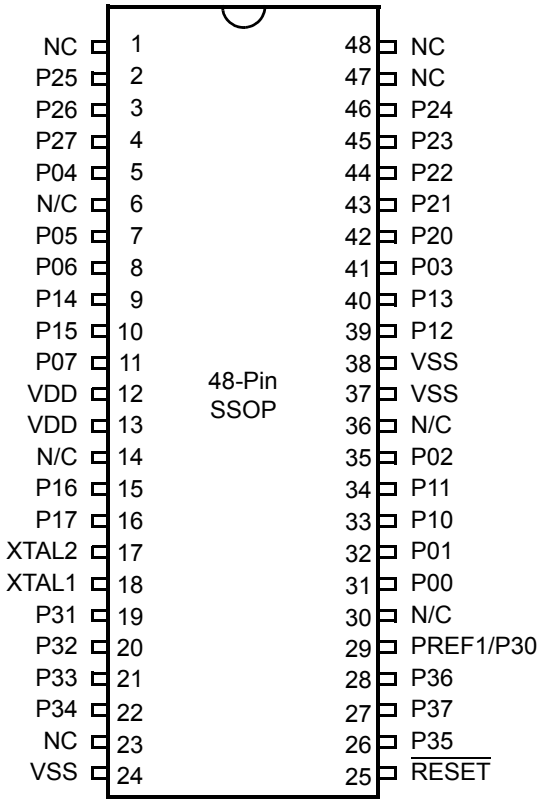


Figure 6. 48-Pin SSOP Pin Configuration

Table 5. 40- and 48-Pin Configuration

40-Pin PDIP No	48-Pin SSOP No	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11

Table 5. 40- and 48-Pin Configuration (Continued)

40-Pin PDIP No	48-Pin SSOP No	Symbol
32	39	P12
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	$\overline{\text{RESET}}$
15	18	XTAL1
14	17	XTAL2
11	12, 13	V_{DD}
31	24, 37, 38	V_{SS}
25	29	Pref1/P30
	48	NC
	6	NC

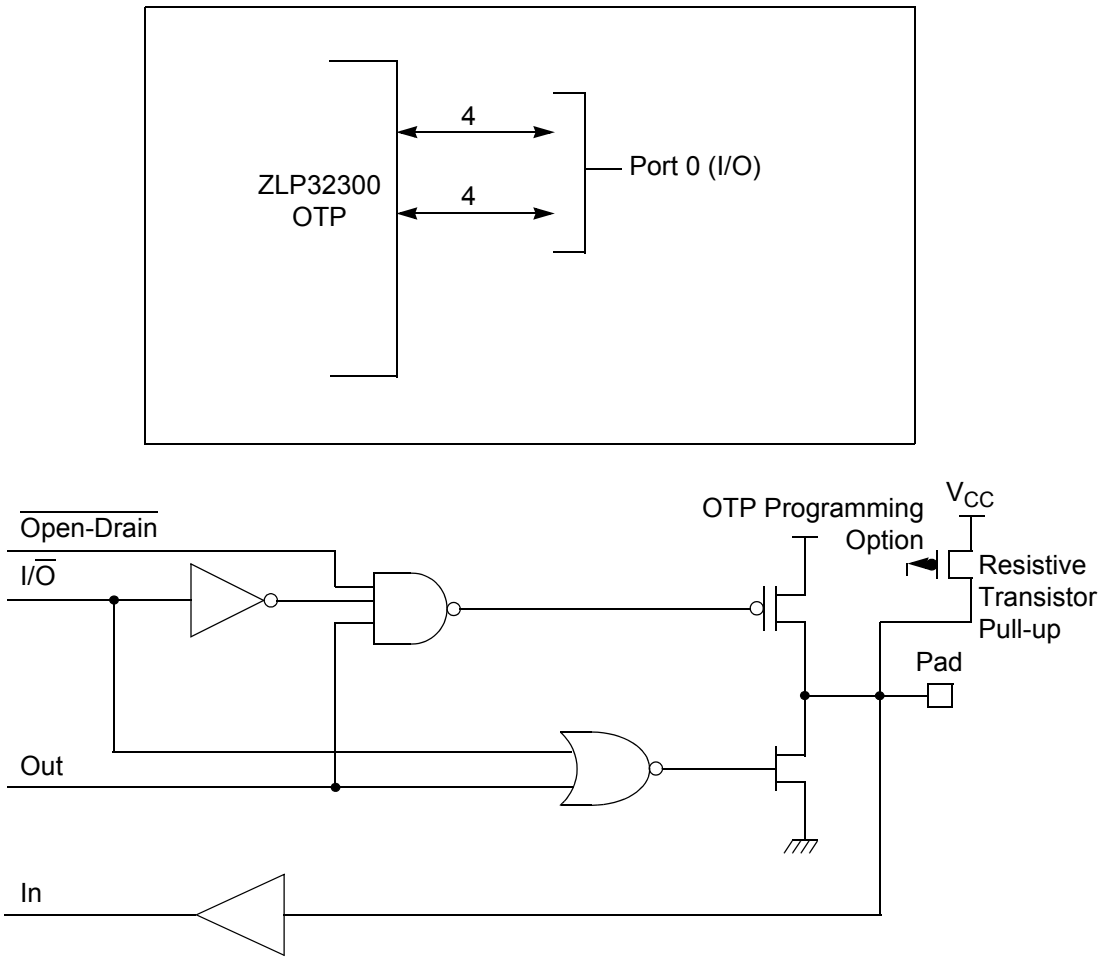


Figure 7. Port 0 Configuration

Port 1 (P17–P10)

Port 1 can be configured for standard port input or output mode (see Figure 8). After POR or Stop Mode Recovery, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

Notes:
1. *The Port 1 direction is reset to be input following an SMR.*
2. *In 20- and 28-pin packages, Port 1 is reserved. A write to this register will have no effect and will always read FF.*

T8_Capture_LO—L08(D)0Ah

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_L0	[7:0]	R/W	Captured Data—No Effect

T16_Capture_HI—HI16(D)09h

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data—No Effect

T16_Capture_LO—L016(D)08h

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	[7:0]	R/W	Captured Data—No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07h

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data

Counter/Timer2 LS-Byte Hold Register—TC16L(D)06h

Field	Bit Position		Description
T16_Data_LO	[7:0]	R/W	Data

Counter/Timer8 High Hold Register—TC8H(D)05h

Field	Bit Position		Description
T8_Level_HI	[7:0]	R/W	Data

Counter/Timer8 Low Hold Register—TC8L(D)04h

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

CTR0 Counter/Timer8 Control Register—CTR0(D)00h

Table 7 lists and briefly describes the fields for this register.

Table 7. CTR0(D)00h Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R/W	0* 1 0 1	Counter Disabled Counter Enabled Stop Counter Enable Counter
Single/Modulo-N	-6-------	R/W	0* 1	Modulo-N Single Pass
Time_Out	--5------	R/W	0** 1 0 1	No Counter Time-Out Counter Time-Out Occurred No Effect Reset Flag to 0
T8 _Clock	---43---	R/W	0 0** 0 1 1 0 1 1	SCLK SCLK/2 SCLK/4 SCLK/8
Capture_INT_Mask	-----2--	R/W	0** 1	Disable Data Capture Interrupt Enable Data Capture Interrupt
Counter_INT_Mask	------1-	R/W	0** 1	Disable Time-Out Interrupt Enable Time-Out Interrupt
P34_Out	-------0	R/W	0* 1	P34 as Port Output T8 Output on P34

*Indicates the value upon Power-On Reset.
**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

CTR3 T8/T16 Control Register—CTR3(D)03h

Table 10 lists and briefly describes the fields for this register. This register allows the T_8 and T_{16} counters to be synchronized.

Table 10.CTR3 (D)03h: T8/T16 Control Register

Field	Bit Position		Value	Description
T_{16} Enable	7-------	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T_8 Enable	-6------	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	--5-----	R/W	0**	Disable Sync Mode
			1	Enable Sync Mode
Reserved	---43210	R	1	Always reads 11111
		W	x	No Effect

*Indicates the value upon Power-On Reset.
**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 16).

T16 TRANSMIT Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set, see Figure 23.

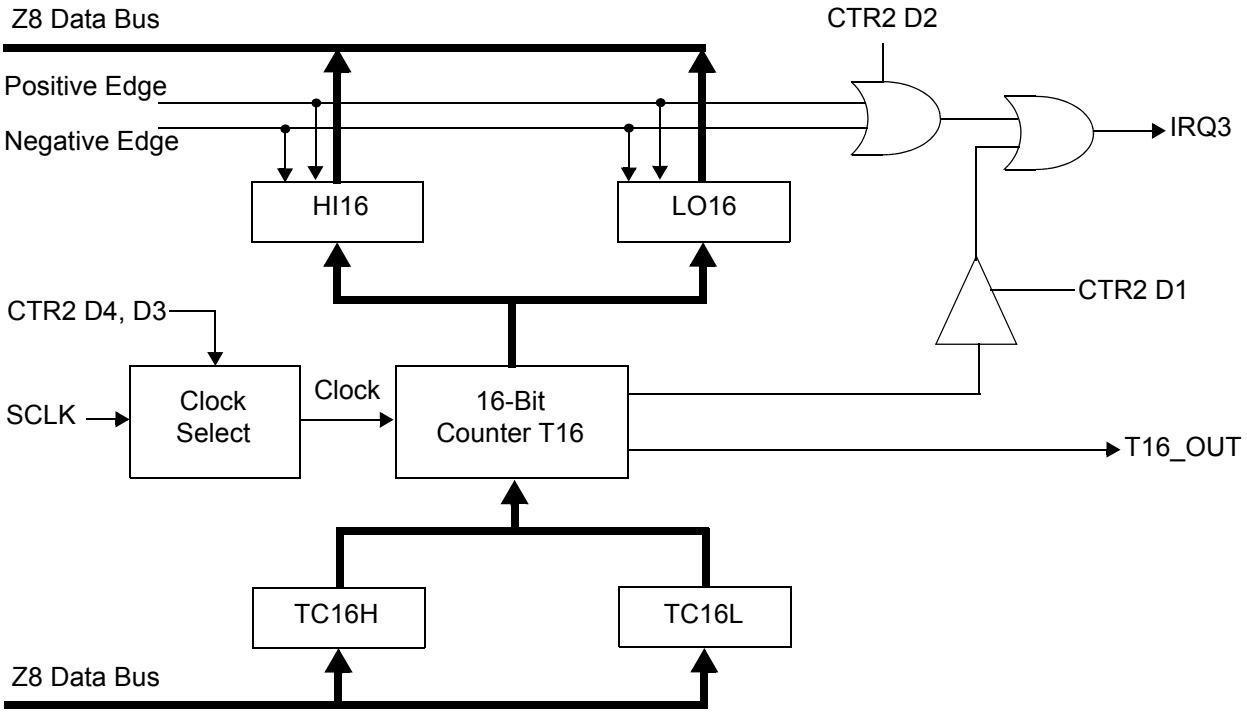


Figure 23. 16-Bit Counter/Timer Circuits

Note: *Global interrupts override this function as described in* Interrupts on page 43.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 24). If it is in MODULO-N mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 25).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.

counter/timers (see Table 11 on page 45) and one for low-voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in DIGITAL mode, Pin P33 is the source. When in ANALOG mode, the output of the Stop Mode Recovery source logic is used as the source for the interrupt, see Figure 33 on page 52.

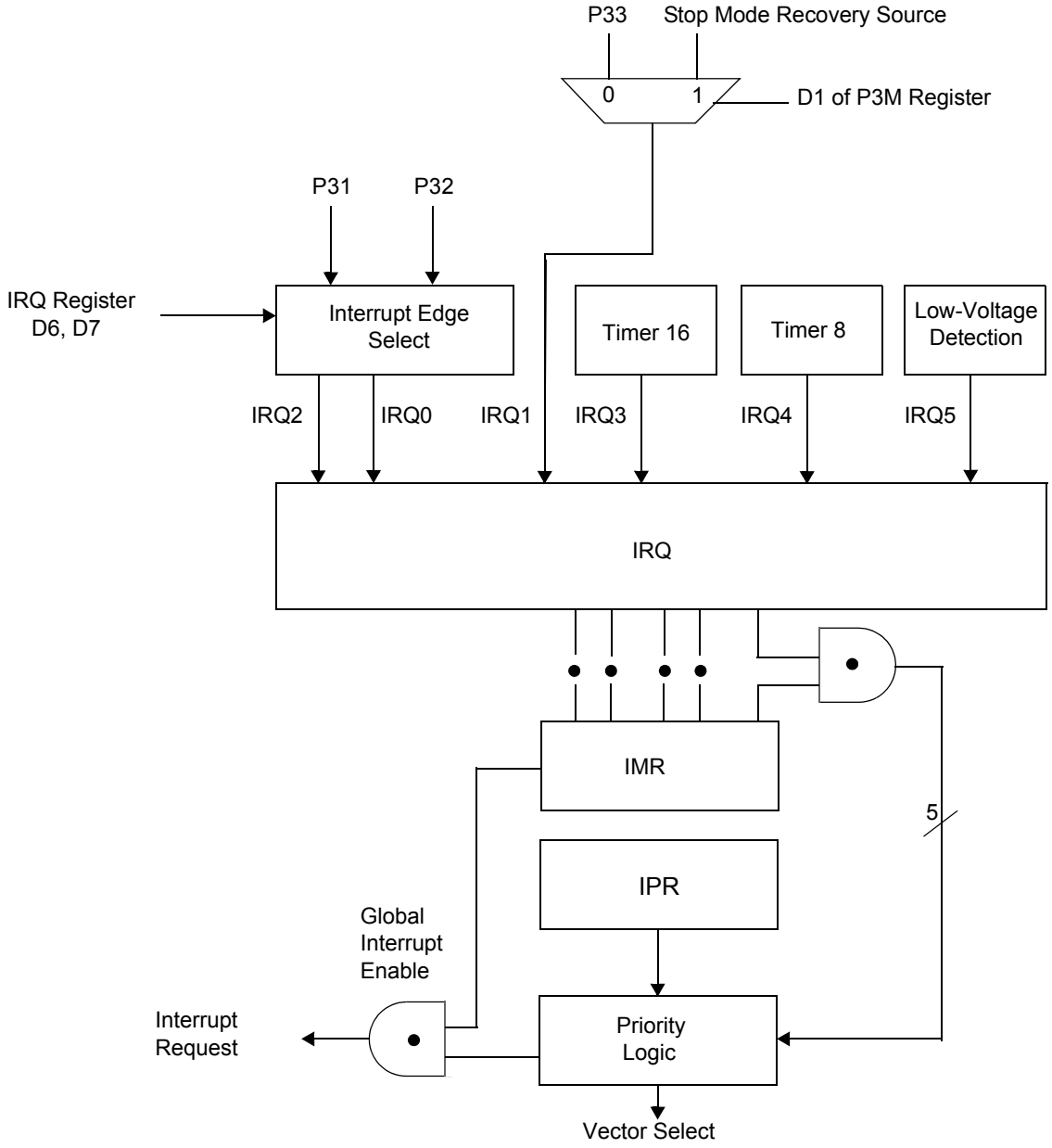
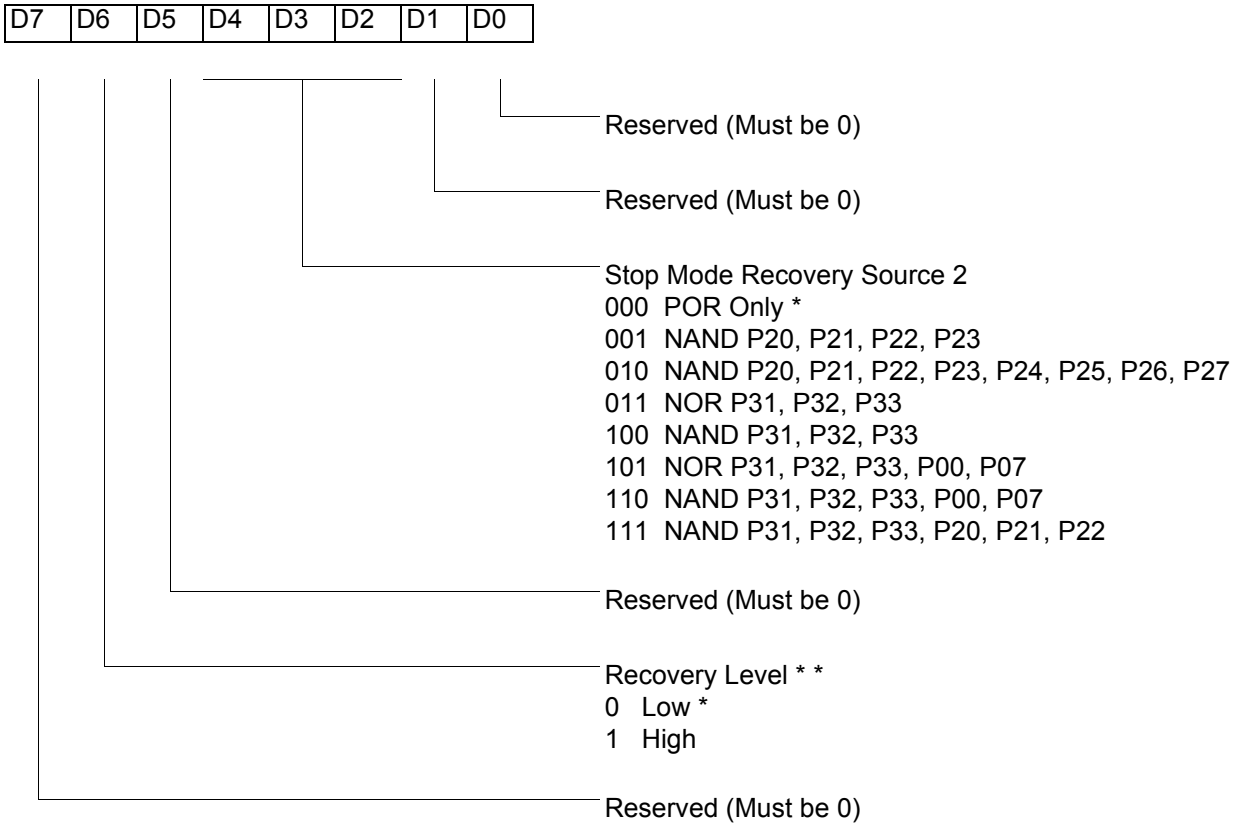


Figure 28. Interrupt Block Diagram

Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (see Figure 34).

SMR2(0F)Dh

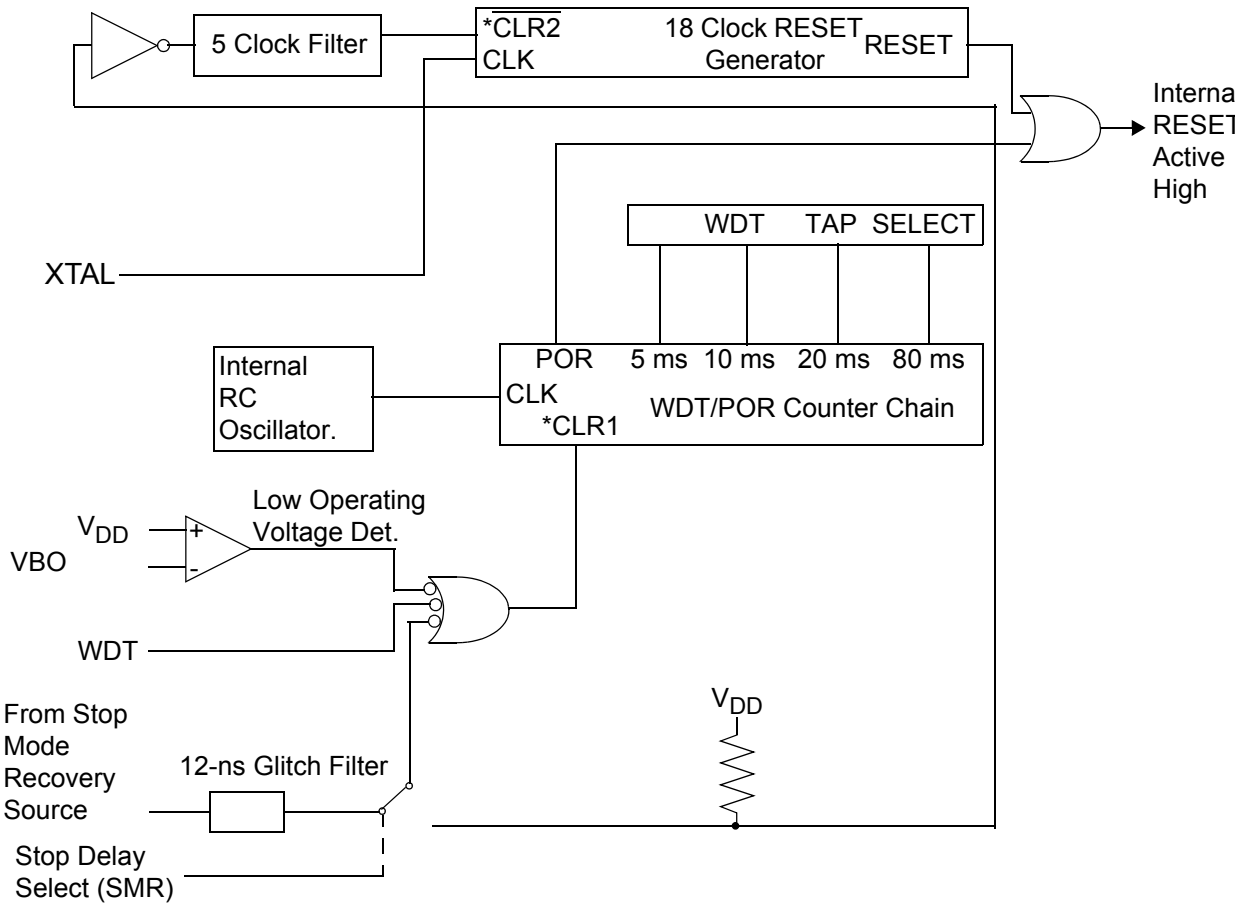


If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.
*Default setting after reset.
* *At the XOR gate input.

Figure 34. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

Note: *Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.*



* CLR1 and $\overline{CLR2}$ enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-High

Figure 36. Resets and WDT

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP mode. A 1 indicates active during Stop. The default is 1.

EPROM Selectable Options

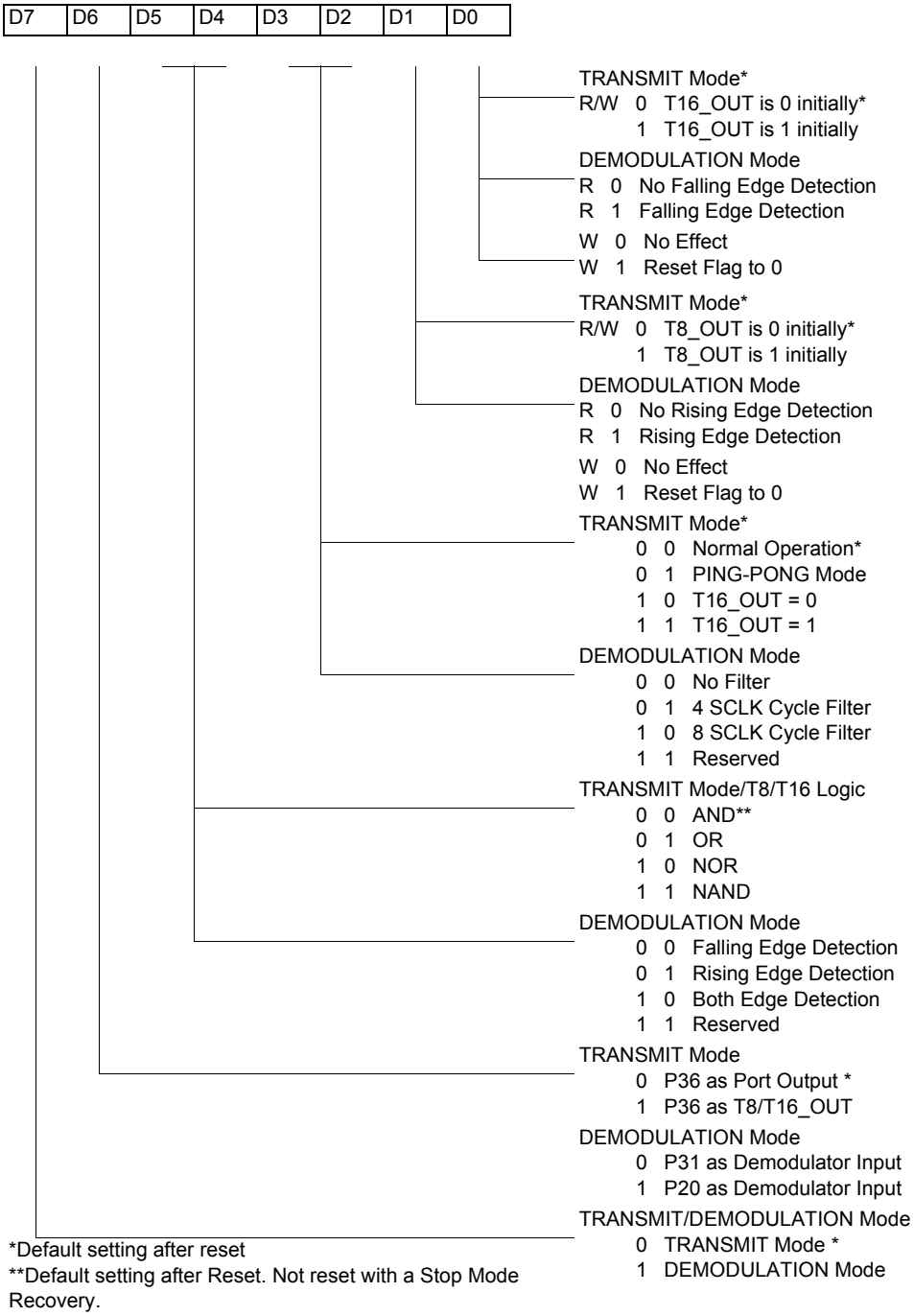
There are seven EPROM Selectable Options to choose from based on ROM code requirements. These are listed in Table 16.

Voltage Detection and Flags

The Voltage Detection register (LVD, register 0Ch at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the V_{CC} level is monitored in real time. The HVD Flag (bit 2 of the LVD register) is set only if V_{CC} is higher than $V_{HVD.}$ The LVD Flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD}. When Voltage Detection is enabled, the LVD Flag also triggers IRQ5. The IRQ bit 5 latches the low-voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a Flag only.

Note: *If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt (EI) instruction prior to enabling the voltage detection.*

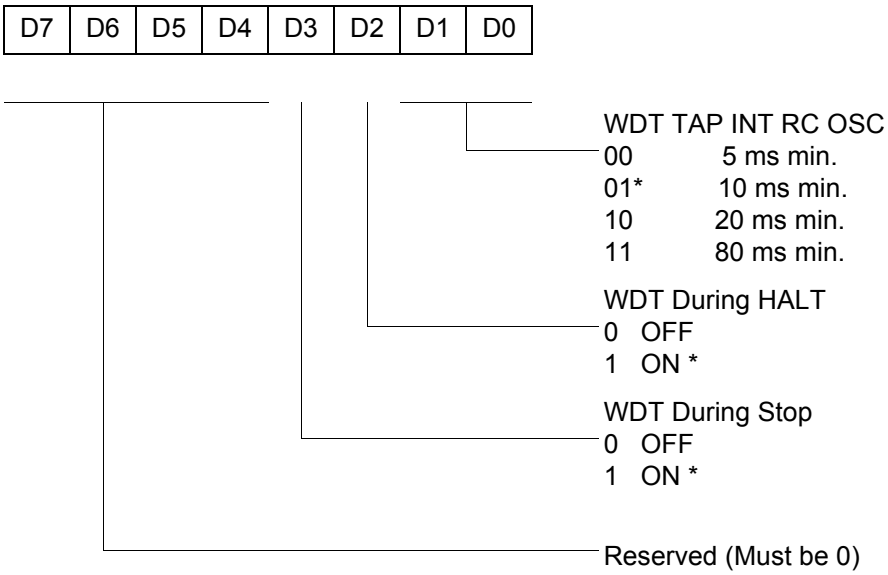
CTR1(0D)01H



*Default setting after reset
**Default setting after Reset. Not reset with a Stop Mode Recovery.

Figure 38. T8 and T16 Common Control Functions ((0D)01H: Read/Write)

WDTMR(0F)0FH



*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 45. Watchdog Timer Register ((0F) 0FH: Write Only)

R249 IPR(F9H)

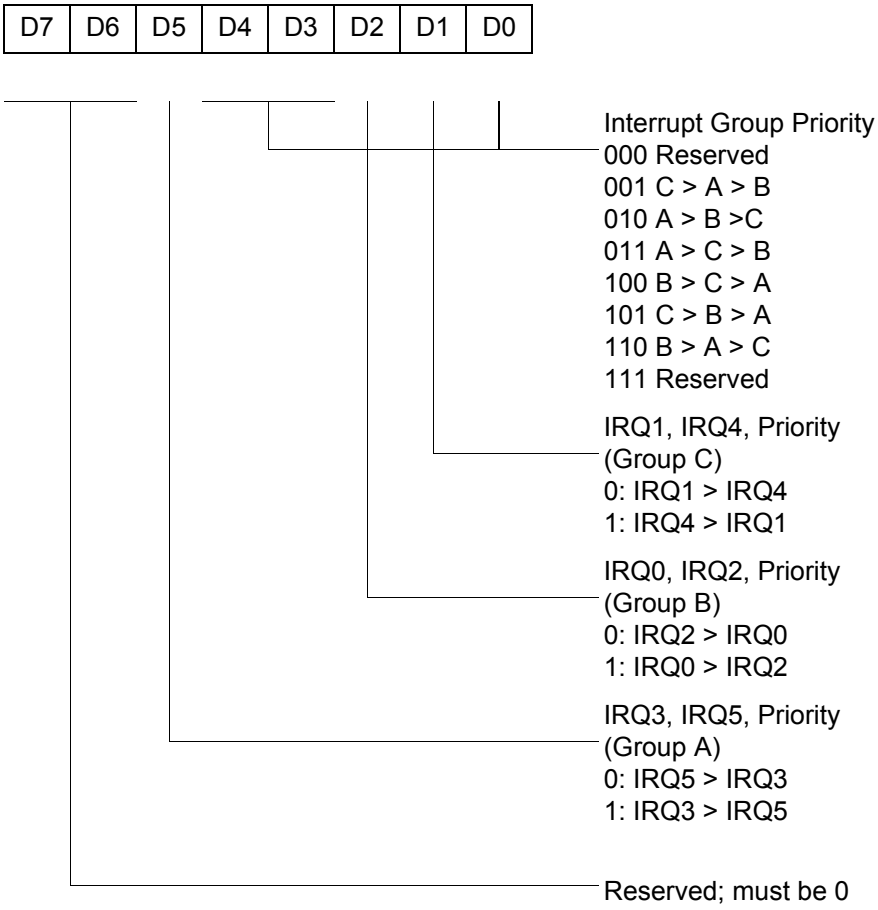


Figure 49. Interrupt Priority Register (F9H: Write Only)

R254 SPH(FEH)

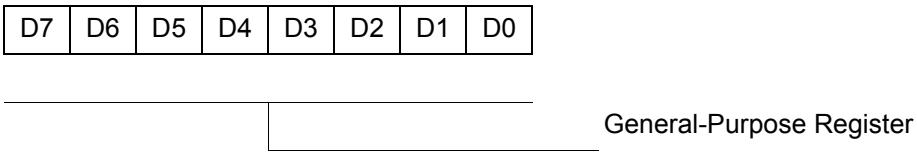


Figure 54. Stack Pointer High (FEH: Read/Write)

R255 SPL(FFH)

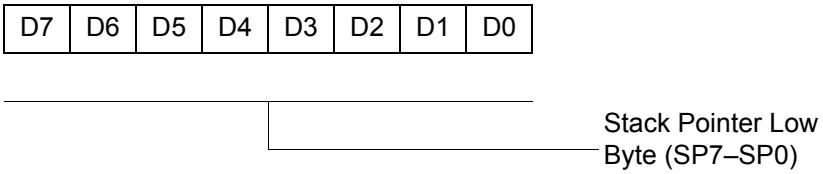


Figure 55. Stack Pointer Low (FFH: Read/Write)

Table 20. AC Characteristics

			T_A=0 °C to +70 °C 8.0 MHz					Watchdog Timer Mode Register (D1, D0)
No	**Symbol**	**Parameter**	**V_{CC}**	**Minimum**	**Maximum**	**Units**	**Notes**	
1	TpC	Input Clock Period	2.0–3.6	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1	
3	TwC	Input Clock Width	2.0–3.6	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–3.6	3TpC			1	
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–3.6	5TpC			1, 2	
10	Twsm	Stop Mode Recovery Width Spec	2.0–3.6	12 10TpC		ns	3 4	
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4	
12	Twdt	Watchdog Timer Delay Time	2.0–3.6 2.0–3.6 2.0–3.6 2.0–3.6	5 10 20 80		ms ms ms ms		0, 0 0, 1 1, 0 1, 1
13	T_{POR}	Power-on reset	2.0–3.6	2.5	10	ms		

Notes
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR–D5 = 1.
4. SMR–D5 = 0.

S

T

V

W

X

Z