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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlp32300p4016c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Architectural Overview

Zilog's Crimzon[®] ZLP32300 is an OTP-based member of the MCU family of infrared microcontrollers. With 237 B of general-purpose RAM and 8 KB to 32 KB of OTP, Zilog's CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Crimzon ZLP32300 architecture (see Figure 1 on page 3) is based on Zilog's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8[®] CPU offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations:

- 1. Program Memory
- 2. Register File
- 3. Expanded Register File

The register file is composed of 256 Bytes of RAM. It includes four I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Crimzon ZLP32300 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2 on page 4). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

Note: All signals with an overline, " $\overline{}$ ", are active Low. For example, B/\overline{W} , in which WORD is active Low, and \overline{B}/W , in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 1.

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

Table 1. Power Connections





Figure 5. 40-Pin PDIP Pin Configuration







Port 1 (P17–P10)

Port 1 can be configured for standard port input or output mode (see Figure 8). After POR or Stop Mode Recovery, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

- **Notes:** 1. The Port 1 direction is reset to be input following an SMR.
 - 2. In 20- and 28-pin packages, Port 1 is reserved. A write to this register will have no effect and will always read FF.

(see T8 and T16 Common Functions—CTR1(0D)01h on page 28). Other edge detect and IRQ modes are described in Table 6.

Note: Comparators are powered down by entering STOP mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into DIGITAL mode.

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	Т8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

 Table 6. Port 3 Pin Function Summary

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 11). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

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The upper nibble of the register pointer (see Figure 14) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Crimzon ZLP32300 family, banks 0, F, and D are implemented. A 0h in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1h to Fh exchanges the lower 16 registers to an expanded register bank.







Example: Crimzon ZLP32300 (see Figure 13 on page 22)

R253 RP = 00h R0 = Port 0 R1 = Port 1 R2 = Port 2 R3 = Port 3

But if:

R253 RP = 0DhR0 = CTR0R1 = CTR1R2 = CTR2R3 = CTR3

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

LD	RP, #0Dh	; Select	ERF D
for access to bank D			
		; (worki	ng
register group 0)			
LD	R0,#xx	; load C	TR0
LD	1, #xx	; load C	TR1

R1, 2 LD; CTR2→CTR1 LD RP, #0Dh ; Select ERF D for access to bank D ; (working register group 0) ; Select LDRP, #7Dh expanded register bank D and working ; register group 7 of bank 0 for access. LD 71h, 2 ; CTRL2 \rightarrow register 71h LD R1, 2 ; CTRL2 \rightarrow register 71h

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 7 on page 27) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (see Figure 15). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.



Working register group E0–EF can only be accessed through working registers and indirect addressing modes.

Crimzon[®] ZLP32300 Product Specification

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Counter/Timer8 High Hold Register—TC8H(D)05h

Field	Bit Position		Description
T8_Level_HI	[7:0]	R/W	Data

Counter/Timer8 Low Hold Register—TC8L(D)04h

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

CTR0 Counter/Timer8 Control Register—CTR0(D)00h

Table 7 lists and briefly describes the fields for this register.

Table 7. CTR0(D)00h Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6	R/W	0*	Modulo-N
			1	Single Pass
Time_Out	5	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8 _Clock	43	R/W	0 0**	SCLK
			0 1	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	2	R/W	0**	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt
Counter_INT_Mask	1-	R/W	0**	Disable Time-Out Interrupt
			1	Enable Time-Out Interrupt
P34_Out	0	R/W	0*	P34 as Port Output
			1	T8 Output on P34

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.



Table 8. CTR1(0D)01h T8 and T16 Common Functions

Field	Bit Position		Value	Description
Mode	7	R/W	0*	TRANSMIT Mode
			1	DEMODULATION Mode
P36_Out/	-б	R/W		TRANSMIT Mode
Demodulator_Input			0*	Port Output
			1	T8/T16 Output
				DEMODULATION Mode
			0*	P31
			1	P20
T8/T16_Logic/	54	R/W		TRANSMIT Mode
Edge _Detect			00**	AND
			01	OR
			10	NOR
			11	NAND
				DEMODULATION Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved
Transmit_Submode/	32	R/W		TRANSMIT Mode
Glitch_Filter			00*	Normal Operation
			01	PING-PONG Mode
			10	T16_Out = 0
			11	T16_Out = 1
				DEMODULATION Mode
			00*	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/	1-			TRANSMIT Mode
Rising Edge		R/W	0*	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				DEMODULATION Mode
		R	0*	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0





Figure 17. TRANSMIT Mode Flowchart

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When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0, D5) is set, and a time-out interrupt can be generated if it is enabled (CTR0, D1). In MODULO-N mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the time-out status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle, see Figure 18.



Figure 18. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.

Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to FFh to FFh.

Note: *The letter* h *denotes hexadecimal values.*

Transition from 0 to FFh is not a timeout condition.

interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 21 and Figure 22).



Figure 21. DEMODULATION Mode Count Capture Flowchart





Figure 22. DEMODULATION Mode Flowchart

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Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω . The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors from each pin to ground. The typical capacitor value is 10 pF for 8 MHz. Also check with the crystal supplier for the optimum capacitance.



*Note: preliminary value.

Figure 29. Oscillator Configuration

Zilog's IR MCU supports crystal, resonator, and oscillator. Most resonators have a frequency tolerance of less than $\pm 0.5\%$, which is enough for remote control application. Resonator has a very fast startup time, which is around few hundred microseconds. Most crystals have a frequency tolerance of less than 50 ppm ($\pm 0.005\%$). However, crystal needs longer startup time than the resonator. The large loading capacitance slows down the oscillation startup time. Zilog[®] suggests not to use more than 10 pF loading capacitor for the crystal. If the stray capacitance of the PCB or the crystal is high, the loading capacitance C1 and C2 must be reduced further to ensure stable oscillation before the T_{POR} (Power-On Reset time is typically 5-6 ms, see Table 20 on page 79).

For Stop Mode Recovery operation, bit 5 of SMR register allows you to select the Stop Mode Recovery delay, which is the T_{POR} . If Stop Mode Recovery delay is not selected, the MCU executes instruction immediately after it wakes up from the STOP mode. If resonator or crystal is used as a clock source then Stop Mode Recovery delay needs to be selected (bit 5 of SMR = 1).



* CLR1 and CLR2 enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-High

Figure 36. Resets and WDT

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP mode. A 1 indicates active during Stop. The default is 1.

EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These are listed in Table 16.

Crimzon[®] ZLP32300 Product Specification

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Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are displayed in Figure 37 through Figure 41.

CTR0(0D)00H



*Default setting after reset.

**Default setting after reset. Not reset with a Stop Mode Recovery.

Figure 37. TC8 Control Register ((0D)O0H: Read/Write Except Where Noted)



CTR3(0D)03H



**Default setting after reset. Not reset with a Stop Mode Recovery.

Figure 40. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)

Note: If Sync Mode is enabled, the first pulse of T8 carrier is always synchronized with T16 (demodulated signal). It can always provide a full carrier pulse.



WDTMR(0F)0FH



*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 45. Watchdog Timer Register ((0F) 0FH: Write Only)



AC Characteristics

Figure 57 and Table 20 describe the Alternating Current (AC) characteristics.









Note: ZiLOG supplies both options for production. Component layout PCB design should cover bigger option 01.





Ordering Information

The Crimzon ZLP32300 is available for the following parts:

Device	Part Number	Description
Crimzon	ZLP32300H4832G	48-pin SSOP 32 K OTP
ZLP32300	ZLP32300P4032G	40-pin PDIP 32 K OTP
	ZLP32300H2832G	28-pin SSOP 32 K OTP
	ZLP32300P2832G	28-pin PDIP 32 K OTP
	ZLP32300S2832G	28-pin SOIC 32 K OTP
	ZLP32300H2032G	20-pin SSOP 32 K OTP
	ZLP32300P2032G	20-pin PDIP 32 K OTP
	ZLP32300S2032G	20-pin SOIC 32 K OTP
	ZLP32300H4816G	48-pin SSOP 16 K OTP
	ZLP32300P4016G	40-pin PDIP 16 K OTP
	ZLP32300H2816G	28-pin SSOP 16 K OTP
	ZLP32300P2816G	28-pin PDIP 16 K OTP
	ZLP32300S2816G	28-pin SOIC 16 K OTP
	ZLP32300H2016G	20-pin SSOP 16 K OTP
	ZLP32300P2016G	20-pin PDIP 16 K OTP
	ZLP32300S2016G	20-pin SOIC 16 K OTP
	ZLP32300H4808G	48-pin SSOP 8 K OTP
	ZLP32300P4008G	40-pin PDIP 8 K OTP
	ZLP32300H2808G	28-pin SSOP 8 K OTP
	ZLP32300P2808G	28-pin PDIP 8 K OTP
	ZLP32300S2808G	28-pin SOIC 8 K OTP
	ZLP32300H2008G	20-pin SSOP 8 K OTP