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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

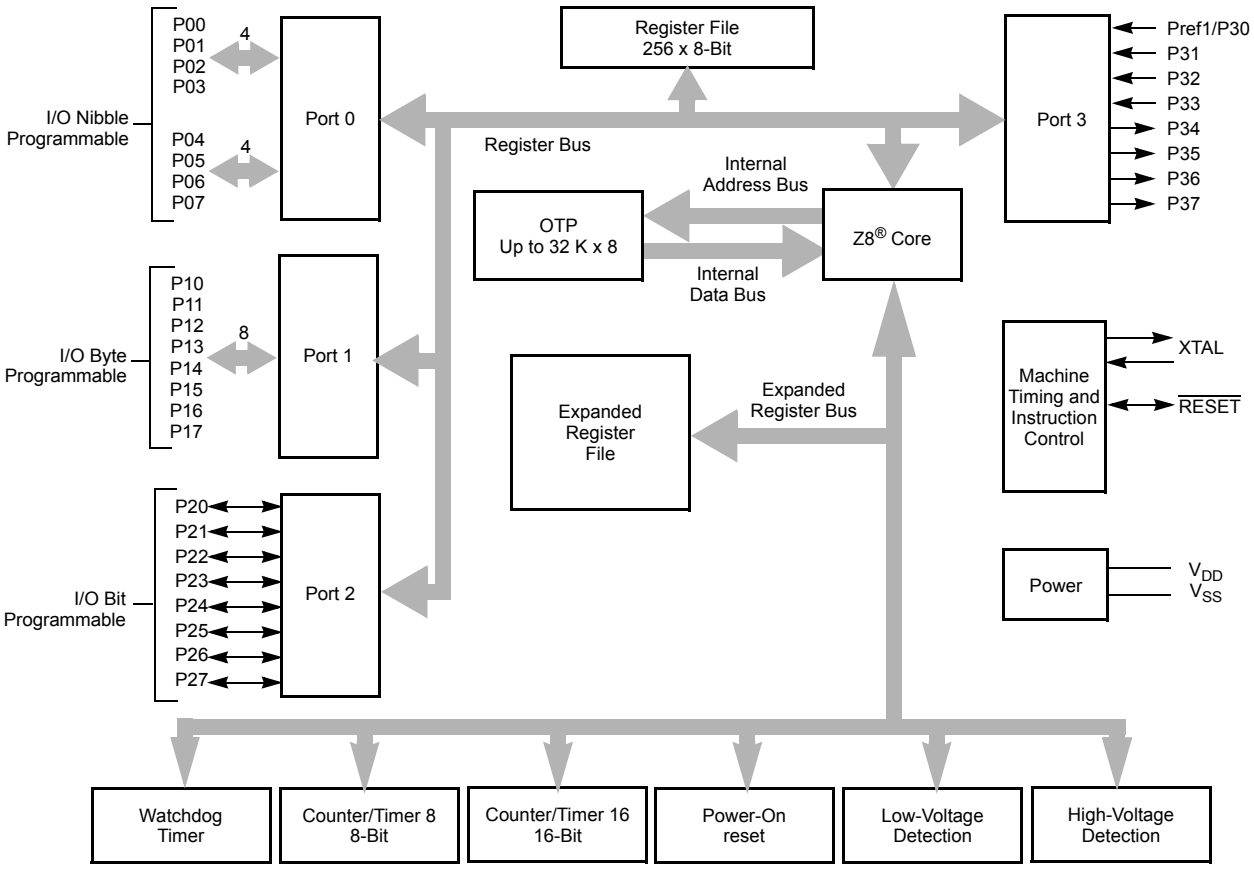
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, HLVD, POR, WDT |
| Number of I/O | 32 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 40-DIP (0.600", 15.24mm) |
| Supplier Device Package | 40-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/zlp32300p4032c |

- Port 2: 0–7 pull-up transistors
- EPROM Protection
- WDT enabled at POR

## Functional Block Diagram

Figure 1 displays the Crimzon ZLP32300 MCU functional block diagram.




Note: Refer to the specific package for available pins.

**Figure 1. Crimzon ZLP32300 MCU Functional Block Diagram**

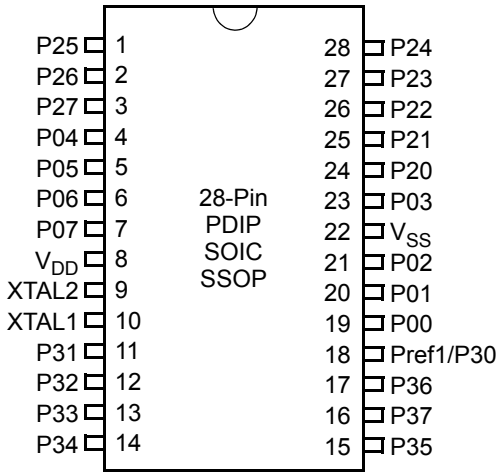



**Figure 4. 28-Pin PDIP/SOIC/SSOP Pin Configuration**

**Table 4. 28-Pin PDIP/SOIC/SSOP Pin Identification**

| Pin No | Symbol | Direction | Description |
|---|---|---|---|
| 1-3 | P25-P27 | Input/Output | Port 2, Bits 5, 6, 7 |
| 4-7 | P04-P07 | Input/Output | Port 0, Bits 4, 5, 6, 7 |
| 8 | $V_{DD}$ | | Power supply |
| 9 | XTAL2 | Output | Crystal, oscillator clock |
| 10 | XTAL1 | Input | Crystal, oscillator clock |
| 11-13 | P31-P33 | Input | Port 3, Bits 1, 2, 3 |
| 14 | P34 | Output | Port 3, Bit 4 |
| 15 | P35 | Output | Port 3, Bit 5 |
| 16 | P37 | Output | Port 3, Bit 7 |
| 17 | P36 | Output | Port 3, Bit 6 |
| 18 | Pref1/P30<br>Port 3 Bit 0 | Input | Analog ref input; connect to $V_{CC}$ if not used<br>Input for Pref1/P30 |
| 19-21 | P00-P02 | Input/Output | Port 0, Bits 0, 1, 2 |
| 22 | $V_{SS}$ | | Ground |
| 23 | P03 | Input/Output | Port 0, Bit 3 |
| 24-28 | P20-P24 | Input/Output | Port 2, Bits 0–4 |

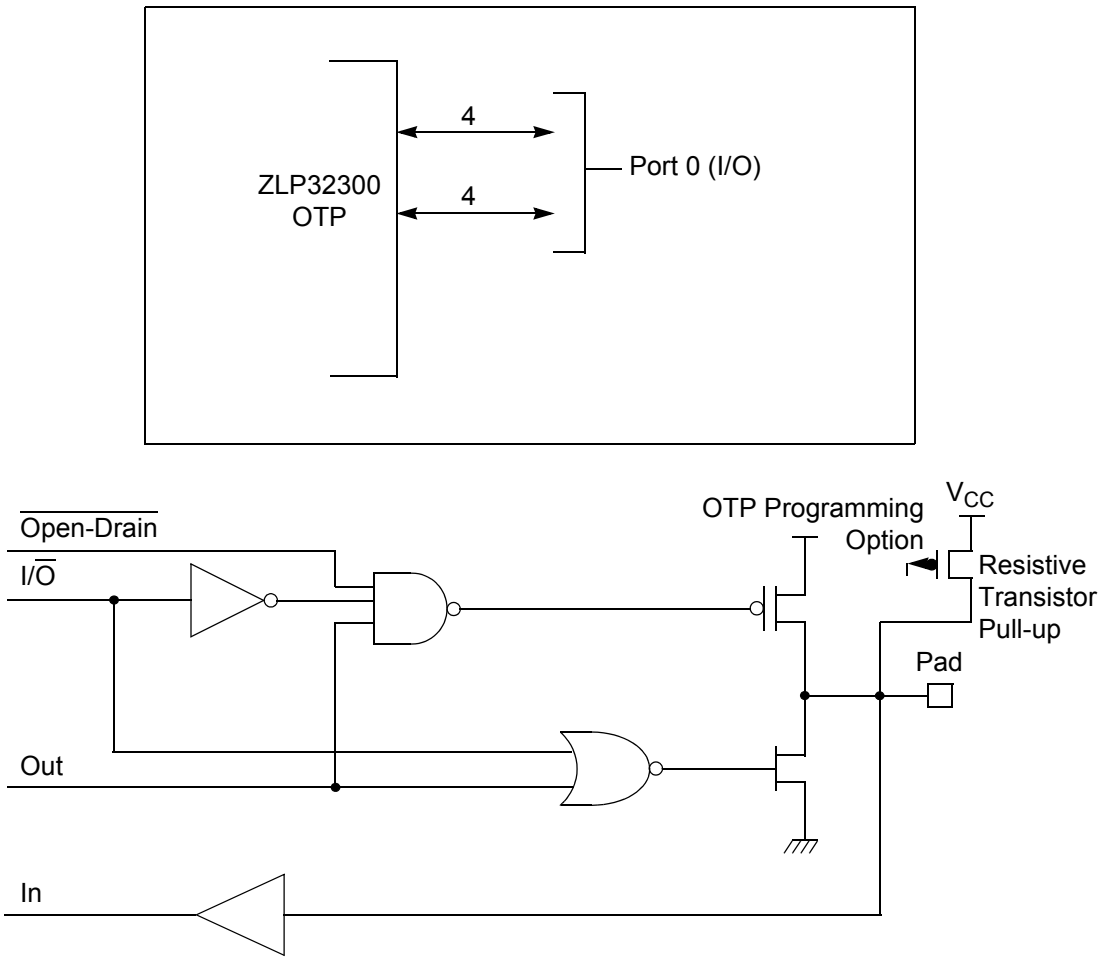



**Figure 7. Port 0 Configuration**

### Port 1 (P17–P10)

Port 1 can be configured for standard port input or output mode (see Figure 8). After POR or Stop Mode Recovery, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

**Notes:**
1. *The Port 1 direction is reset to be input following an SMR.*
2. *In 20- and 28-pin packages, Port 1 is reserved. A write to this register will have no effect and will always read FF.*

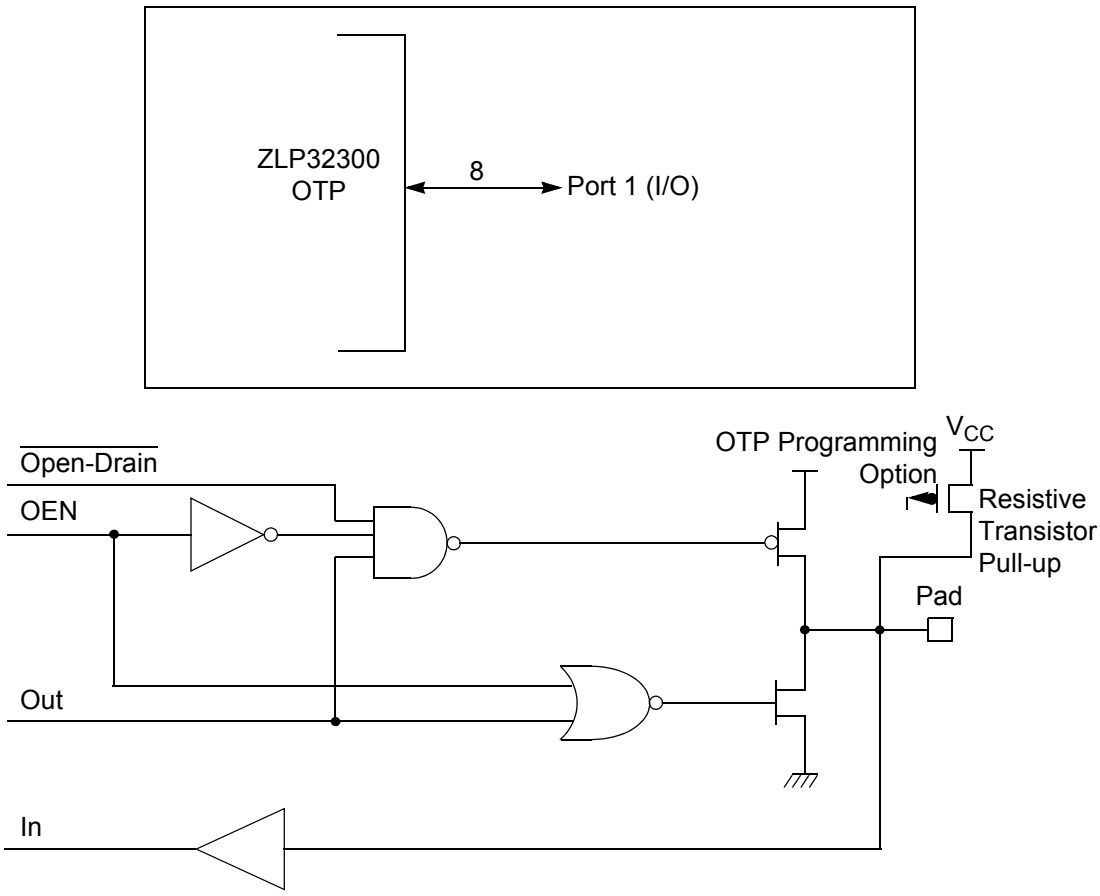



**Figure 8. Port 1 Configuration**

### Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 9). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A EPROM option bit is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in DEMODULATION mode.

### Comparator Inputs

In ANALOG mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as displayed in Figure 10 on page 15. In DIGITAL mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

**Note:** *Comparators are powered down by entering STOP mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into DIGITAL mode.*

### Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

## $\overline{\text{RESET}}$ (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watchdog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watchdog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the ZLP32300 asserts (Low) the $\overline{\text{RESET}}$ pin, the internal pull-up is disabled. The ZLP32300 does not assert the $\overline{\text{RESET}}$ pin when under VBO.

**Note:** *The external Reset does not initiate an exit from STOP mode.*

# Functional Description

This device incorporates special functions to enhance the Z8 functionality in consumer and battery-operated applications.

## Program Memory

This device addresses 32 KB of OTP memory. The first 12 bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts. See Figure 12.

## RAM

This device features 256 B of RAM.

```
LD                      R1, 2                   ; CTR2→CTR1

LD                      RP, #0Dh                ; Select ERF D
for access to bank D
                                                ; (working
register group 0)
LD                      RP, #7Dh                ; Select
expanded register bank D and working            ; register
group 7 of bank 0 for access.
LD                      71h, 2
; CTRL2→register 71h
LD                      R1, 2
; CTRL2→register 71h
```

## Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 7 on page 27) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (see Figure 15). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

**Note:** *Working register group E0–EF can only be accessed through working registers and indirect addressing modes.*

### T8_Capture_LO—L08(D)0Ah

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

| Field | Bit Position | | Description |
|---|---|---|---|
| T8_Capture_L0 | [7:0] | R/W | Captured Data—No Effect |

### T16_Capture_HI—HI16(D)09h

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

| Field | Bit Position | | Description |
|---|---|---|---|
| T16_Capture_HI | [7:0] | R/W | Captured Data—No Effect |

### T16_Capture_LO—L016(D)08h

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

| Field | Bit Position | | Description |
|---|---|---|---|
| T16_Capture_LO | [7:0] | R/W | Captured Data—No Effect |

### Counter/Timer2 MS-Byte Hold Register—TC16H(D)07h

| Field | Bit Position | | Description |
|---|---|---|---|
| T16_Data_HI | [7:0] | R/W | Data |

### Counter/Timer2 LS-Byte Hold Register—TC16L(D)06h

| Field | Bit Position | | Description |
|---|---|---|---|
| T16_Data_LO | [7:0] | R/W | Data |

### T8 Enable

This field enables T8 when set (written) to 1.

### Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

### Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.

**Caution:** *Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers. The first clock of T8 might not have complete clock width and can occur any time when enabled.*

**Note:** *Ensure to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (DEMODULATION mode) when using the OR or AND commands. These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.*

### T8 Clock

These bits define the frequency of the input signal to T8.

### Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in DEMODULATION mode.

### Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

### P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

## T8 and T16 Common Functions—CTR1(0D)01h

This register controls the functions in common with the T8 and T16.

Table 8 lists and briefly describes the fields for this register.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

### If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

### PING-PONG Mode

This operation mode is only valid in TRANSMIT mode. T8 and T16 must be programmed in SINGLE-PASS mode (CTR0, D6; CTR2, D6), and PING-PONG mode must be programmed in CTR1, D3; D2. You can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1, see Figure 26.

**Note:** *Enabling Ping-Pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status Flags before instituting this operation.*

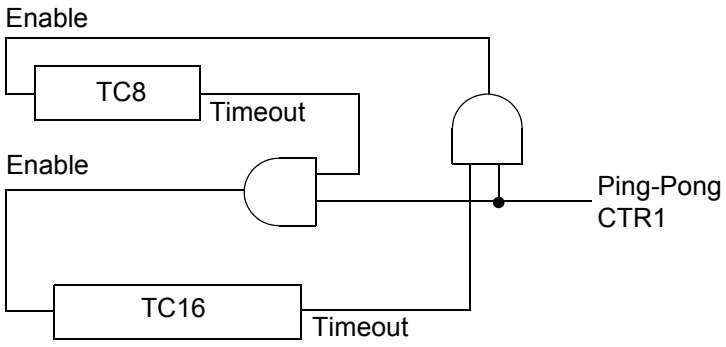



**Figure 26. PING-PONG Mode Diagram**

**Table 14. Stop Mode Recovery Source**

| SMR:432 | | | Operation |
|---|---|---|---|
| D4 | D3 | D2 | Description of Action |
| 0 | 0 | 0 | POR and/or external reset recovery |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | P31 transition |
| 0 | 1 | 1 | P32 transition |
| 1 | 0 | 0 | P33 transition |
| 1 | 0 | 1 | P27 transition |
| 1 | 1 | 0 | Logical NOR of P20 through P23 |
| 1 | 1 | 1 | Logical NOR of P20 through P27 |

**Note:** *Any Port 2 bit defined as an output drives the corresponding input to the default state. For example, if the NOR of P23-P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23-P21) form the NOR equation. This condition allows the remaining inputs to control the AND/OR function, refer to SMR2 register* on page 54 *for other recover sources.*

### Stop Mode Recovery Delay Select (D5)

This bit, if low, disables the $T_{POR}$ delay after Stop Mode Recovery. The default configuration of this bit is 1. If the 'fast' wake up is selected, the Stop Mode Recovery source must be kept active for at least 10 TpC.

**Note:** *This bit must be set to 1 if a crystal or resonator clock source is used. The $T_{POR}$ delay allows the clock source to stabilize before executing instructions.*

### Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Crimzon ZLP32300 from STOP mode. A 0 indicates Low level recovery. The default is 0 on POR.

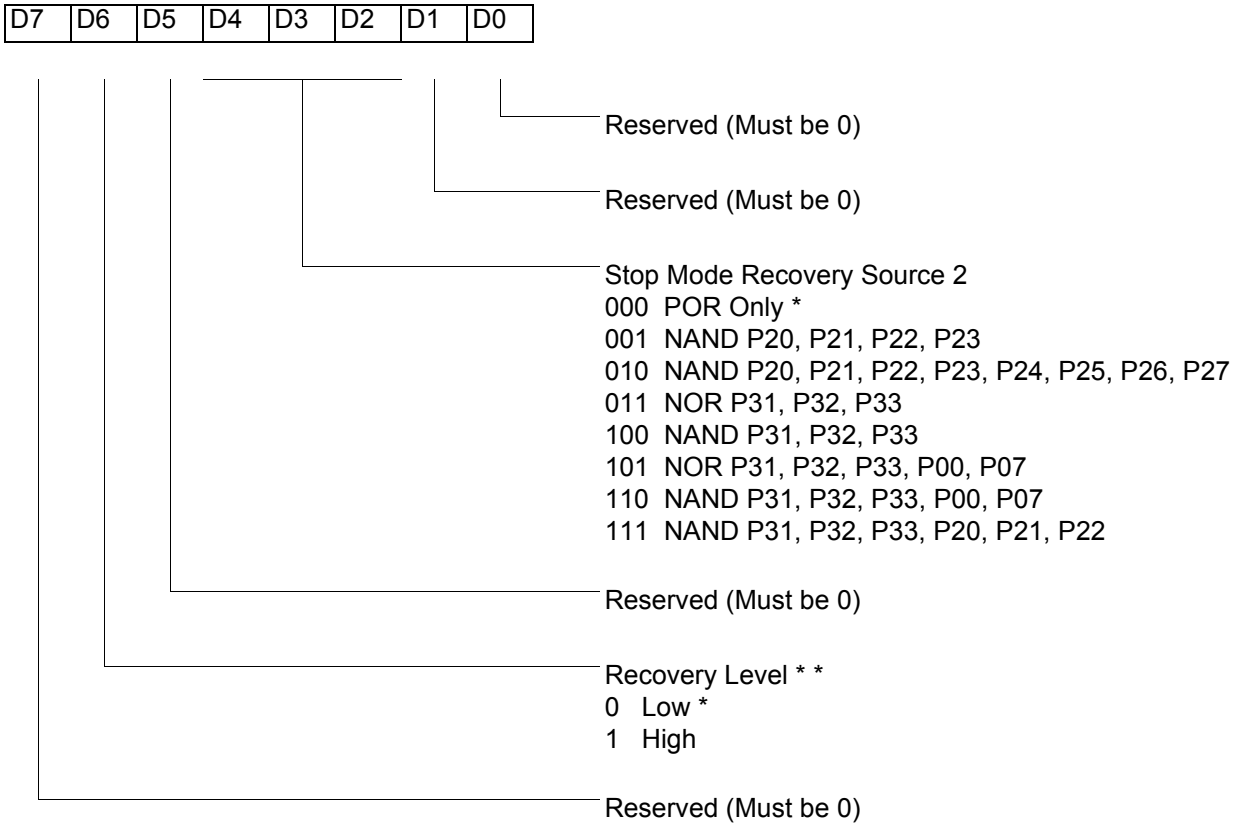
### Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from STOP mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery.

### Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (see Figure 34).

SMR2(0F)Dh




If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.
*Default setting after reset.
* *At the XOR gate input.

**Figure 34. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)**

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

**Note:** *Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.*

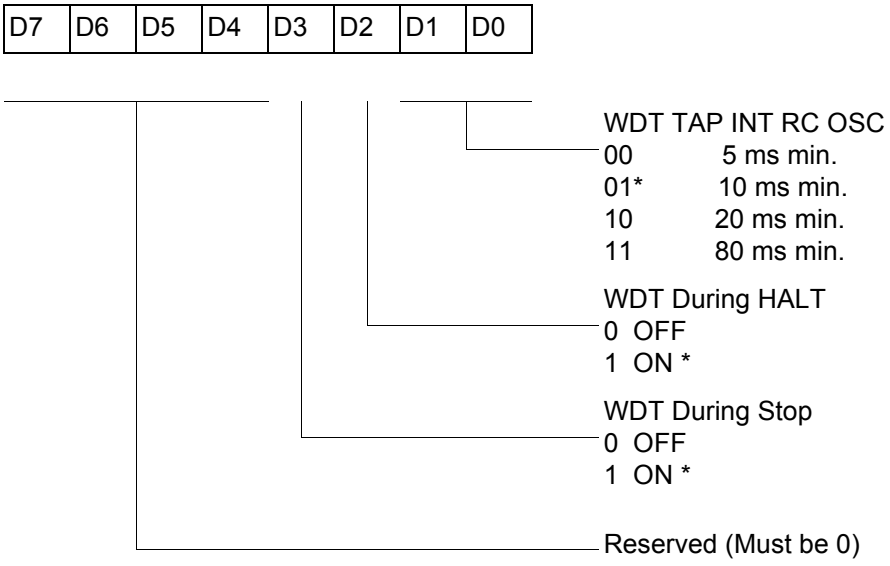
# Watchdog Timer Mode

## Watchdog Timer Mode Register (WDTMR)

The Watchdog Timer is a retriggerable one-shot timer that resets the Z8® if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) Flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum time-out period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (see Figure 35). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-on reset, Watchdog Reset, or a Stop Mode Recovery (see Figure 34). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 35.

WDTMR(0F)0Fh




*Default setting after reset

**Figure 35. Watchdog Timer Mode Register (Write Only)**

**Notes:**

1. *Ensure to differentiate the TRANSMIT mode from DEMODULATION mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.*
2. *Changing from one mode to another cannot be performed without disabling the counter/timers.*

CTR2(0D)02H

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

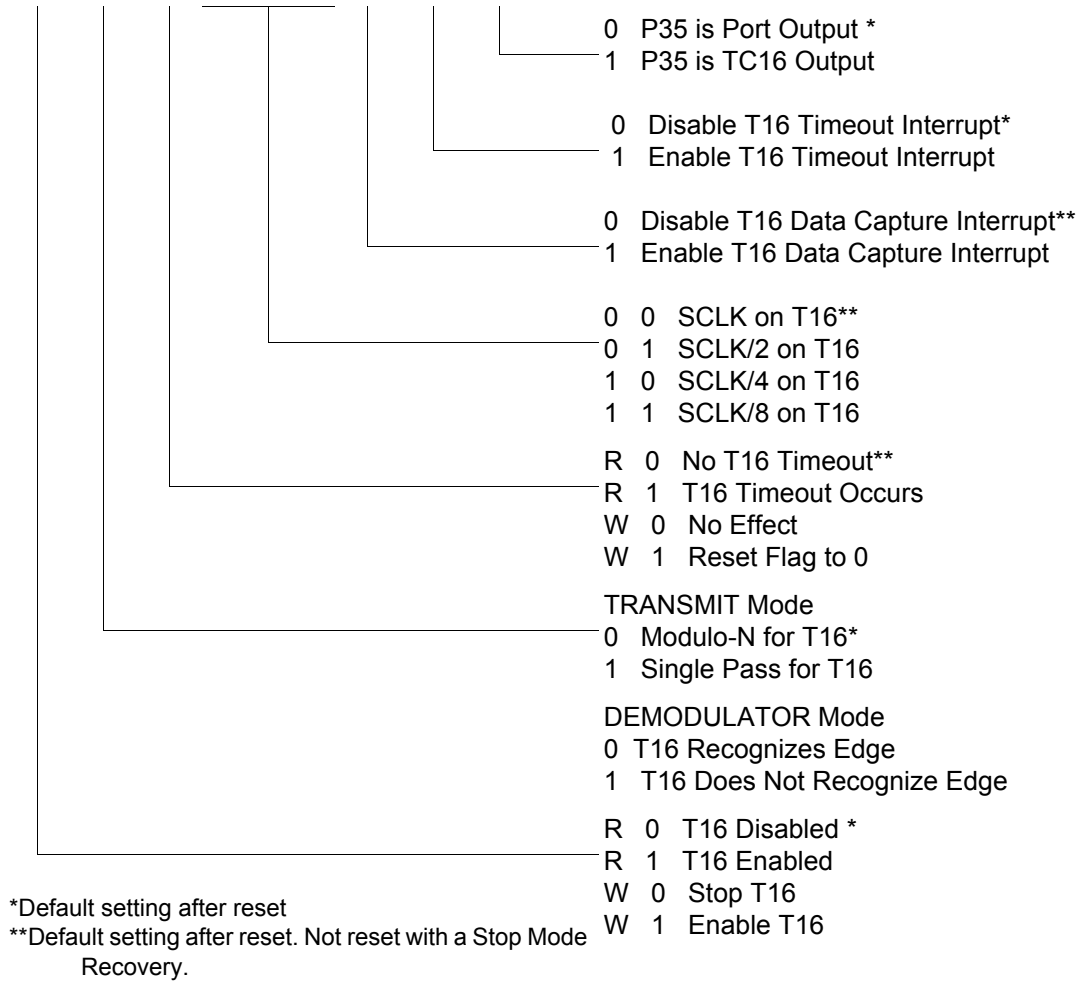
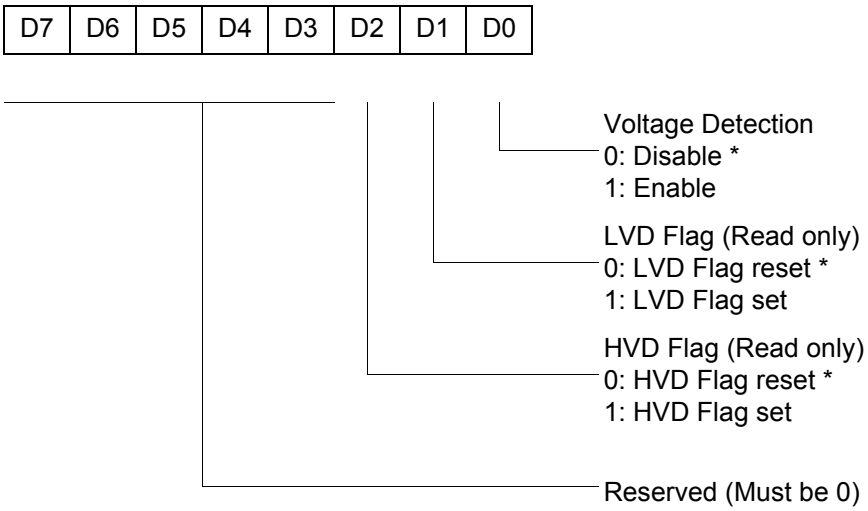



**Figure 39. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)**

LVD(0D)0CH




*Default setting after reset.

**Figure 41. Voltage Detection Register**

**Note:** *Do not modify register P01M while checking a low-voltage condition. Switching noise of both Ports 0 and 1 together might trigger the LVD Flag.*

**Table 20. AC Characteristics**

| | | | $T_A$=0 °C to +70 °C 8.0 MHz | | | | | Watchdog Timer Mode Register (D1, D0) |
|---|---|---|---|---|---|---|---|---|
| **No** | **Symbol** | **Parameter** | **$V_{CC}$** | **Minimum** | **Maximum** | **Units** | **Notes** | |
| 1 | TpC | Input Clock Period | 2.0–3.6 | 121 | DC | ns | 1 | |
| 2 | TrC,TfC | Clock Input Rise and Fall Times | 2.0–3.6 | | 25 | ns | 1 | |
| 3 | TwC | Input Clock Width | 2.0–3.6 | 37 | | ns | 1 | |
| 4 | TwTinL | Timer Input Low Width | 2.0<br>3.6 | 100<br>70 | | ns | 1 | |
| 5 | TwTinH | Timer Input High Width | 2.0–3.6 | 3TpC | | | 1 | |
| 6 | TpTin | Timer Input Period | 2.0–3.6 | 8TpC | | | 1 | |
| 7 | TrTin,TfTin | Timer Input Rise and Fall Timers | 2.0–3.6 | | 100 | ns | 1 | |
| 8 | TwIL | Interrupt Request Low Time | 2.0<br>3.6 | 100<br>70 | | ns | 1, 2 | |
| 9 | TwIH | Interrupt Request Input High Time | 2.0–3.6 | 5TpC | | | 1, 2 | |
| 10 | Twsm | Stop Mode Recovery Width Spec | 2.0–3.6 | 12<br><br>10TpC | | ns | 3<br><br>4 | |
| 11 | Tost | Oscillator Start-Up Time | 2.0–3.6 | | 5TpC | | 4 | |
| 12 | Twdt | Watchdog Timer Delay Time | 2.0–3.6<br>2.0–3.6<br>2.0–3.6<br>2.0–3.6 | 5<br>10<br>20<br>80 | | ms<br>ms<br>ms<br>ms | | 0, 0<br>0, 1<br>1, 0<br>1, 1 |
| 13 | $T_{POR}$ | Power-on reset | 2.0–3.6 | 2.5 | 10 | ms | | |

**Notes**
1. Timing Reference uses 0.9 $V_{CC}$ for a logic 1 and 0.1 $V_{CC}$ for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR–D5 = 1.
4. SMR–D5 = 0.

| Device | Part Number | Description |
|---|---|---|
| | ZLP32300P2008G | 20-pin PDIP 8 K OTP |
| | ZLP32300S2008G | 20-pin SOIC 8 K OTP |
| | | |
| | ZLP32300H4804G | 48-pin SSOP 4 K OTP |
| | ZLP32300P4004G | 40-pin PDIP 4 K OTP |
| | ZLP32300H2804G | 28-pin SSOP 4 K OTP |
| | ZLP32300P2804G | 28-pin PDIP 4 K OTP |
| | ZLP32300S2804G | 28-pin SOIC 4 K OTP |
| | ZLP32300H2004G | 20-pin SSOP 4 K OTP |
| | ZLP32300P2004G | 20-pin PDIP 4 K OTP |
| | ZLP32300S2004G | 20-pin SOIC 4 K OTP |
| | | |
| | ZLP323ICE01ZAC* | 40-PDIP/48-SSOP Accessory Kit |
| | Note: *ZLP323ICE01ZAC has been replaced by an improved version, ZCRMZNICE02ZACG. | |
| | ZLP128ICE01ZEMG | In-Circuit Emulator |
| | Note: *ZLP128ICE01ZEMG has been replaced by an improved version, ZCRMZNICE01ZEMG. | |
| | ZCRMZNICE01ZEMG | Crimzon In-Circuit Emulator |
| | ZCRMZN00100KITG | Crimzon In-Circuit Emulator Development Kit |
| | ZCRMZNICE01ZACG | 20-Pin Accessory Kit |
| | ZCRMZNICE02ZACG | 40/48-Pin Accessory Kit |

**Notes**
1. Replace C with G for Lead-Free Packaging.
2. Contact www.zilog.com for the die form.

For fast results, contact your local Zilog® sales office for assistance in ordering the part(s) desired.

## O



## P



## R

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For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.