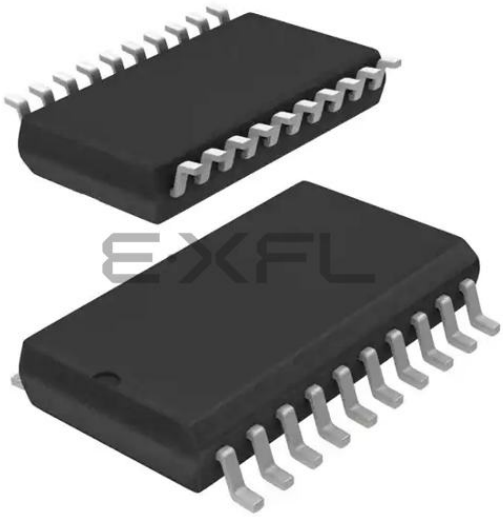

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zlp32300s2008c00tr

Architectural Overview

Zilog's Crimzon® ZLP32300 is an OTP-based member of the MCU family of infrared microcontrollers. With 237 B of general-purpose RAM and 8 KB to 32 KB of OTP, Zilog's CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Crimzon ZLP32300 architecture (see Figure 1 on page 3) is based on Zilog's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® CPU offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations:

1. Program Memory
2. Register File
3. Expanded Register File

The register file is composed of 256 Bytes of RAM. It includes four I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Crimzon ZLP32300 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2 on page 4). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

Note: *All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.*

Power connections use the conventional descriptions listed in Table 1.

Table 1. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

open-drain output with output logic as ONE, it is a floating port and reads back as ZERO. The following instruction sets P00-P07 all Low.

```
AND P0,#%F0
```

Port 0 (P00–P07)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 01 mode register (P01M). After a hardware reset or Stop Mode Recovery, Port 0 is configured as an input port.

An optional pull-up transistor is available as a OTP option bit on all Port 0 bits with nibble select.

Note: *The Port 0 direction is reset to be input following an SMR.*

Table 8. CTR1(0D)01h T8 and T16 Common Functions

Field	Bit Position		Value	Description
Mode	7-------	R/W	0*	TRANSMIT Mode
			1	DEMODULATION Mode
P36_Out/	-6------	R/W		TRANSMIT Mode
Demodulator_Input			0*	Port Output
			1	T8/T16 Output
				DEMODULATION Mode
			0*	P31
			1	P20
T8/T16_Logic/	--54----	R/W		TRANSMIT Mode
Edge _Detect			00**	AND
			01	OR
			10	NOR
			11	NAND
				DEMODULATION Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved
Transmit_Submode/	----32--	R/W		TRANSMIT Mode
Glitch_Filter			00*	Normal Operation
			01	PING-PONG Mode
			10	T16_Out = 0
			11	T16_Out = 1
				DEMODULATION Mode
			00*	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/	------1-			TRANSMIT Mode
Rising Edge		R/W	0*	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				DEMODULATION Mode
		R	0*	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

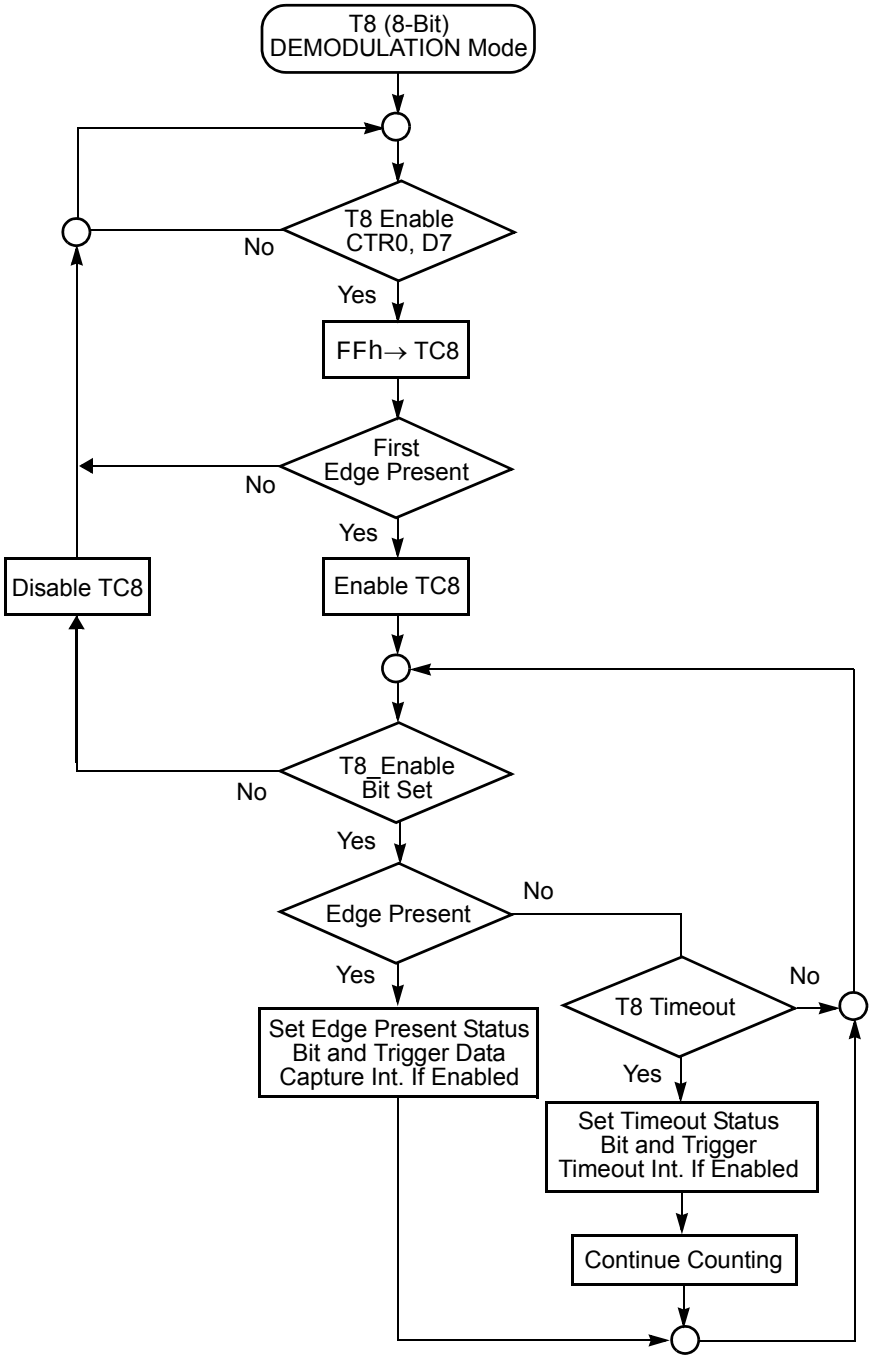


Figure 22. DEMODULATION Mode Flowchart

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

PING-PONG Mode

This operation mode is only valid in TRANSMIT mode. T8 and T16 must be programmed in SINGLE-PASS mode (CTR0, D6; CTR2, D6), and PING-PONG mode must be programmed in CTR1, D3; D2. You can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1, see Figure 26.

Note: *Enabling Ping-Pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status Flags before instituting this operation.*

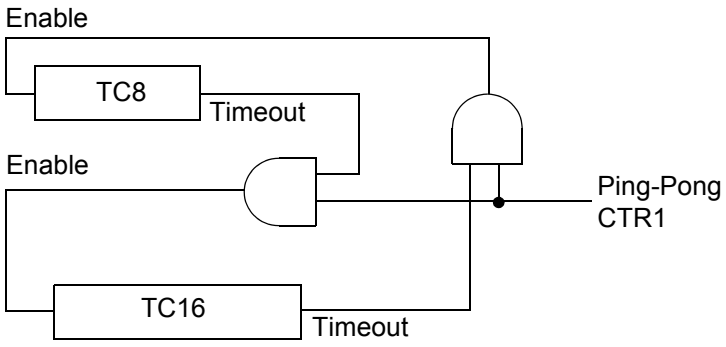


Figure 26. PING-PONG Mode Diagram

Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into SINGLE-PASS mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the PING-PONG mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7), see Figure 26.

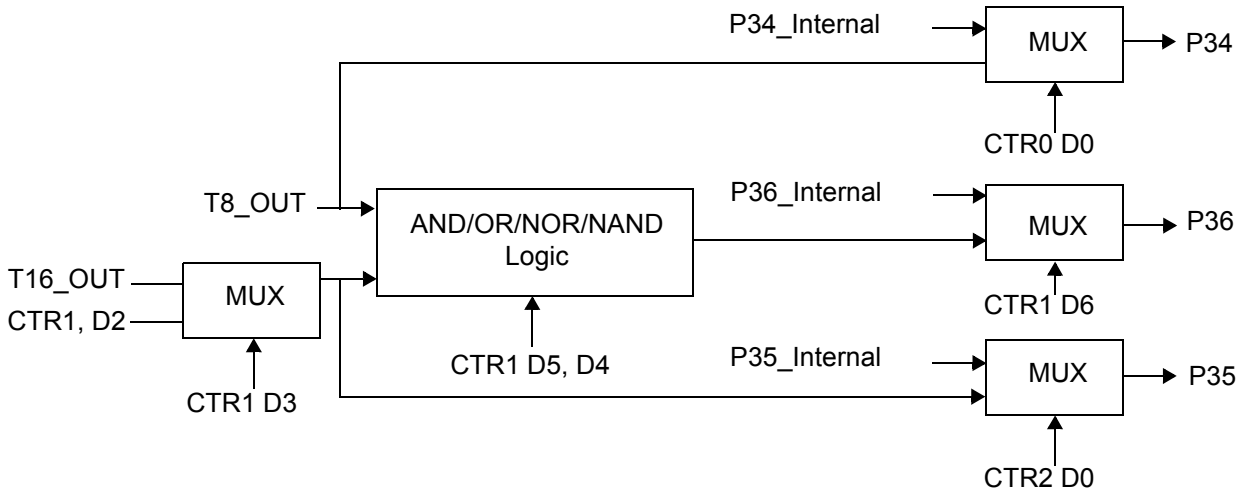


Figure 27. Output Circuit

The initial value of T8 or T16 must not be `1`. If you stop the timer and restart the timer, reload the initial value to avoid an unknown previous value.

During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

Timer Output

The output logic for the timers is displayed in Figure 27. P34 is used to output T8-OUT when D0 of CTR0 is set. P35 is used to output the value of TI6-OUT when D0 of CTR2 is set. When D6 of CTR1 is set, P36 outputs the logic combination of T8-OUT and T16-OUT determined by D5 and D4 of CTR1.

Interrupts

The Crimzon ZLP32300 features six different interrupts (see Table 11 on page 45). The interrupts are maskable and prioritized (see Figure 28). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the

For both resonator and crystal oscillator, the oscillation ground must go directly to the ground pin of the microcontroller. The oscillation ground must use the shortest distance from the microcontroller ground pin and it must be isolated from other connections.

Power Management

Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset timer function. The POR time allows V_{DD} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from V_{BO} Standby
- Stop Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop Mode Register determines whether the POR timer is bypassed after Stop Mode Recovery (typical for external clock).

HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

STOP Mode

This instruction turns OFF the internal clock and external crystal oscillation, reducing the standby current to 10 µA or less. STOP mode is terminated only by a reset, such as WDT time-out, POR or SMR. This condition causes the processor to restart the application program at address 000Ch. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFh) immediately before the appropriate sleep instruction, as follows:

```
FF          NOP         ; clear the pipeline
6F          STOP        ; enter Stop Mode
```

or

```
FF          NOP         ; clear the pipeline
7F          HALT        ; enter HALT Mode
```

Voltage Detection and Flags

The Voltage Detection register (LVD, register 0Ch at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the V_{CC} level is monitored in real time. The HVD Flag (bit 2 of the LVD register) is set only if V_{CC} is higher than $V_{HVD.}$ The LVD Flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD}. When Voltage Detection is enabled, the LVD Flag also triggers IRQ5. The IRQ bit 5 latches the low-voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a Flag only.

Note: *If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt (EI) instruction prior to enabling the voltage detection.*

Notes:

1. *Ensure to differentiate the TRANSMIT mode from DEMODULATION mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.*
2. *Changing from one mode to another cannot be performed without disabling the counter/timers.*

CTR2(0D)02H

D7	D6	D5	D4	D3	D2	D1	D0

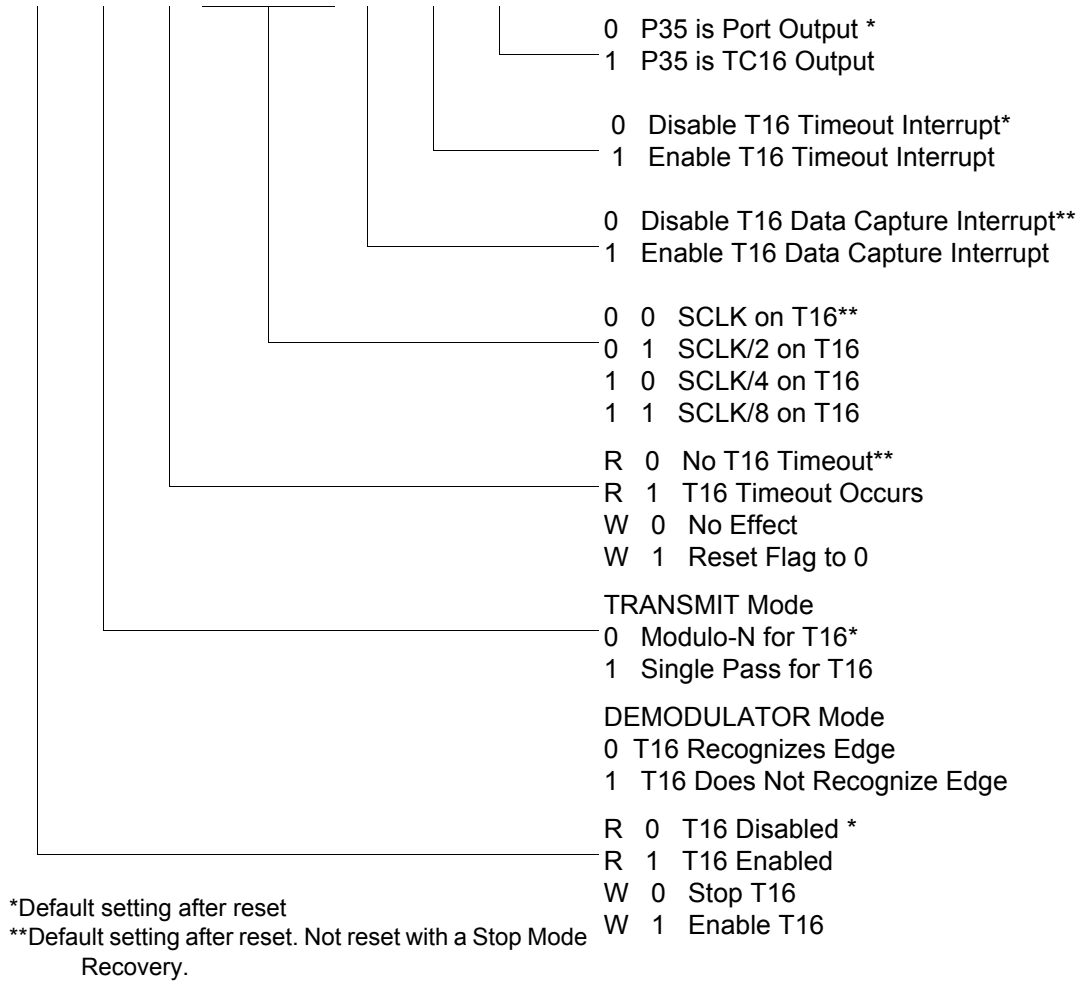
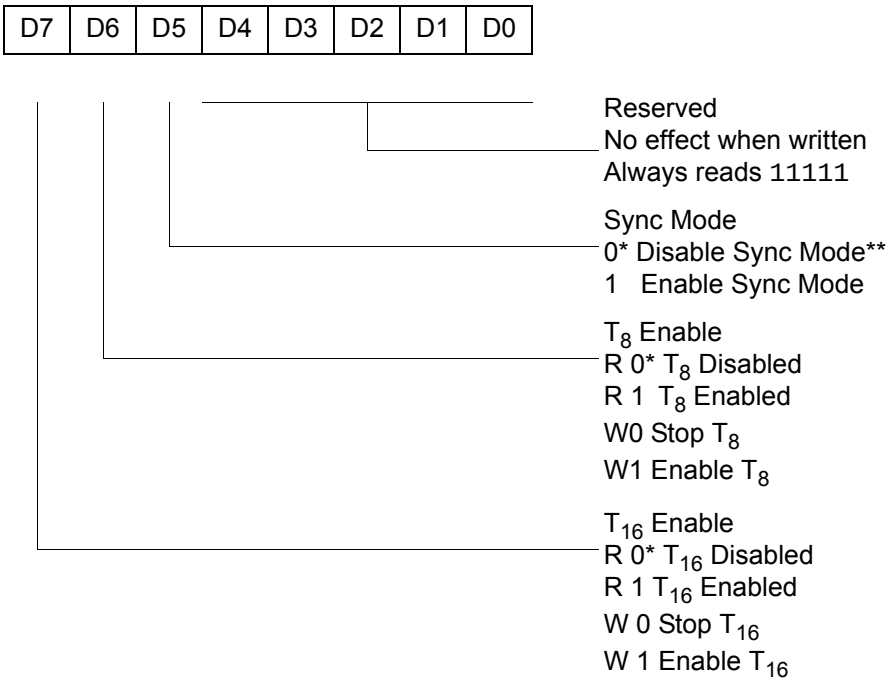


Figure 39. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)

CTR3(0D)03H

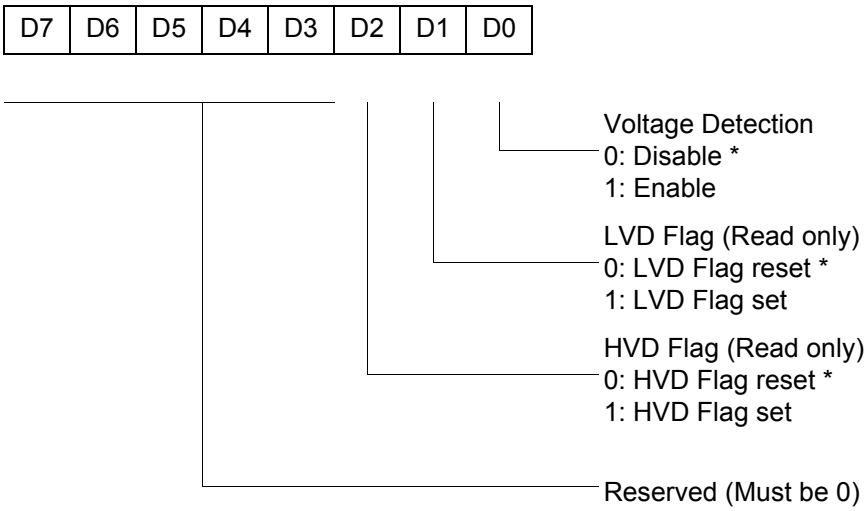


*Default setting after reset.
**Default setting after reset. Not reset with a Stop Mode Recovery.

Figure 40. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)

Note: *If Sync Mode is enabled, the first pulse of T8 carrier is always synchronized with T16 (demodulated signal). It can always provide a full carrier pulse.*

LVD(0D)0CH



*Default setting after reset.

Figure 41. Voltage Detection Register

Note: *Do not modify register P01M while checking a low-voltage condition. Switching noise of both Ports 0 and 1 together might trigger the LVD Flag.*

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are displayed in Figure 42 through Figure 55 on page 74.

PCON(0F)00H

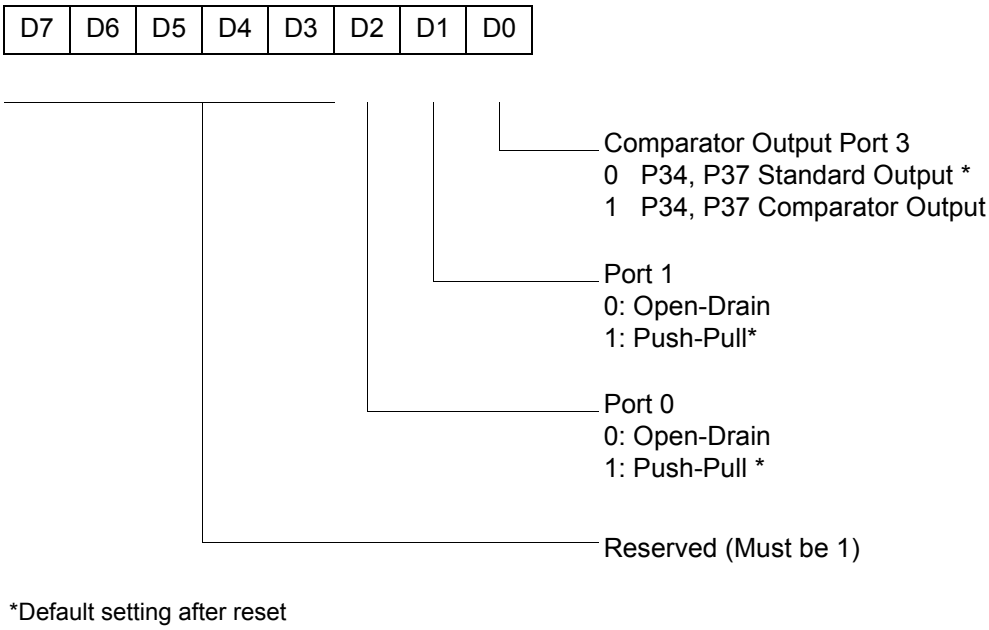
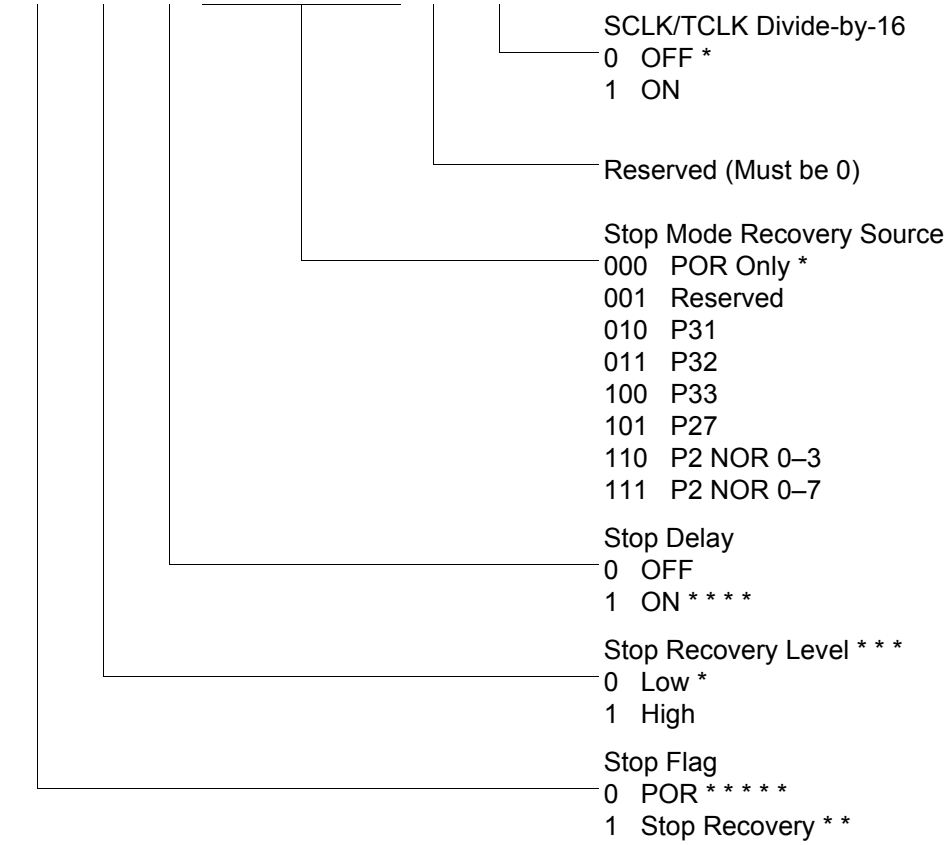


Figure 42. Port Configuration Register (PCON)(0F)00H: Write Only)

SMR(0F)0BH

D7	D6	D5	D4	D3	D2	D1	D0



*Default setting after Reset
* *Set after Stop Mode Recovery
* * *At the XOR gate input
* * * *Default setting after Reset. Must be 1 if using a crystal or resonator clock source.
* * * * *Default setting after Power-On Reset. Not Reset with a Stop Mode Recovery.

Figure 43. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)

R249 IPR(F9H)

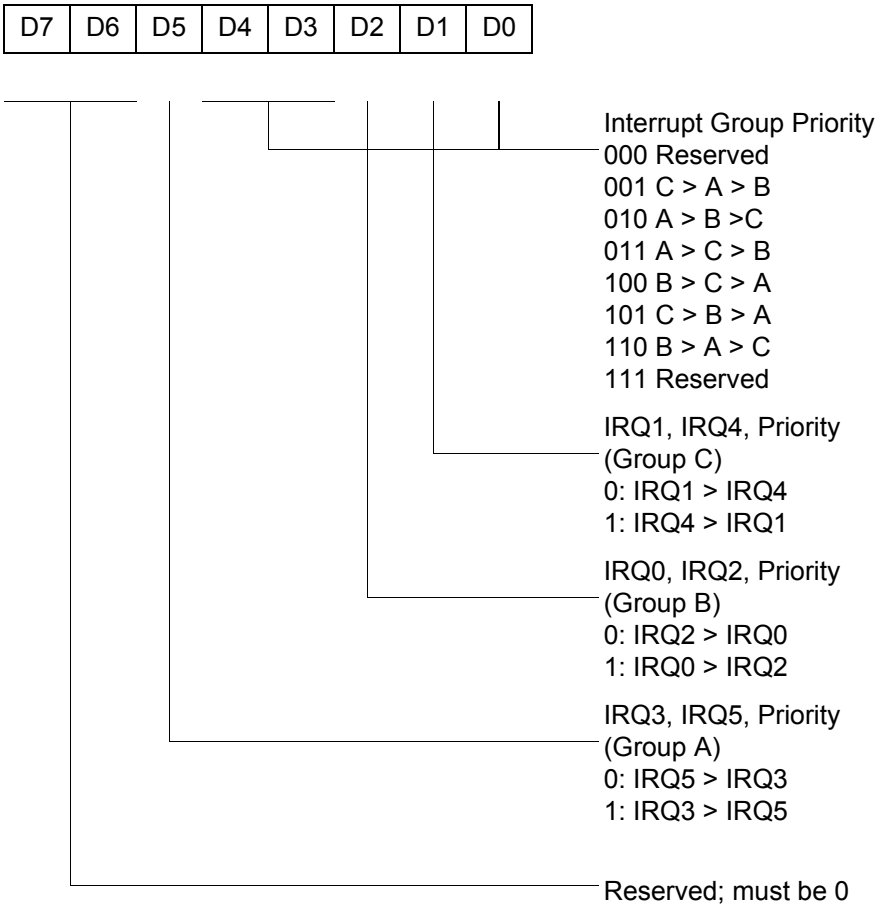


Figure 49. Interrupt Priority Register (F9H: Write Only)

R252 Flags(FCH)

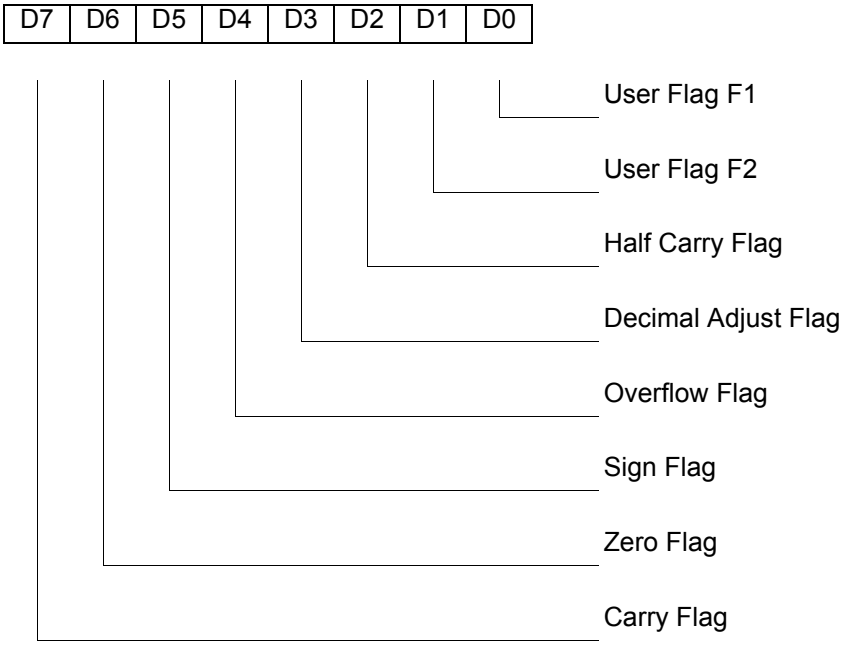
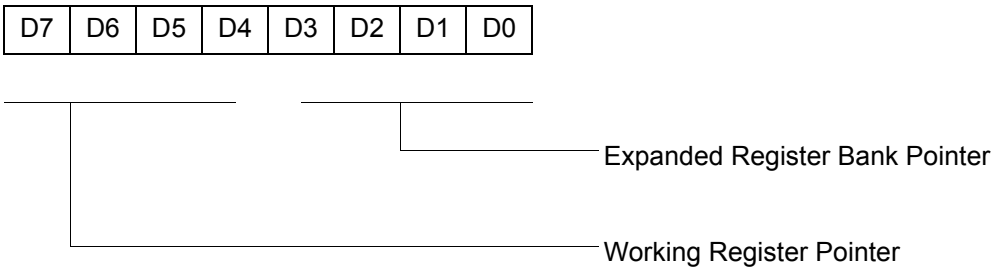


Figure 52. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 53. Register Pointer (FDH: Read/Write)

Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than those listed in Table 18 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 17. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	0	+70	C	
Storage temperature	–65	+150	C	
Voltage on any pin with respect to V_{SS}	–0.3	+5.5	V	1
Voltage on V_{DD} pin with respect to V_{SS}	–0.3	+3.6	V	
Maximum current on input and/or inactive output pin	–5	+5	µA	
Maximum output current from active output pin	–25	+25	mA	
Maximum current into V_{DD} or out of V_{SS}		75	mA	

[1]This voltage applies to all pins except the following: V_{DD}, P32, P33 and $\overline{\text{RESET}}$.

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 56).

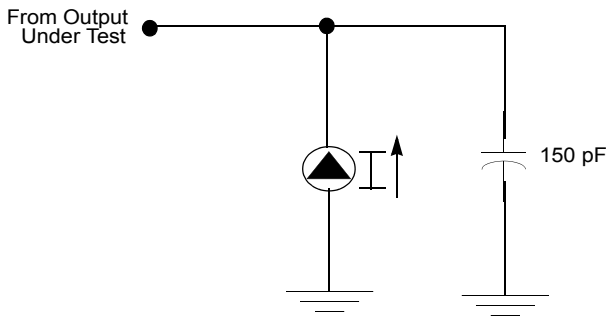


Figure 56. Test Load Diagram

Capacitance

Table 18 lists the capacitances.

Table 18. Capacitance

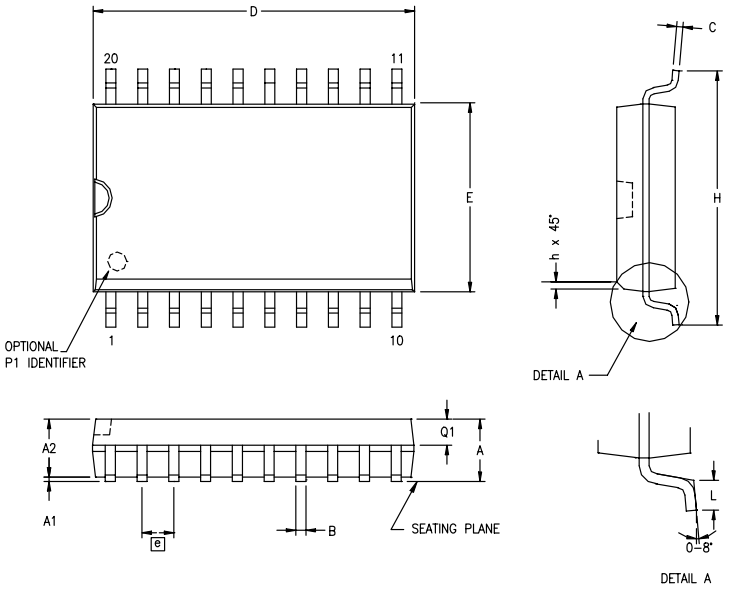
Parameter	Maximum
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF
T_A = 25 °C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND	

DC Characteristics

Table 19 describes the DC characteristics.

Table 19. DC Characteristics

			T_A= 0 °C to +70 °C					
Symbol	Parameter	V_{CC}	Min	Typ(7)	Max	Units	Conditions	Notes
V_{CC}	Supply Voltage		2.0		3.6	V	See Notes	5
V_{CH}	Clock Input High Voltage	2.0-3.6	0.8 V_{CC}		V_{CC}+0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-3.6	V_{SS}–0.3		0.4	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-3.6	0.7 V_{CC}		V_{CC}+0.3	V		
V_{IL}	Input Low Voltage	2.0-3.6	V_{SS}–0.3		0.2 V_{CC}	V		
V_{OH1}	Output High Voltage	2.0-3.6	V_{CC}–0.4			V	I_{OH} = –0.5 mA	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-3.6	V_{CC}–0.8			V	I_{OH} = –7 mA	
V_{OL1}	Output Low Voltage	2.0-3.6			0.4	V	I_{OL} = 4.0 mA	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-3.6			0.8	V	I_{OL} = 10 mA	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-3.6			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-3.6	0		V_{CC} -1.75	V		



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	**.496**	.510
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 59. 20-Pin SOIC Package Diagram

Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.