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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlp32300s2808c

Table 5. 40- and 48-Pin Configuration (Continued)

40-Pin PDIP No	48-Pin SSOP No	Symbol
32	39	P12
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	$\overline{\text{RESET}}$
15	18	XTAL1
14	17	XTAL2
11	12, 13	V_{DD}
31	24, 37, 38	V_{SS}
25	29	Pref1/P30
	48	NC
	6	NC

(see T8 and T16 Common Functions—CTR1(0D)01h on page 28). Other edge detect and IRQ modes are described in Table 6.

Note: *Comparators are powered down by entering STOP mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into DIGITAL mode.*

Table 6. Port 3 Pin Function Summary

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	T8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 11). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

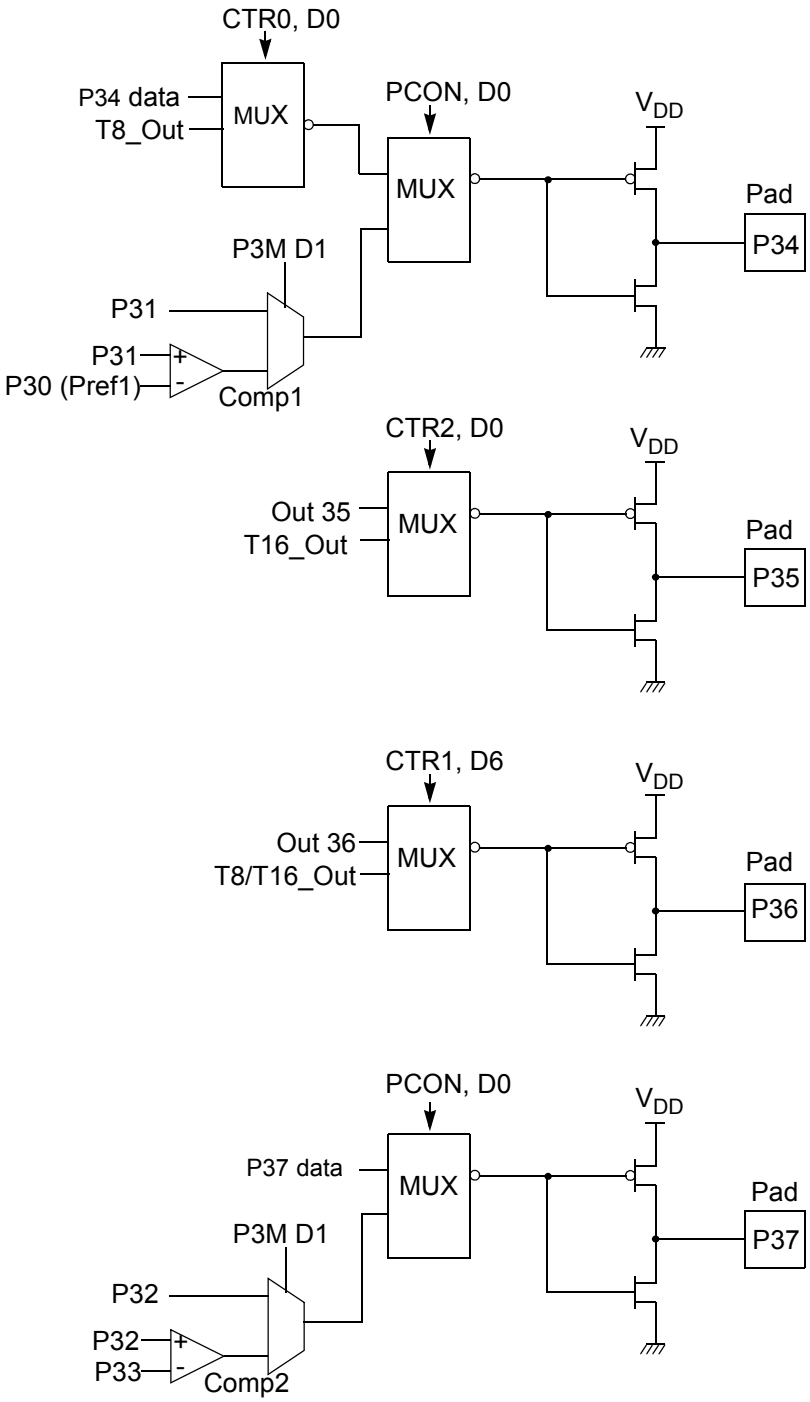


Figure 11. Port 3 Counter/Timer Output Configuration

```
LD                      R1, 2                   ; CTR2→CTR1

LD                      RP, #0Dh                ; Select ERF D
for access to bank D
                                                ; (working
register group 0)
LD                      RP, #7Dh                ; Select
expanded register bank D and working            ; register
group 7 of bank 0 for access.
LD                      71h, 2
; CTRL2→register 71h
LD                      R1, 2
; CTRL2→register 71h
```

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 7 on page 27) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (see Figure 15). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note: *Working register group E0–EF can only be accessed through working registers and indirect addressing modes.*

Counter/Timer8 High Hold Register—TC8H(D)05h

Field	Bit Position		Description
T8_Level_HI	[7:0]	R/W	Data

Counter/Timer8 Low Hold Register—TC8L(D)04h

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

CTR0 Counter/Timer8 Control Register—CTR0(D)00h

Table 7 lists and briefly describes the fields for this register.

Table 7. CTR0(D)00h Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R/W	0* 1 0 1	Counter Disabled Counter Enabled Stop Counter Enable Counter
Single/Modulo-N	-6-------	R/W	0* 1	Modulo-N Single Pass
Time_Out	--5------	R/W	0** 1 0 1	No Counter Time-Out Counter Time-Out Occurred No Effect Reset Flag to 0
T8 _Clock	---43---	R/W	0 0** 0 1 1 0 1 1	SCLK SCLK/2 SCLK/4 SCLK/8
Capture_INT_Mask	-----2--	R/W	0** 1	Disable Data Capture Interrupt Enable Data Capture Interrupt
Counter_INT_Mask	------1-	R/W	0** 1	Disable Time-Out Interrupt Enable Time-Out Interrupt
P34_Out	-------0	R/W	0* 1	P34 as Port Output T8 Output on P34

*Indicates the value upon Power-On Reset.
**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0, D5) is set, and a time-out interrupt can be generated if it is enabled (CTR0, D1). In MODULO-N mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the time-out status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle, see Figure 18.

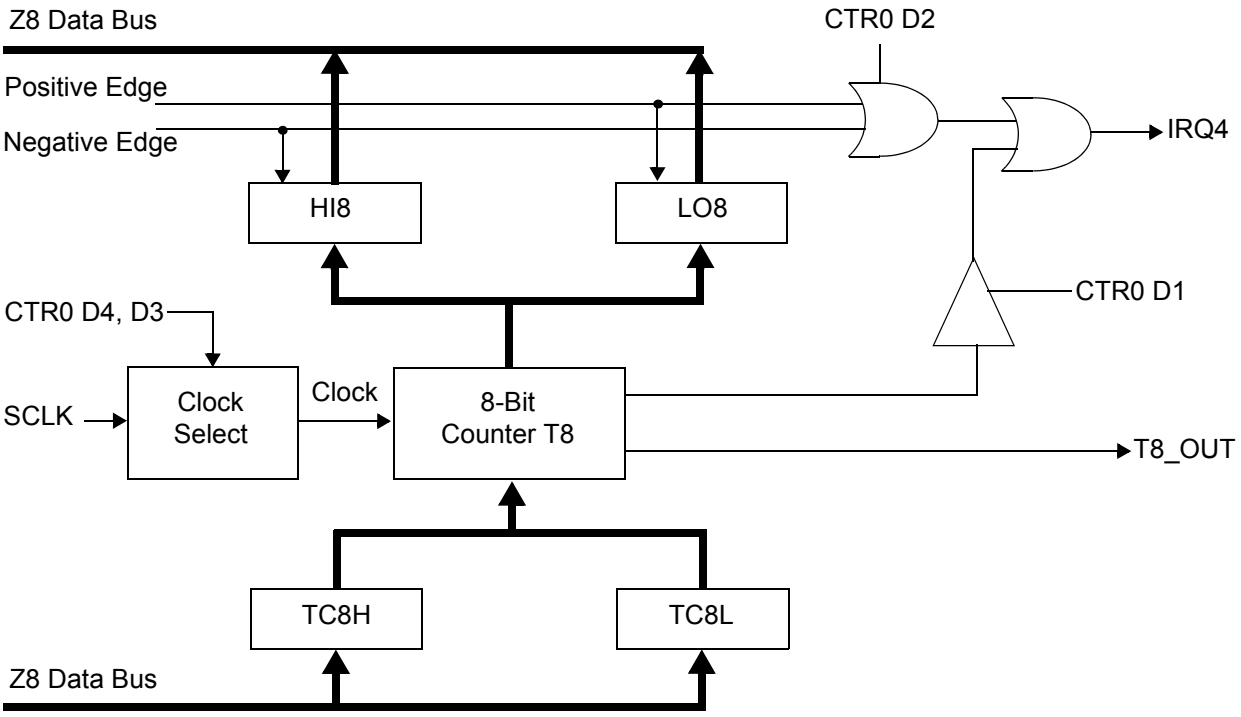


Figure 18. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.

Caution: *To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to* FFh *to* FEh.

Note: *The letter* h *denotes hexadecimal values.*

Transition from 0 to FFh is not a timeout condition.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

PING-PONG Mode

This operation mode is only valid in TRANSMIT mode. T8 and T16 must be programmed in SINGLE-PASS mode (CTR0, D6; CTR2, D6), and PING-PONG mode must be programmed in CTR1, D3; D2. You can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1, see Figure 26.

Note: *Enabling Ping-Pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status Flags before instituting this operation.*

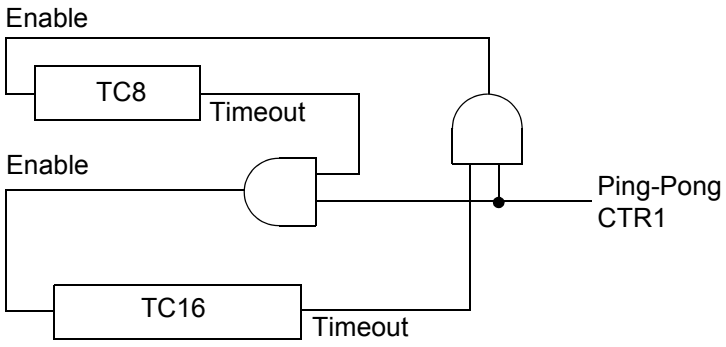


Figure 26. PING-PONG Mode Diagram

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (see Figure 32). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.

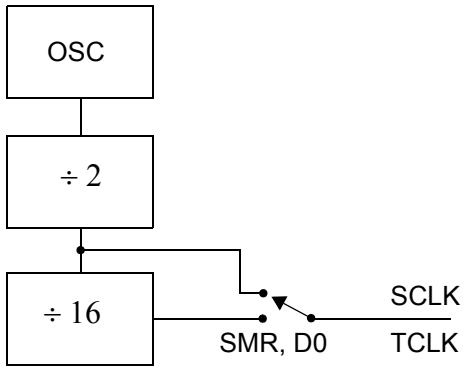


Figure 32. SCLK Circuit

Stop Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (see Figure 33 and Table 14).

Stop Mode Recovery Register 2—SMR2(F)0Dh

Table 13 lists and briefly describes the fields for this register.

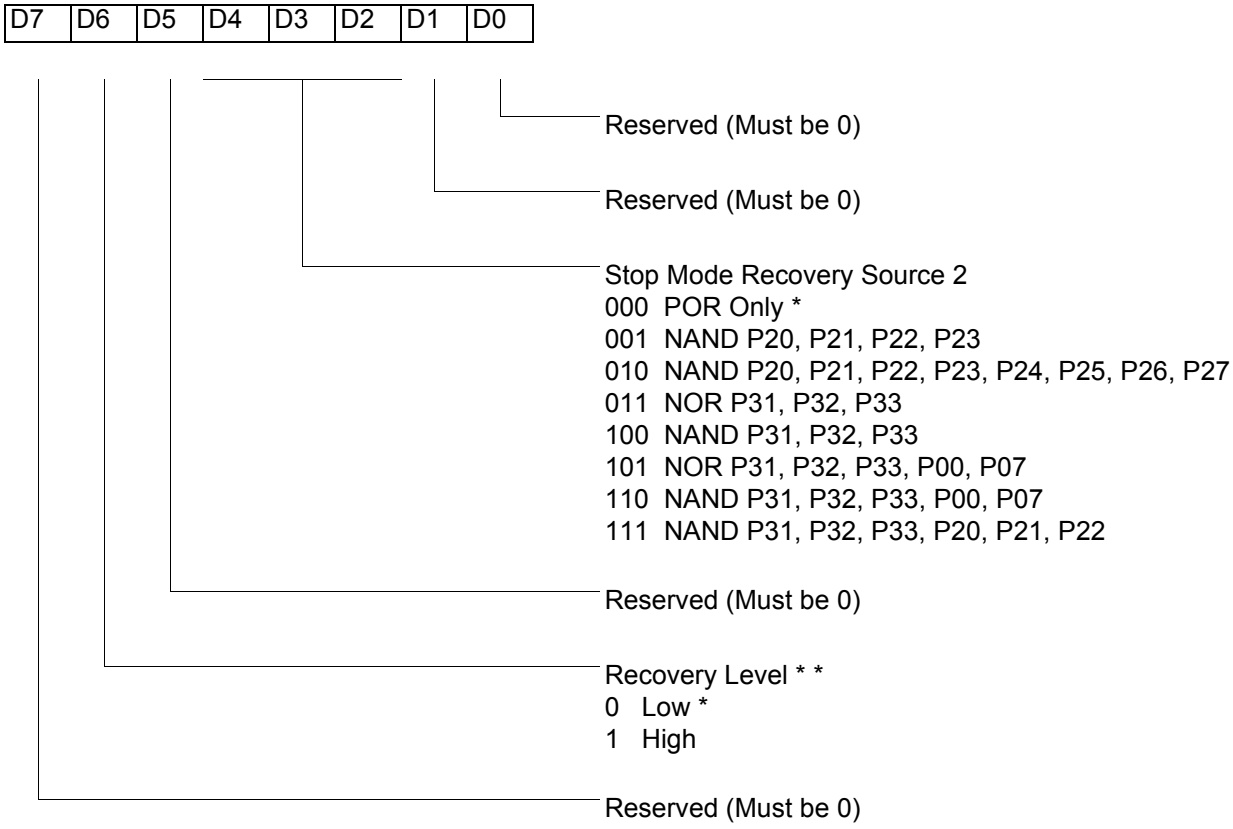
Table 13. SMR2(F)0Dh:Stop Mode Recovery Register 2*

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0†	Low
			1	High
Reserved	--5-----		0	Reserved (Must be 0)

Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (see Figure 34).

SMR2(0F)Dh



If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.
*Default setting after reset.
* *At the XOR gate input.

Figure 34. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

Note: *Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.*

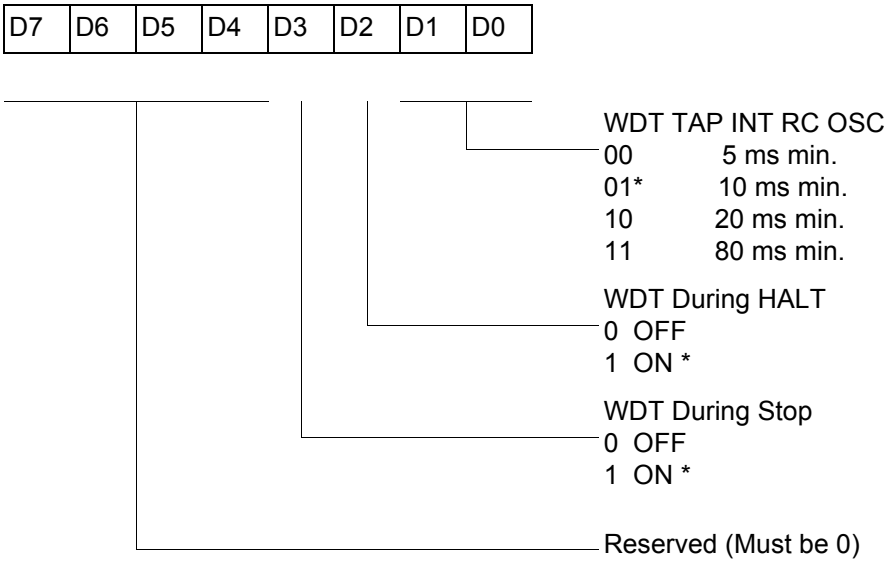
Watchdog Timer Mode

Watchdog Timer Mode Register (WDTMR)

The Watchdog Timer is a retriggerable one-shot timer that resets the Z8® if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) Flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum time-out period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (see Figure 35). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-on reset, Watchdog Reset, or a Stop Mode Recovery (see Figure 34). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 35.

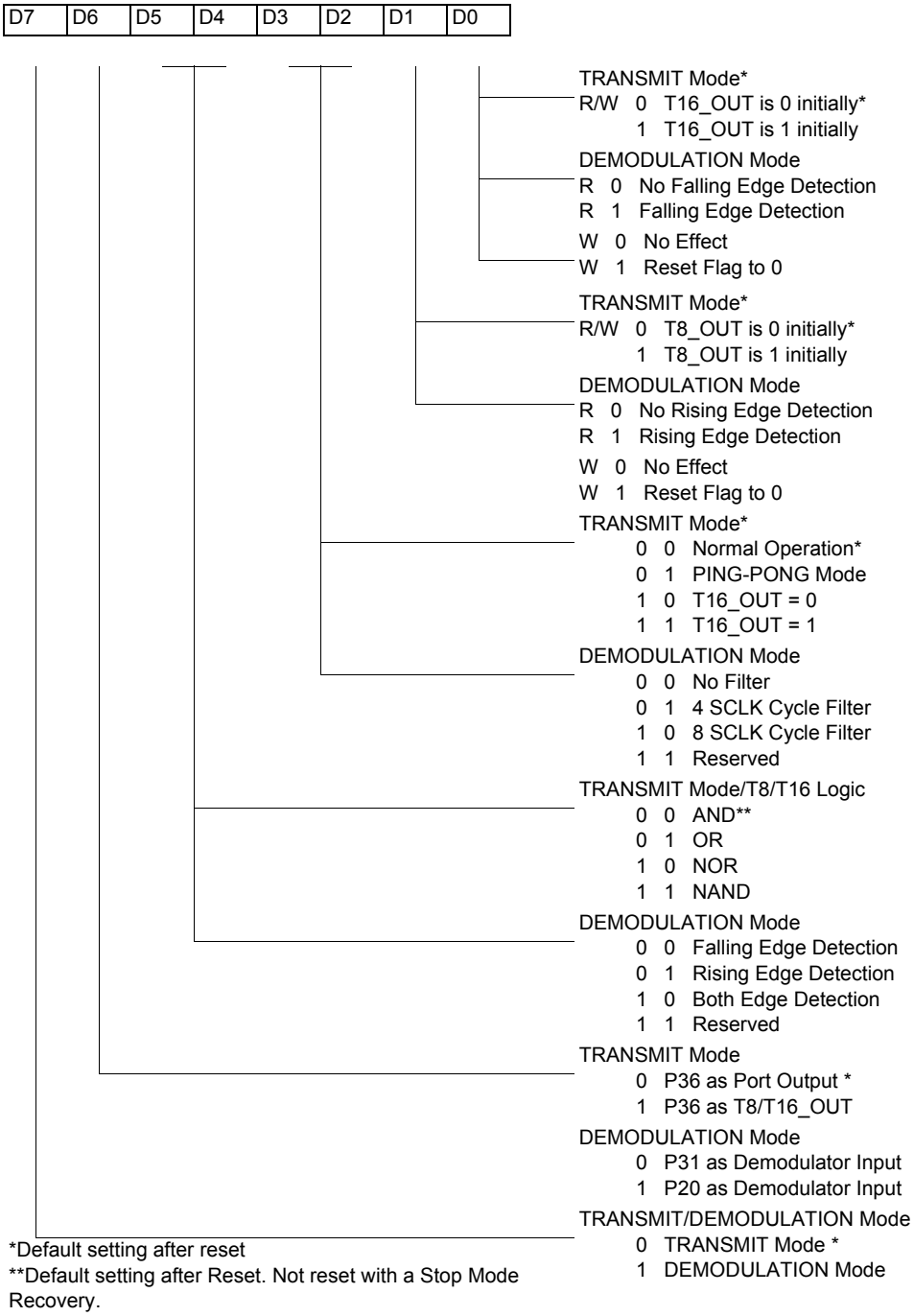
WDTMR(0F)0Fh



*Default setting after reset

Figure 35. Watchdog Timer Mode Register (Write Only)

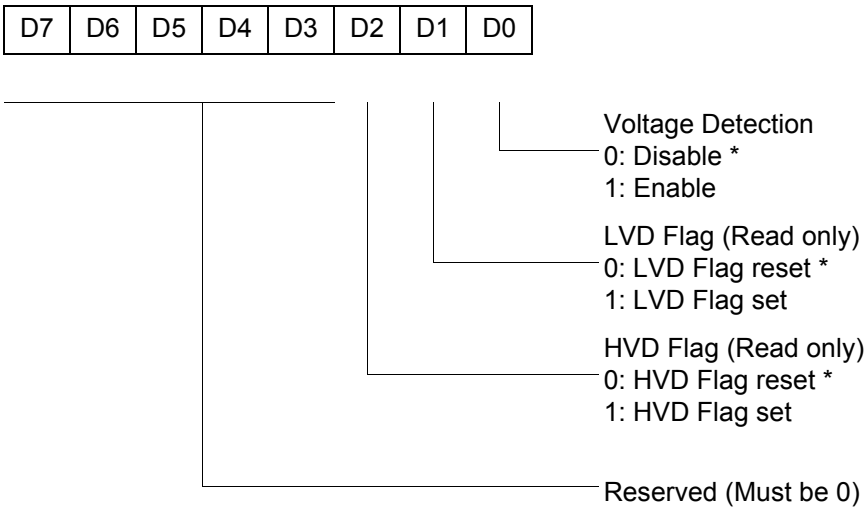
CTR1(0D)01H



*Default setting after reset
**Default setting after Reset. Not reset with a Stop Mode Recovery.

Figure 38. T8 and T16 Common Control Functions ((0D)01H: Read/Write)

LVD(0D)0CH



*Default setting after reset.

Figure 41. Voltage Detection Register

Note: *Do not modify register P01M while checking a low-voltage condition. Switching noise of both Ports 0 and 1 together might trigger the LVD Flag.*

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are displayed in Figure 42 through Figure 55 on page 74.

PCON(0F)00H

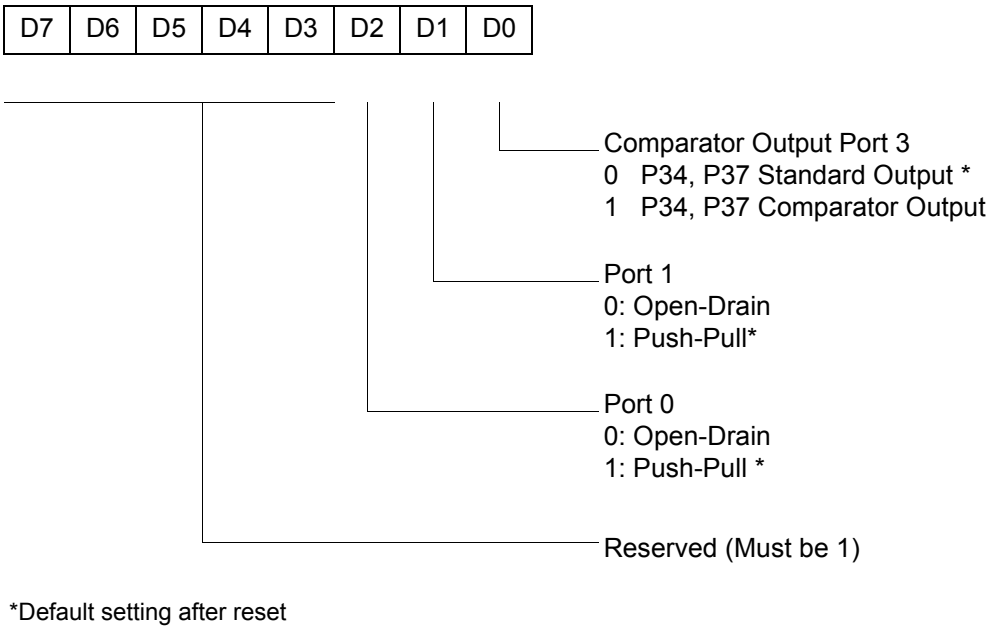
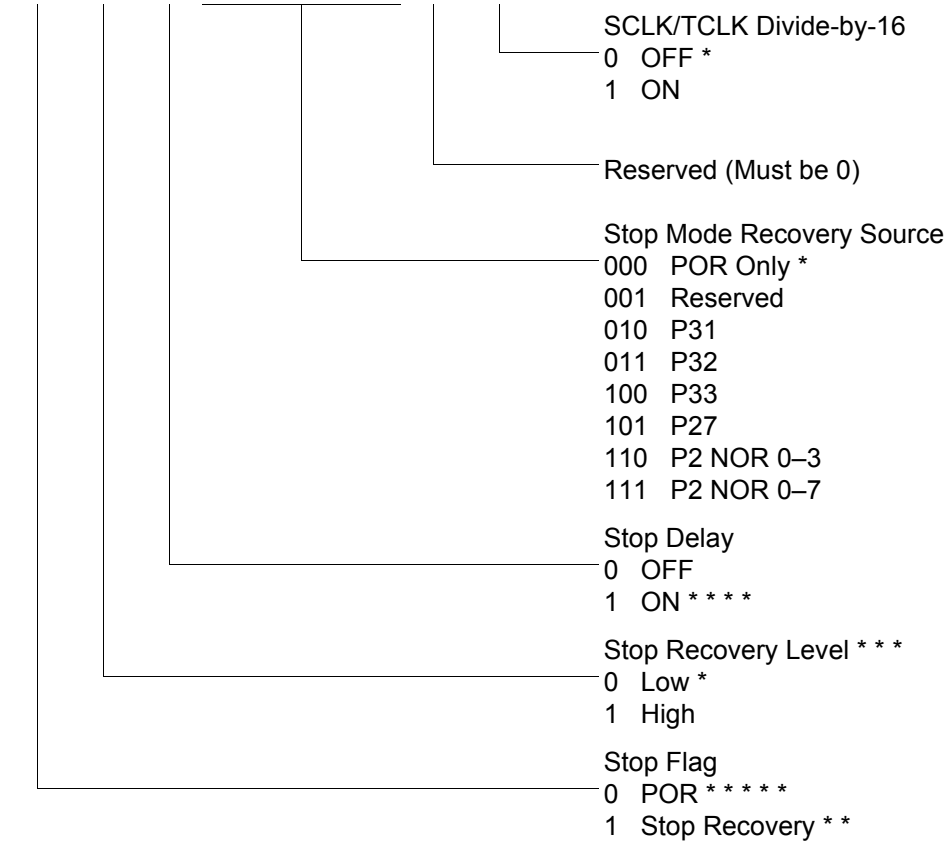


Figure 42. Port Configuration Register (PCON)(0F)00H: Write Only)

SMR(0F)0BH

D7	D6	D5	D4	D3	D2	D1	D0



*Default setting after Reset
* *Set after Stop Mode Recovery
* * *At the XOR gate input
* * * *Default setting after Reset. Must be 1 if using a crystal or resonator clock source.
* * * * *Default setting after Power-On Reset. Not Reset with a Stop Mode Recovery.

Figure 43. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)

Standard Control Registers

The standard control registers are displayed in Figure 46 through Figure 55 on page 74.

R246 P2M(F6H)

D7	D6	D5	D4	D3	D2	D1	D0

P27–P20 I/O Definition
0 Defines bit as OUTPUT
1 Defines bit as INPUT *

*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 46. Port 2 Mode Register (F6H: Write Only)

R247 P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0

0: Port 2 Open Drain *
1: Port 2 Push-Pull

0= P31, P32 DIGITAL Mode*
1= P31, P32 ANALOG Mode

Reserved (Must be 0)

*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 47. Port 3 Mode Register (F7H: Write Only)

R249 IPR(F9H)

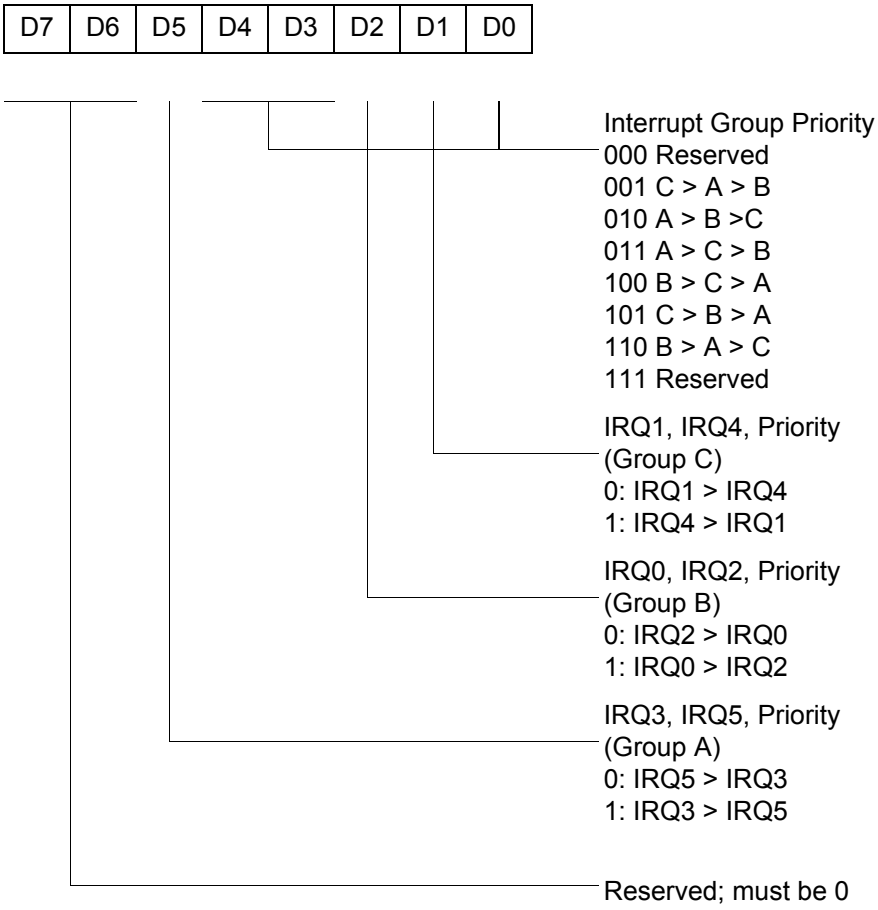


Figure 49. Interrupt Priority Register (F9H: Write Only)

AC Characteristics

Figure 57 and Table 20 describe the Alternating Current (AC) characteristics.

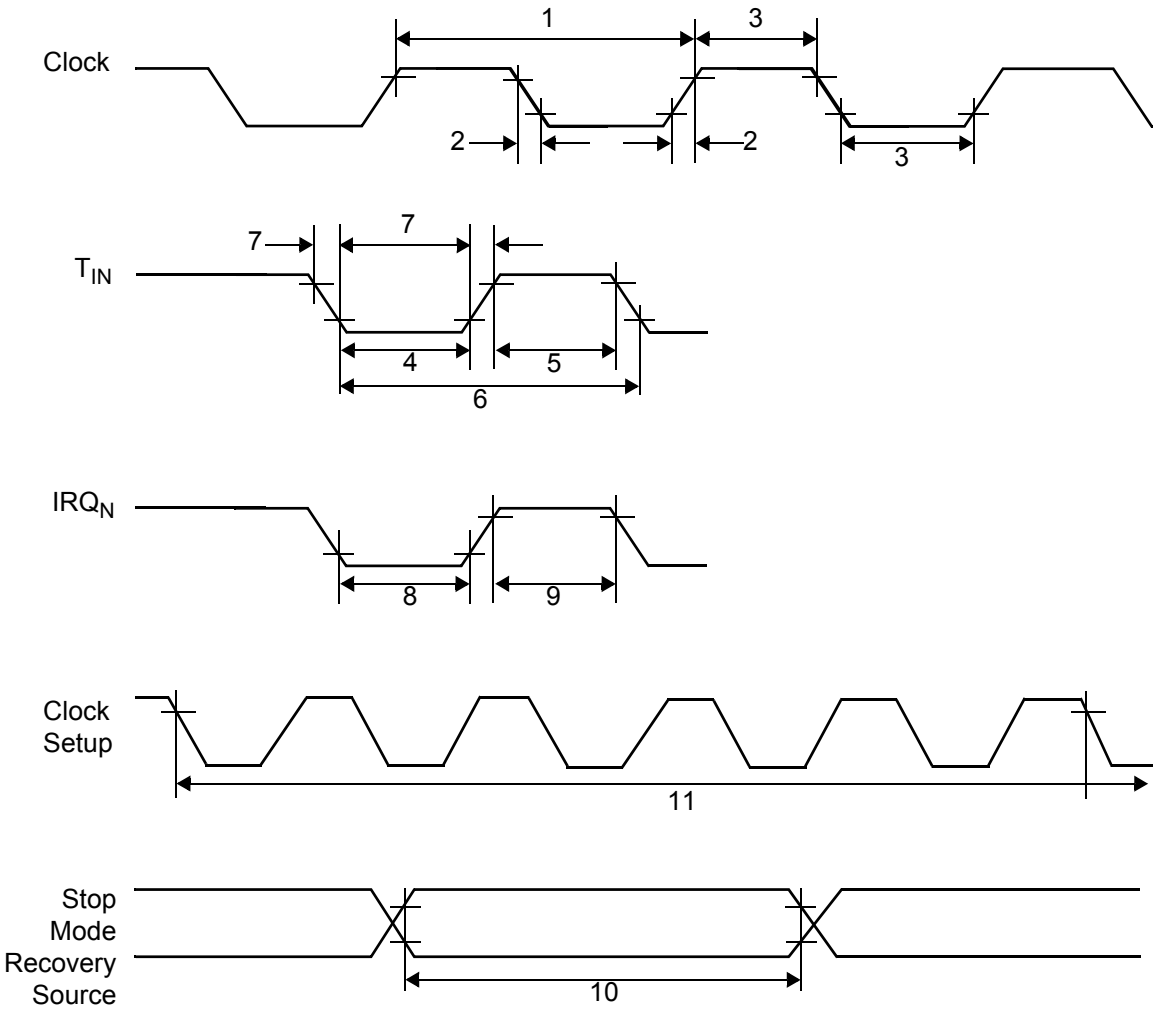
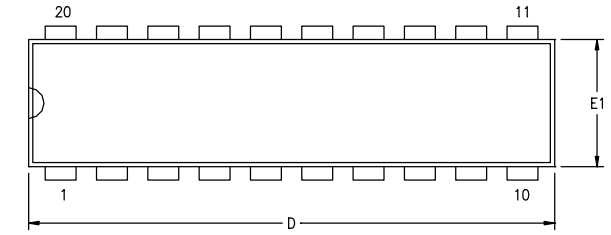


Figure 57. AC Timing Diagram

Packaging

Package information for all versions of Crimzon ZLP32300 is displayed in Figure 58 through Figure 65.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	0.81	.015	.032
A2	3.25	3.68	.128	.145
B	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
e	2.54 BSC		.100 BSC	
eA	7.87	9.14	.310	.360
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

CONTROLLING DIMENSIONS : INCH

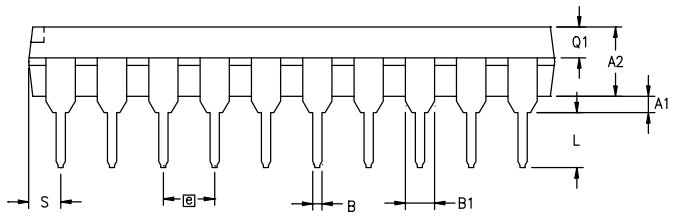
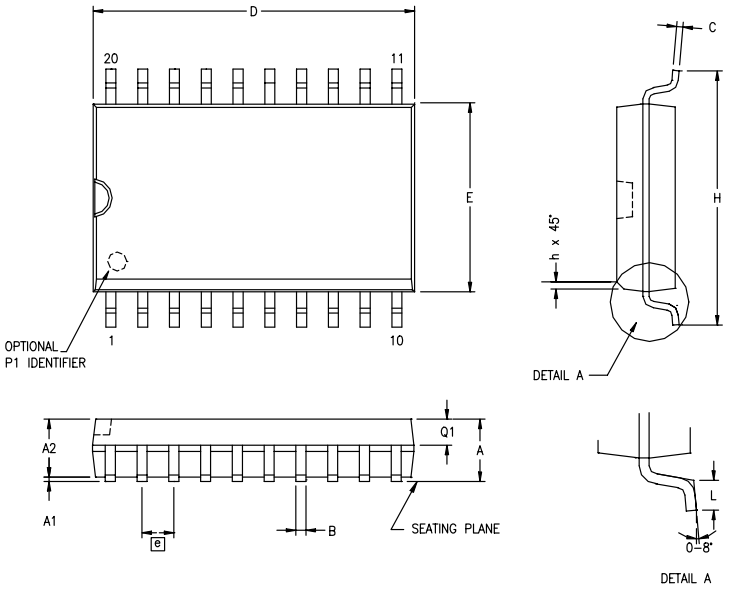


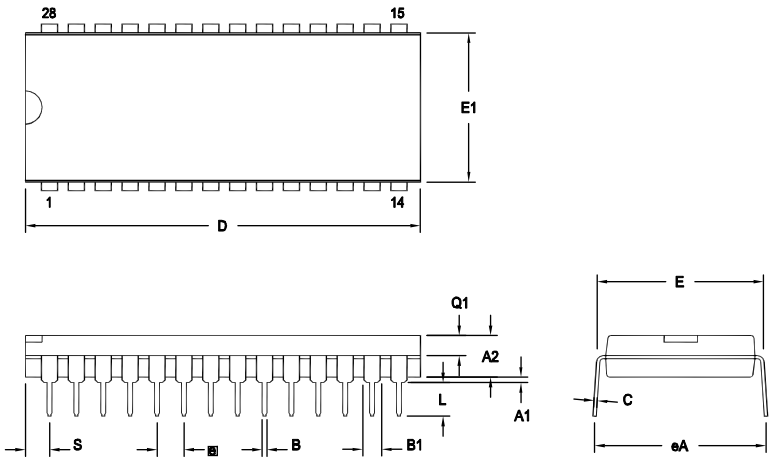
Figure 58. 20-Pin PDIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	**.496**	.510
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 59. 20-Pin SOIC Package Diagram



SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 BSC	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Note: ZiLOG supplies both options for production. Component layout PCB design should cover bigger option 01.

Figure 62. 28-Pin PDIP Package Diagram