#### Zilog - ZLP32300S2808C00TR Datasheet





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#### Details

Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zlp32300s2808c00tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



- EPROM Protection
- WDT enabled at POR

## **Functional Block Diagram**

Figure 1 displays the Crimzon ZLP32300 MCU functional block diagram.



Note: Refer to the specific package for available pins.

### Figure 1. Crimzon ZLP32300 MCU Functional Block Diagram

Crimzon<sup>®</sup> ZLP32300 Product Specification

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Pin No	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5, 6, 7
4-7	P04-P07	Input/Output	Port 0, Bits 4, 5, 6, 7
8	V <sub>DD</sub>		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1, 2, 3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30	Input	Analog ref input; connect to
	Port 3 Bit 0		V <sub>CC</sub> if not used
			Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0, 1, 2
22	V <sub>SS</sub>		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0–4

Table 4. 28-Pin PDIP/SOIC/SSOP Pin Identification



40-Pin PDIP No	48-Pin SSOP No	Symbol
32	39	P12
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V <sub>DD</sub>
31	24, 37, 38	V <sub>SS</sub>
25	29	Pref1/P30
	48	NC
	6	NC

### Table 5. 40- and 48-Pin Configuration (Continued)



open-drain output with output logic as ONE, it is a floating port and reads back as ZERO. The following instruction sets P00-P07 all Low.

AND P0,#%F0

#### Port 0 (P00–P07)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or opendrain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 01 mode register (P01M). After a hardware reset or Stop Mode Recovery, Port 0 is configured as an input port.

An optional pull-up transistor is available as a OTP option bit on all Port 0 bits with nibble select.

**Note:** *The Port 0 direction is reset to be input following an SMR.* 





Figure 10. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The Analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20





Figure 11. Port 3 Counter/Timer Output Configuration



# **Functional Description**

This device incorporates special functions to enhance the Z8 functionality in consumer and battery-operated applications.

## **Program Memory**

This device addresses 32 KB of OTP memory. The first 12 bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts. See Figure 12.

#### RAM

This device features 256 B of RAM.

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Figure 13. Expanded Register File Architecture

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## Table 8. CTR1(0D)01h T8 and T16 Common Functions

Field	Bit Position		Value	Description
Mode	7	R/W	0*	TRANSMIT Mode
			1	DEMODULATION Mode
P36_Out/	-б	R/W		TRANSMIT Mode
Demodulator_Input			0*	Port Output
			1	T8/T16 Output
				DEMODULATION Mode
			0*	P31
			1	P20
T8/T16_Logic/	54	R/W		TRANSMIT Mode
Edge _Detect			00**	AND
			01	OR
			10	NOR
			11	NAND
				DEMODULATION Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved
Transmit_Submode/	32	R/W		TRANSMIT Mode
Glitch_Filter			00*	Normal Operation
			01	PING-PONG Mode
			10	T16_Out = 0
			11	T16_Out = 1
				DEMODULATION Mode
			00*	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/	1-			TRANSMIT Mode
Rising Edge		R/W	0*	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				DEMODULATION Mode
		R	0*	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0



#### SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (see Figure 32). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.



Figure 32. SCLK Circuit

#### Stop Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (see Figure 33 and Table 14).

#### Stop Mode Recovery Register 2—SMR2(F)0Dh

Table 13 lists and briefly describes the fields for this register.

Fable 13. SMR2(F)0Dh:Stop	Mode Recovery	Register 2*
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Field	Bit Position	Value	Description
Reserved	7	0	Reserved (Must be 0)
Recovery Level	-6 W	0 <sup>†</sup> 1	Low High
Reserved	5	0	Reserved (Must be 0)





Figure 33. Stop Mode Recovery Source





#### Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (see Figure 34).

SMR2(0F)Dh

D7	D6	D5	D4	D3	D2	D1	D0	
								Reserved (Must be 0) Reserved (Must be 0) Stop Mode Recovery Source 2 000 POR Only * 001 NAND P20, P21, P22, P23 010 NAND P20, P21, P22, P23, P24, P25, P26, P27 011 NOR P31, P32, P33 100 NAND P31, P32, P33 101 NOR P31, P32, P33, P00, P07 110 NAND P31, P32, P33, P00, P07
								<ul> <li>111 NAND P31, P32, P33, P20, P21, P22</li> <li>Reserved (Must be 0)</li> <li>Recovery Level * *</li> <li>0 Low *</li> <li>1 High</li> </ul>
								Reserved (Must be 0)

If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.

\*Default setting after reset.

\* \*At the XOR gate input.

### Figure 34. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

**Note:** Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.



#### CTR3(0D)03H



\*\*Default setting after reset. Not reset with a Stop Mode Recovery.

#### Figure 40. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)

**Note:** If Sync Mode is enabled, the first pulse of T8 carrier is always synchronized with T16 (demodulated signal). It can always provide a full carrier pulse.



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## **Standard Control Registers**

The standard control registers are displayed in Figure 46 through Figure 55 on page 74. R246 P2M(F6H)



\*Default setting after reset. Not Reset with a Stop Mode Recovery.



#### R247 P3M(F7H)



\*Default setting after reset. Not Reset with a Stop Mode Recovery.

#### Figure 47. Port 3 Mode Register (F7H: Write Only)



## **AC Characteristics**

Figure 57 and Table 20 describe the Alternating Current (AC) characteristics.















Note: ZiLOG supplies both options for production. Component layout PCB design should cover bigger option 01.







Figure 65. 48-Pin SSOP Package Design

**Note:** Contact  $Zilog^{\mathbb{R}}$  on the actual bonding diagram and coordinate for chip-on-board assembly.





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