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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, HLVD, POR, WDT |
| Number of I/O | 24 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 28-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/zlp32300s2816c |

# Revision History

Each instance in the Revision History table reflects a change to this document from its previous revision. For more details, refer to the corresponding pages or appropriate link in the table.

| Date | Revision Level | Description | Page Number |
|---|---|---|---|
| February 2008 | 23 | Updated Ordering Information section. | 87 |
| January 2008 | 22 | Updated Ordering Information section. | 87 |
| July 2007 | 21 | Updated Disclaimer section and implemented style guide. | All |
| February 2007 | 20 | Updated Low-Voltage Detection. | 58 |
| May 2006 | 19 | Updated Figure 33 with pin P22 in SMR block input. | 52 |
| December 2005 | 18 | Updated Clock and Input/Output Ports sections. | 15 and 51 |

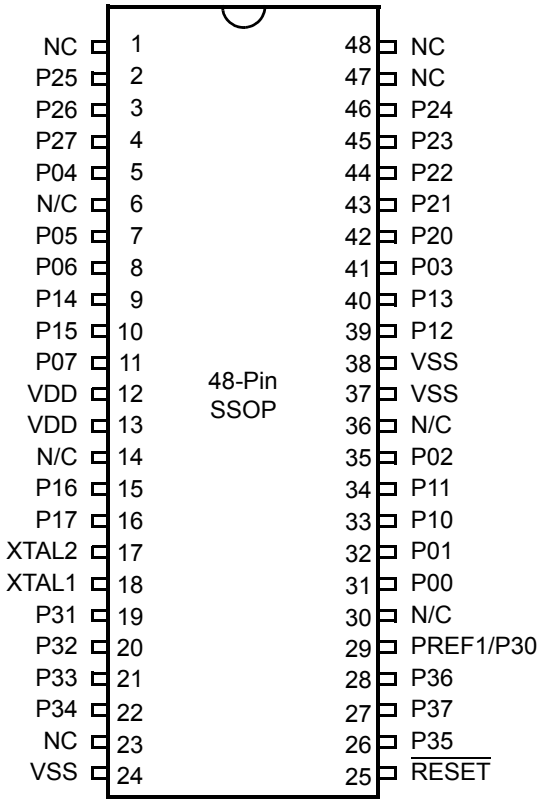



**Figure 6. 48-Pin SSOP Pin Configuration**

**Table 5. 40- and 48-Pin Configuration**

| 40-Pin PDIP No | 48-Pin SSOP No | Symbol |
|---|---|---|
| 26 | 31 | P00 |
| 27 | 32 | P01 |
| 30 | 35 | P02 |
| 34 | 41 | P03 |
| 5 | 5 | P04 |
| 6 | 7 | P05 |
| 7 | 8 | P06 |
| 10 | 11 | P07 |
| 28 | 33 | P10 |
| 29 | 34 | P11 |

**Table 5. 40- and 48-Pin Configuration (Continued)**

| 40-Pin PDIP No | 48-Pin SSOP No | Symbol |
|---|---|---|
| 32 | 39 | P12 |
| 33 | 40 | P13 |
| 8 | 9 | P14 |
| 9 | 10 | P15 |
| 12 | 15 | P16 |
| 13 | 16 | P17 |
| 35 | 42 | P20 |
| 36 | 43 | P21 |
| 37 | 44 | P22 |
| 38 | 45 | P23 |
| 39 | 46 | P24 |
| 2 | 2 | P25 |
| 3 | 3 | P26 |
| 4 | 4 | P27 |
| 16 | 19 | P31 |
| 17 | 20 | P32 |
| 18 | 21 | P33 |
| 19 | 22 | P34 |
| 22 | 26 | P35 |
| 24 | 28 | P36 |
| 23 | 27 | P37 |
| 20 | 23 | NC |
| 40 | 47 | NC |
| 1 | 1 | NC |
| 21 | 25 | $\overline{\text{RESET}}$ |
| 15 | 18 | XTAL1 |
| 14 | 17 | XTAL2 |
| 11 | 12, 13 | $V_{DD}$ |
| 31 | 24, 37, 38 | $V_{SS}$ |
| 25 | 29 | Pref1/P30 |
|  | 48 | NC |
|  | 6 | NC |

**Table 5. 40- and 48-Pin Configuration (Continued)**

| 40-Pin PDIP No | 48-Pin SSOP No | Symbol |
|---|---|---|
| | 14 | NC |
| | 30 | NC |
| | 36 | NC |

# Pin Functions

## XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

## XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonant to the on-chip oscillator output.

## Input/Output Ports

**Caution:** *The CMOS input buffer for each Port 0, 1, or 2 pin is always connected to the pin, even when the pin is configured as an output. If the pin is configured as an open-drain output and no external signal is applied, a High output state can cause the CMOS input buffer to float. This might lead to excessive leakage current of more than 100 µA. To prevent this leakage, connect the pin to an external signal with a defined logic level or ensure its output state is Low, especially during STOP mode.*

*Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.*

*Port 0, 1, and 2 have both input and output capability. The input logic is always present no matter whether the port is configured as input or output. When doing a READ instruction, the MCU reads the actual value at the input logic but not from the output buffer. In addition, the instructions of OR, AND, and XOR have the Read-Modify-Write sequence. The MCU first reads the port, and then modifies the value and load back to the port.*

*Precaution must be taken if the port is configured as open-drain output or if the port is driving any circuit that makes the voltage different from the desired output logic. For example, pins P00–P07 are not connected to anything else. If it is configured as*

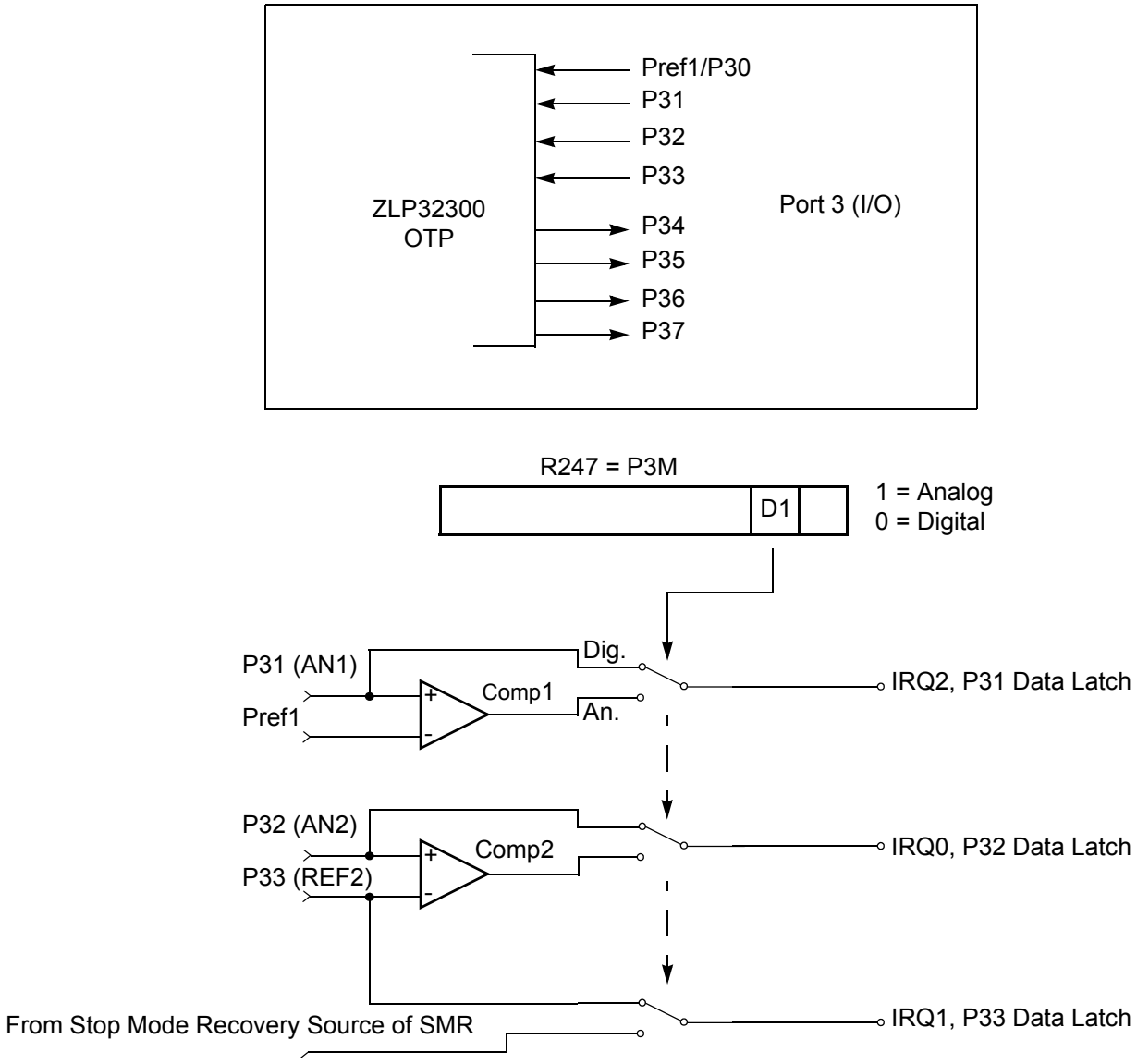



**Figure 10. Port 3 Configuration**

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The Analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20

The upper nibble of the register pointer (see Figure 14) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Crimzon ZLP32300 family, banks 0, F, and D are implemented. A `0h` in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from `1h` to `Fh` exchanges the lower 16 registers to an expanded register bank.

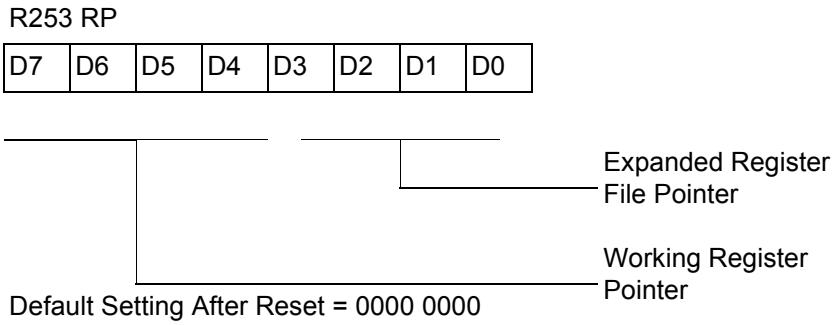



**Figure 14. Register Pointer**

**Example**: Crimzon ZLP32300 (see Figure 13 on page 22)

R253 RP = 00h
R0 = Port 0
R1 = Port 1
R2 = Port 2
R3 = Port 3

But if:

R253 RP = 0Dh
R0 = CTR0
R1 = CTR1
R2 = CTR2
R3 = CTR3

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

```
LD                      RP, #0Dh                ; Select ERF D
for access to bank D
                                                ; (working
register group 0)
LD                      R0,#xx                  ; load CTR0
LD                      1, #xx                  ; load CTR1
```

### Counter/Timer8 High Hold Register—TC8H(D)05h

| Field | Bit Position | | Description |
|---|---|---|---|
| T8_Level_HI | [7:0] | R/W | Data |

### Counter/Timer8 Low Hold Register—TC8L(D)04h

| Field | Bit Position | | Description |
|---|---|---|---|
| T8_Level_LO | [7:0] | R/W | Data |

### CTR0 Counter/Timer8 Control Register—CTR0(D)00h

Table 7 lists and briefly describes the fields for this register.

**Table 7. CTR0(D)00h Counter/Timer8 Control Register**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| T8_Enable | 7------- | R/W | 0*<br>1<br>0<br>1 | Counter Disabled<br>Counter Enabled<br>Stop Counter<br>Enable Counter |
| Single/Modulo-N | -6------- | R/W | 0*<br>1 | Modulo-N<br>Single Pass |
| Time_Out | --5------ | R/W | 0**<br>1<br>0<br>1 | No Counter Time-Out<br>Counter Time-Out Occurred<br>No Effect<br>Reset Flag to 0 |
| T8 _Clock | ---43--- | R/W | 0 0**<br>0 1<br>1 0<br>1 1 | SCLK<br>SCLK/2<br>SCLK/4<br>SCLK/8 |
| Capture_INT_Mask | -----2-- | R/W | 0**<br>1 | Disable Data Capture Interrupt<br>Enable Data Capture Interrupt |
| Counter_INT_Mask | ------1- | R/W | 0**<br>1 | Disable Time-Out Interrupt<br>Enable Time-Out Interrupt |
| P34_Out | -------0 | R/W | 0*<br>1 | P34 as Port Output<br>T8 Output on P34 |

*Indicates the value upon Power-On Reset.
**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.

### P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

### CTR3 T8/T16 Control Register—CTR3(D)03h

Table 10 lists and briefly describes the fields for this register. This register allows the $T_8$ and $T_{16}$ counters to be synchronized.

**Table 10.CTR3 (D)03h: T8/T16 Control Register**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| $T_{16}$ Enable | 7------- | R | 0* | Counter Disabled |
| | | R | 1 | Counter Enabled |
| | | W | 0 | Stop Counter |
| | | W | 1 | Enable Counter |
| $T_8$ Enable | -6------ | R | 0* | Counter Disabled |
| | | R | 1 | Counter Enabled |
| | | W | 0 | Stop Counter |
| | | W | 1 | Enable Counter |
| Sync Mode | --5----- | R/W | 0** | Disable Sync Mode |
| | | | 1 | Enable Sync Mode |
| Reserved | ---43210 | R | 1 | Always reads 11111 |
| | | W | x | No Effect |

*Indicates the value upon Power-On Reset.
**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.

## Counter/Timer Functional Blocks

### Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 16).

### Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into SINGLE-PASS mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the PING-PONG mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7), see Figure 26.

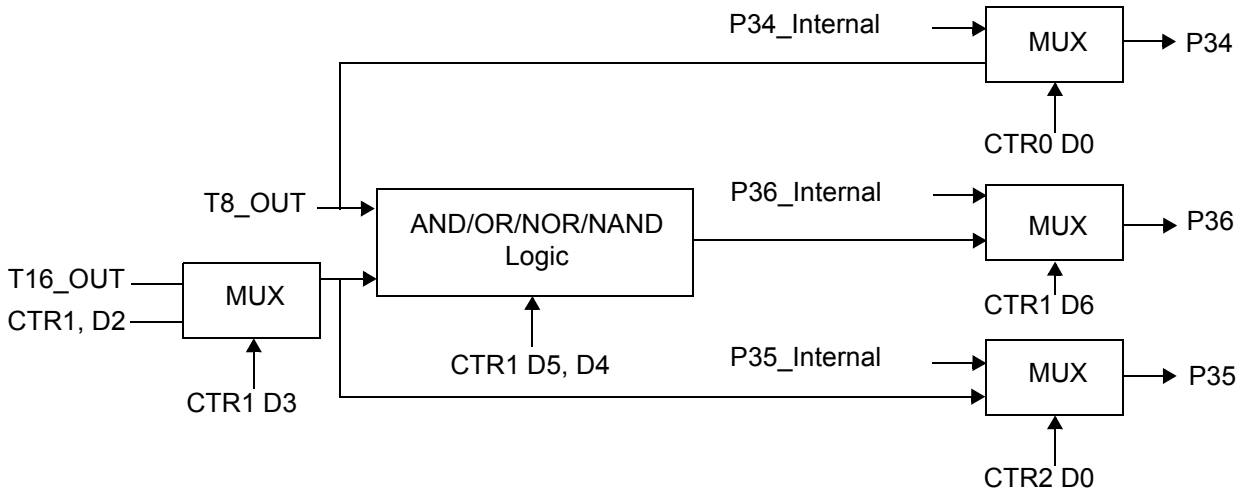



**Figure 27. Output Circuit**

The initial value of T8 or T16 must not be `1`. If you stop the timer and restart the timer, reload the initial value to avoid an unknown previous value.

### During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

### Timer Output

The output logic for the timers is displayed in Figure 27. P34 is used to output T8-OUT when D0 of CTR0 is set. P35 is used to output the value of TI6-OUT when D0 of CTR2 is set. When D6 of CTR1 is set, P36 outputs the logic combination of T8-OUT and T16-OUT determined by D5 and D4 of CTR1.

## Interrupts

The Crimzon ZLP32300 features six different interrupts (see Table 11 on page 45). The interrupts are maskable and prioritized (see Figure 28). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the

**Table 13. SMR2(F)0Dh:Stop Mode Recovery Register 2* (Continued)**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| Source | ---432-- | W | 000† | A. POR Only |
| | | | 001 | B. NAND of P23–P20 |
| | | | 010 | C. NAND of P27–P20 |
| | | | 011 | D. NOR of P33–P31 |
| | | | 100 | E. NAND of P33–P31 |
| | | | 101 | F. NOR of P33–P31, P00, P07 |
| | | | 110 | G. NAND of P33–P31, P00, P07 |
| | | | 111 | H. NAND of P33–P31, P22–P20 |
| Reserved | ------10 | | 00 | Reserved (Must be 0) |

*Port pins configured as outputs are ignored as an SMR recovery source.
†Indicates the value upon Power-On Reset.

**Table 16. EPROM Selectable Options**

| | |
|---|---|
| Port 00–03 Pull-Ups | ON/OFF |
| Port 04–07 Pull-Ups | ON/OFF |
| Port 10–13 Pull-Ups | ON/OFF |
| Port 14–17 Pull-Ups | ON/OFF |
| Port 20–27 Pull-Ups | ON/OFF |
| EPROM Protection | ON/OFF |
| Watchdog Timer at Power-On Reset | ON/OFF |

### Voltage Brownout/Standby

An on-chip Voltage Comparator checks that the $V_{DD}$ is at the required level for correct operation of the device. Reset is globally driven when $V_{DD}$ falls below $V_{BO}$. A small drop in $V_{DD}$ causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the $V_{DD}$ is allowed to stay above $V_{RAM}$, the RAM content is preserved. When the power level is returned to above $V_{BO}$, the device performs a POR and functions normally.

## Low-Voltage Detection

### Low-Voltage Detection Register—LVD(D)0Ch

**Note:** *Voltage detection does not work at STOP mode.*

| Field | Bit Position | | | Description |
|---|---|---|---|---|
| LVD | 76543--- | | | Reserved<br>No Effect |
| | -----2-- | R | 1<br>0* | HVD Flag set<br>HVD Flag reset |
| | ------1- | R | 1<br>0* | LVD Flag set<br>LVD Flag reset |
| | -------0 | R/W | 1<br>0* | Enable VD<br>Disable VD |
| *Default after POR | | | | |

**Note:** *Do not modify register P01M while checking a low-voltage condition. Switching noise of both Ports 0 and 1 together might trigger the LVD Flag.*

**Notes:**

1. *Ensure to differentiate the TRANSMIT mode from DEMODULATION mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.*
2. *Changing from one mode to another cannot be performed without disabling the counter/timers.*

CTR2(0D)02H

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

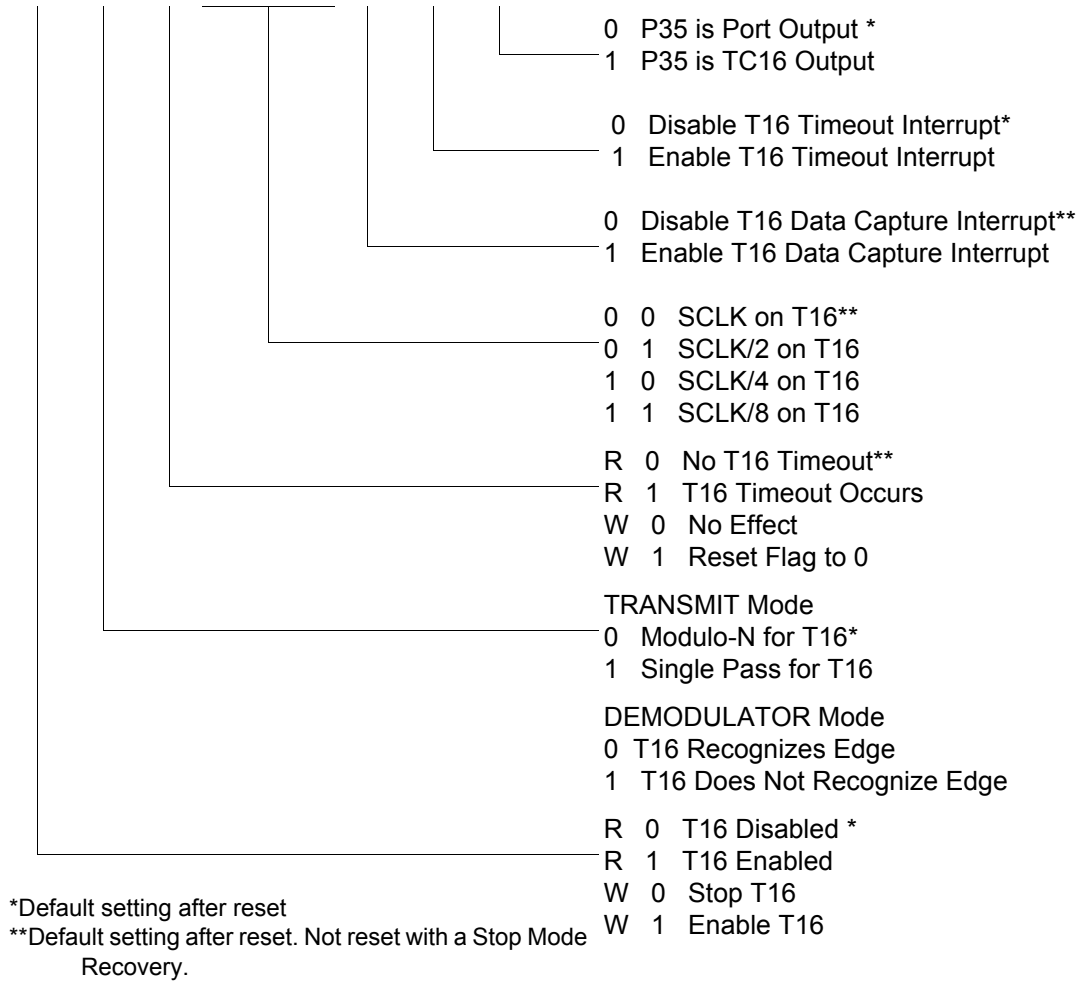
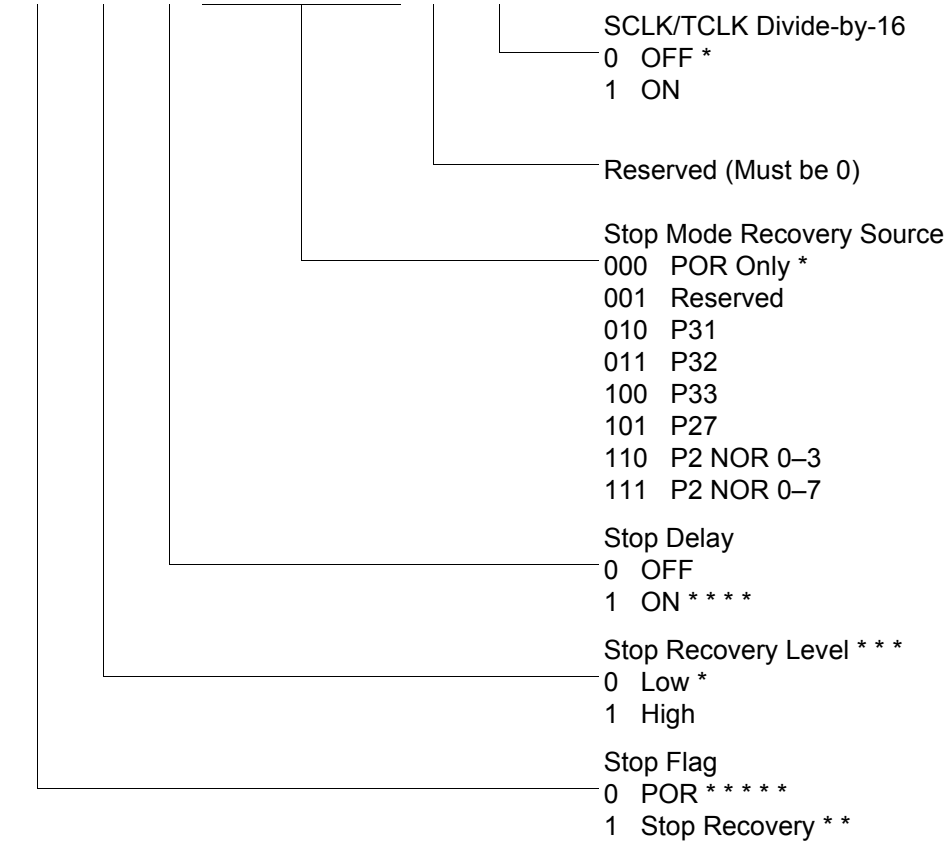



**Figure 39. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)**

SMR(0F)0BH

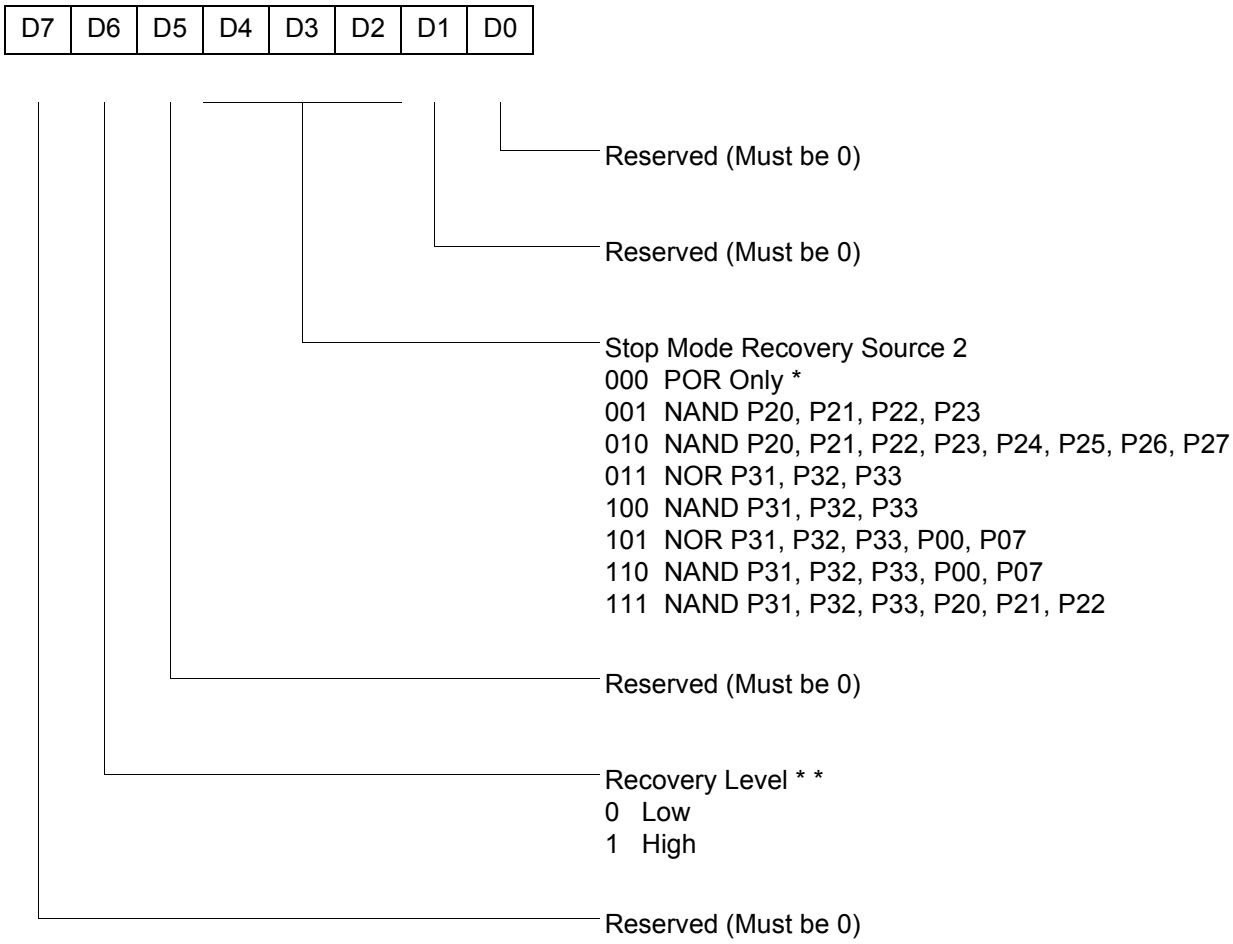
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|




*Default setting after Reset
* *Set after Stop Mode Recovery
* * *At the XOR gate input
* * * *Default setting after Reset. Must be 1 if using a crystal or resonator clock source.
* * * * *Default setting after Power-On Reset. Not Reset with a Stop Mode Recovery.

**Figure 43. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)**

SMR2(0F)0DH




If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.
*Default setting after reset. Not Reset with a Stop Mode Recovery.
* *At the XOR gate input

**Figure 44. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)**

# AC Characteristics

Figure 57 and Table 20 describe the Alternating Current (AC) characteristics.

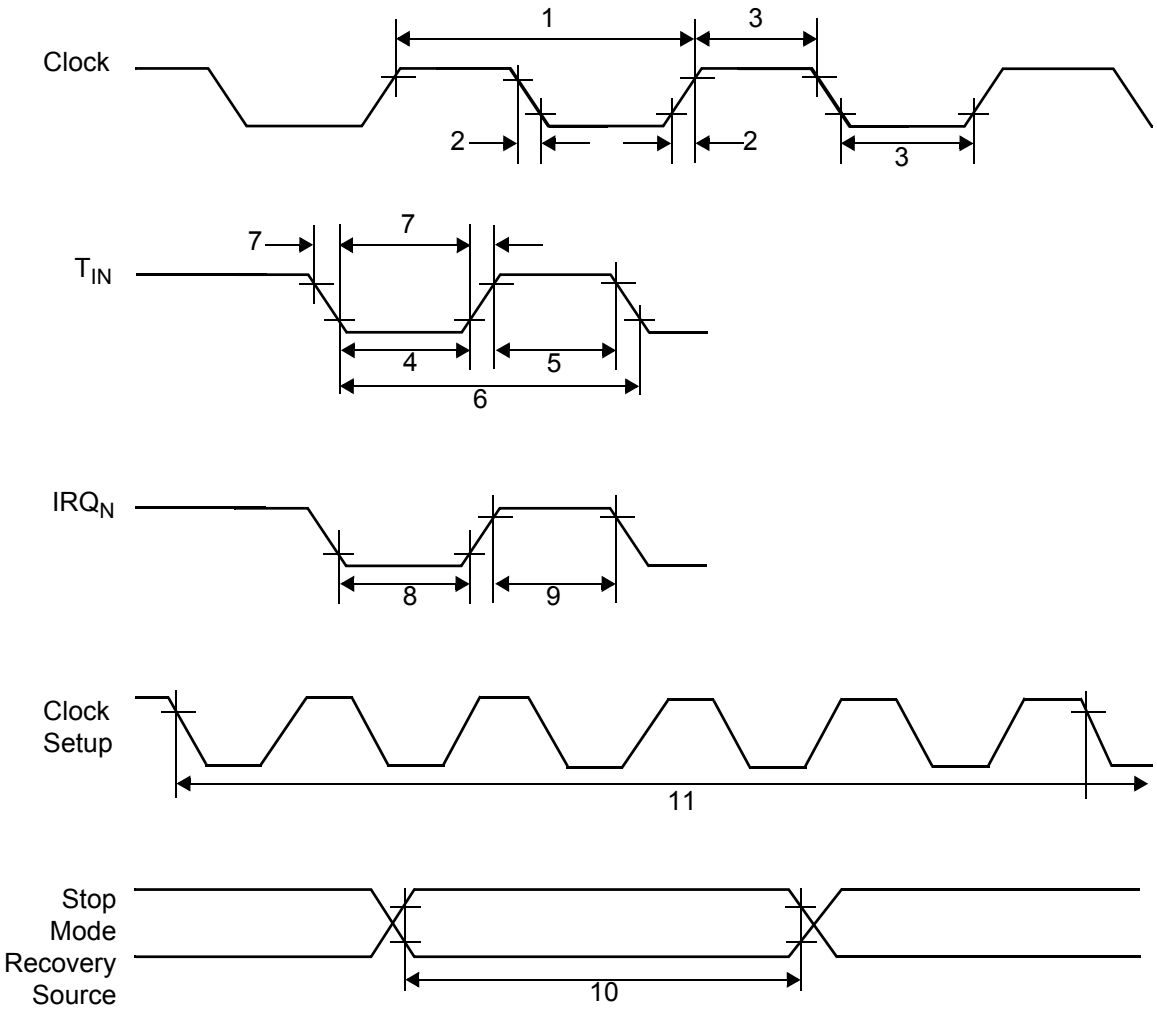
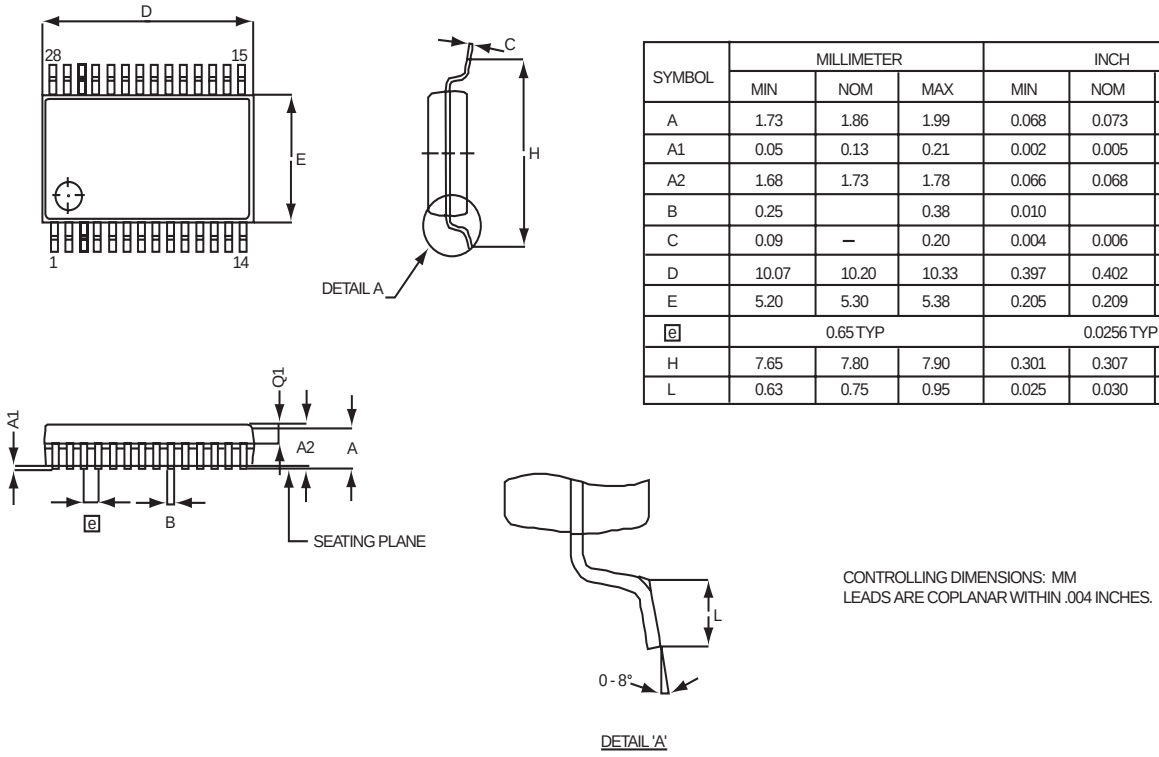
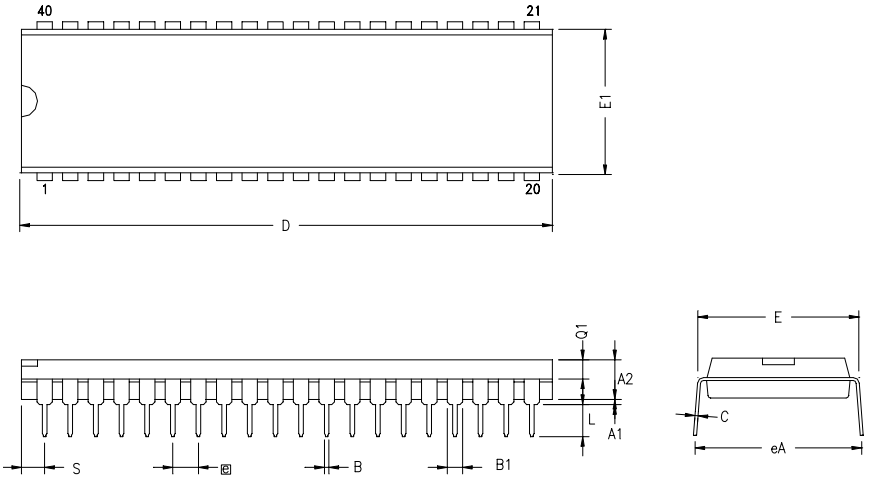



**Figure 57. AC Timing Diagram**




| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.73 | 1.86 | 1.99 | 0.068 | 0.073 | 0.078 |
| A1 | 0.05 | 0.13 | 0.21 | 0.002 | 0.005 | 0.008 |
| A2 | 1.68 | 1.73 | 1.78 | 0.066 | 0.068 | 0.070 |
| B | 0.25 | | 0.38 | 0.010 | | 0.015 |
| C | 0.09 | – | 0.20 | 0.004 | 0.006 | 0.008 |
| D | 10.07 | 10.20 | 10.33 | 0.397 | 0.402 | 0.407 |
| E | 5.20 | 5.30 | 5.38 | 0.205 | 0.209 | 0.212 |
| e | 0.65 TYP | | | 0.0256 TYP | | |
| H | 7.65 | 7.80 | 7.90 | 0.301 | 0.307 | 0.311 |
| L | 0.63 | 0.75 | 0.95 | 0.025 | 0.030 | 0.037 |

**Figure 63. 28-Pin SSOP Package Diagram**




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.51 | 1.02 | .020 | .040 |
| A2 | 3.18 | 3.94 | .125 | .155 |
| B | 0.38 | 0.53 | .015 | .021 |
| B1 | 1.02 | 1.52 | .040 | .060 |
| C | 0.23 | 0.38 | .009 | .015 |
| D | 52.07 | 52.58 | 2.050 | 2.070 |
| E | 15.24 | 15.75 | .600 | .620 |
| E1 | 13.59 | 14.22 | .535 | .560 |
| e | 2.54 TYP | | .100 TYP | |
| eA | 15.49 | 16.76 | .610 | .660 |
| L | 3.05 | 3.81 | .120 | .150 |
| Q1 | 1.40 | 1.91 | .055 | .075 |
| S | 1.52 | 2.29 | .060 | .090 |

CONTROLLING DIMENSIONS : INCH

**Figure 64. 40-Pin PDIP Package Diagram**

# Ordering Information

The Crimzon ZLP32300 is available for the following parts:

| Device | Part Number | Description |
|---|---|---|
| Crimzon ZLP32300 | ZLP32300H4832G | 48-pin SSOP 32 K OTP |
| | ZLP32300P4032G | 40-pin PDIP 32 K OTP |
| | ZLP32300H2832G | 28-pin SSOP 32 K OTP |
| | ZLP32300P2832G | 28-pin PDIP 32 K OTP |
| | ZLP32300S2832G | 28-pin SOIC 32 K OTP |
| | ZLP32300H2032G | 20-pin SSOP 32 K OTP |
| | ZLP32300P2032G | 20-pin PDIP 32 K OTP |
| | ZLP32300S2032G | 20-pin SOIC 32 K OTP |
| | | |
| | ZLP32300H4816G | 48-pin SSOP 16 K OTP |
| | ZLP32300P4016G | 40-pin PDIP 16 K OTP |
| | ZLP32300H2816G | 28-pin SSOP 16 K OTP |
| | ZLP32300P2816G | 28-pin PDIP 16 K OTP |
| | ZLP32300S2816G | 28-pin SOIC 16 K OTP |
| | ZLP32300H2016G | 20-pin SSOP 16 K OTP |
| | ZLP32300P2016G | 20-pin PDIP 16 K OTP |
| | ZLP32300S2016G | 20-pin SOIC 16 K OTP |
| | | |
| | ZLP32300H4808G | 48-pin SSOP 8 K OTP |
| | ZLP32300P4008G | 40-pin PDIP 8 K OTP |
| | ZLP32300H2808G | 28-pin SSOP 8 K OTP |
| | ZLP32300P2808G | 28-pin PDIP 8 K OTP |
| | ZLP32300S2808G | 28-pin SOIC 8 K OTP |
| | ZLP32300H2008G | 20-pin SSOP 8 K OTP |

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# Customer Support

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