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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlp32300s2832c

Warning: DO NOT USE IN LIFE SUPPORT

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As used herein

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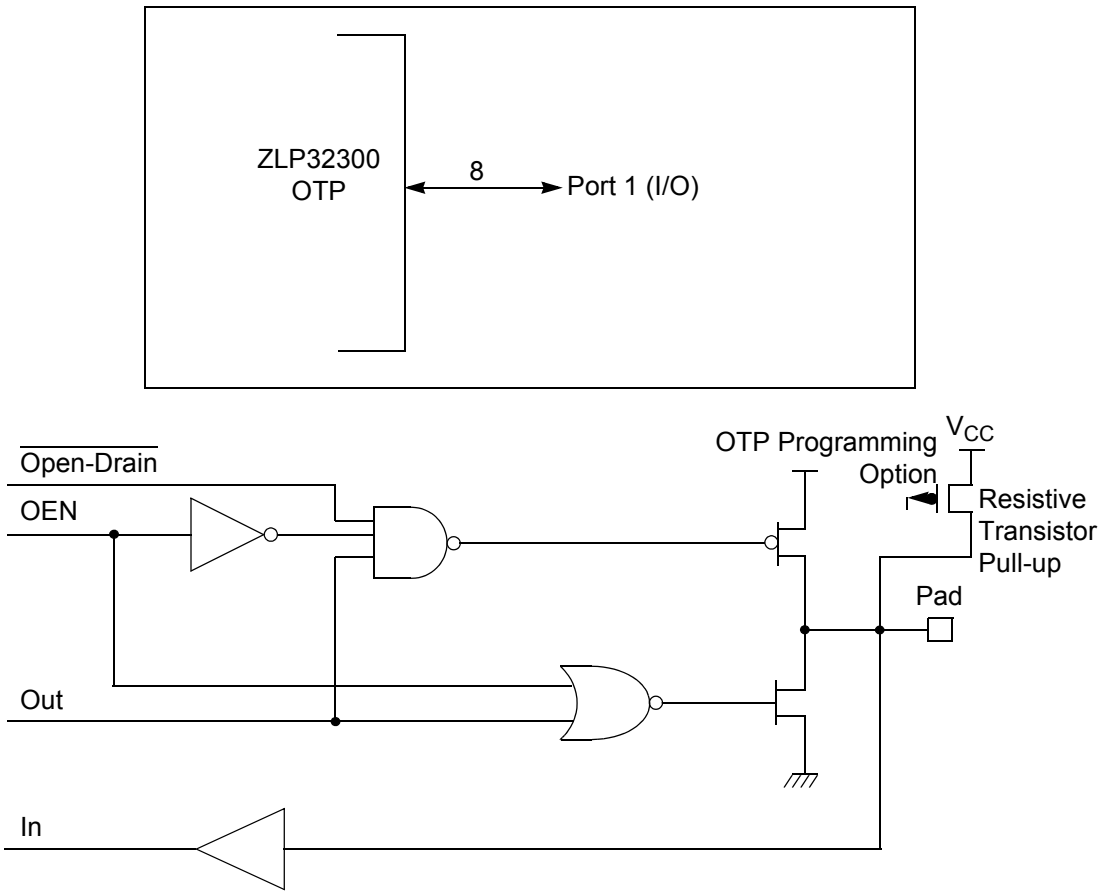


Figure 8. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 9). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A EPROM option bit is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in DEMODULATION mode.

register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

Note: *An expanded register bank is also referred to as an expanded register group (see* Figure 13*).*

```
LD                      R1, 2                   ; CTR2→CTR1

LD                      RP, #0Dh                ; Select ERF D
for access to bank D
                                                ; (working
register group 0)
LD                      RP, #7Dh                ; Select
expanded register bank D and working            ; register
group 7 of bank 0 for access.
LD                      71h, 2
; CTRL2→register 71h
LD                      R1, 2
; CTRL2→register 71h
```

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 7 on page 27) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (see Figure 15). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note: *Working register group E0–EF can only be accessed through working registers and indirect addressing modes.*

Counter/Timer8 High Hold Register—TC8H(D)05h

Field	Bit Position		Description
T8_Level_HI	[7:0]	R/W	Data

Counter/Timer8 Low Hold Register—TC8L(D)04h

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

CTR0 Counter/Timer8 Control Register—CTR0(D)00h

Table 7 lists and briefly describes the fields for this register.

Table 7. CTR0(D)00h Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R/W	0* 1 0 1	Counter Disabled Counter Enabled Stop Counter Enable Counter
Single/Modulo-N	-6-------	R/W	0* 1	Modulo-N Single Pass
Time_Out	--5------	R/W	0** 1 0 1	No Counter Time-Out Counter Time-Out Occurred No Effect Reset Flag to 0
T8 _Clock	---43---	R/W	0 0** 0 1 1 0 1 1	SCLK SCLK/2 SCLK/4 SCLK/8
Capture_INT_Mask	-----2--	R/W	0** 1	Disable Data Capture Interrupt Enable Data Capture Interrupt
Counter_INT_Mask	------1-	R/W	0** 1	Disable Time-Out Interrupt Enable Time-Out Interrupt
P34_Out	-------0	R/W	0* 1	P34 as Port Output T8 Output on P34

*Indicates the value upon Power-On Reset.
**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.

Caution: *Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.*

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur, see Figure 19 and Figure 20.

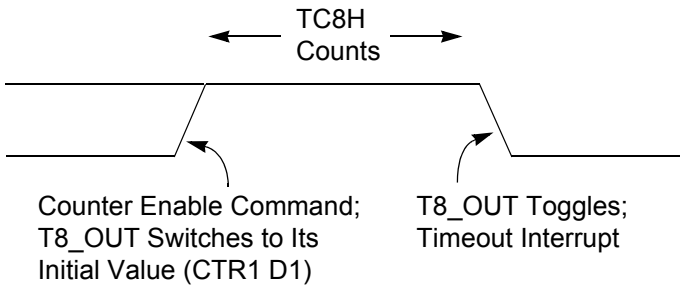


Figure 19. T8_OUT in SINGLE-PASS Mode

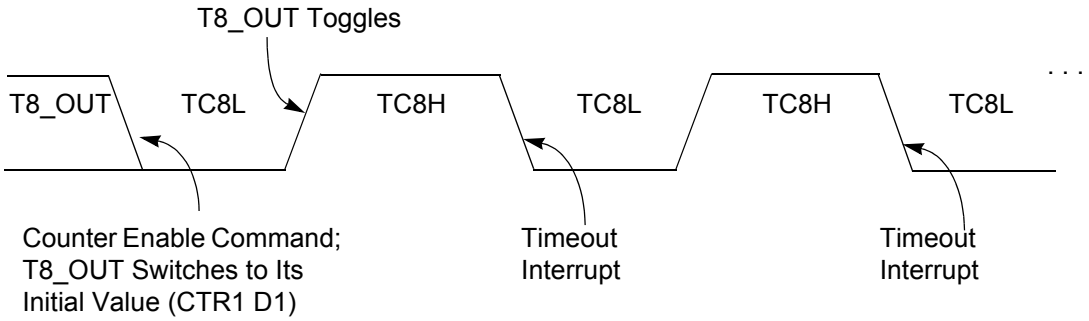


Figure 20. T8_OUT in MODULO-N Mode

T8 DEMODULATION Mode

You must program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the time-out status bit (CTR0, D5) is set, and an

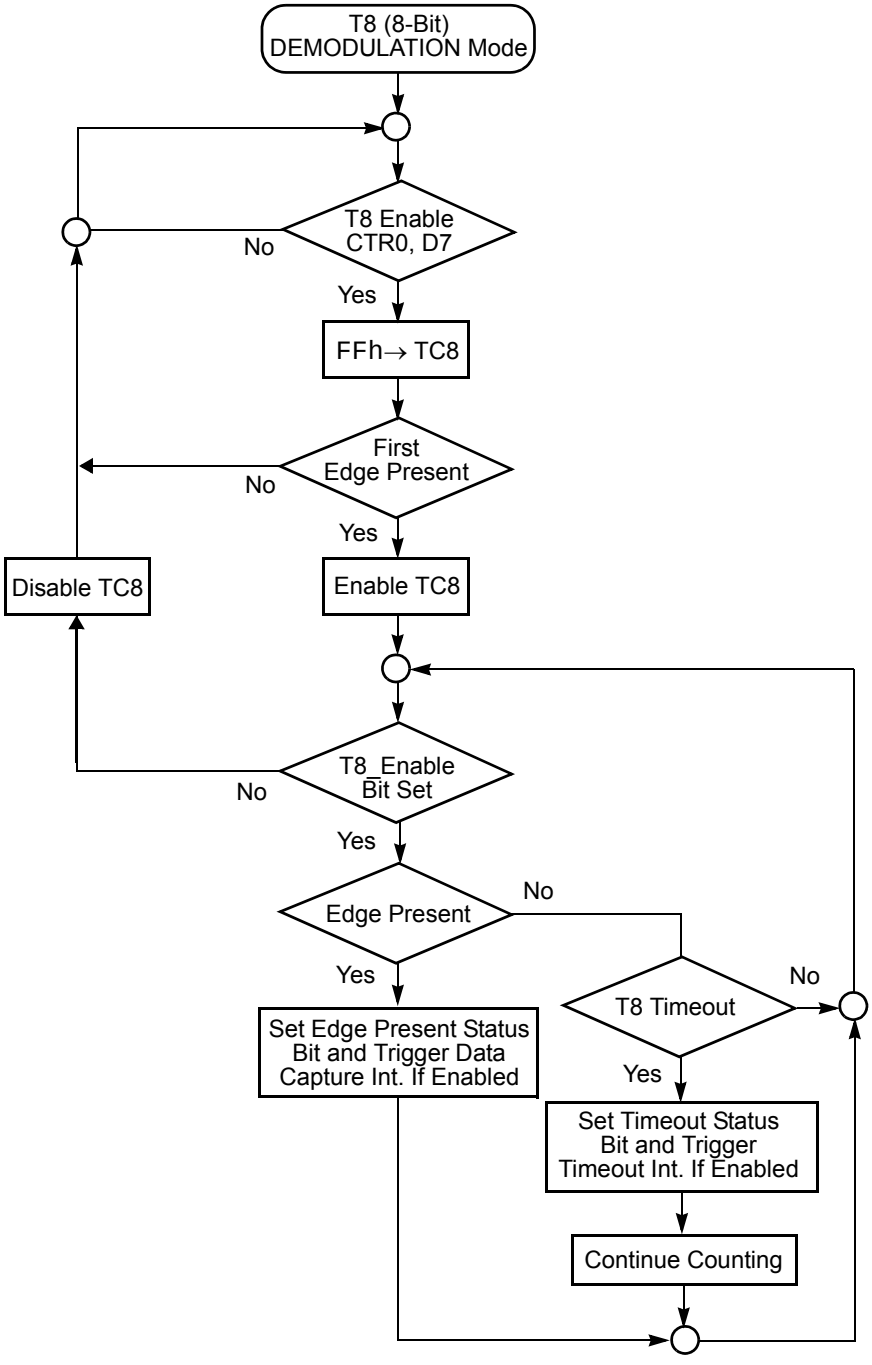


Figure 22. DEMODULATION Mode Flowchart

Caution: *Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to* FFFFh *to* FFFEh. *Transition from 0 to* FFFFh *is not a timeout condition.*

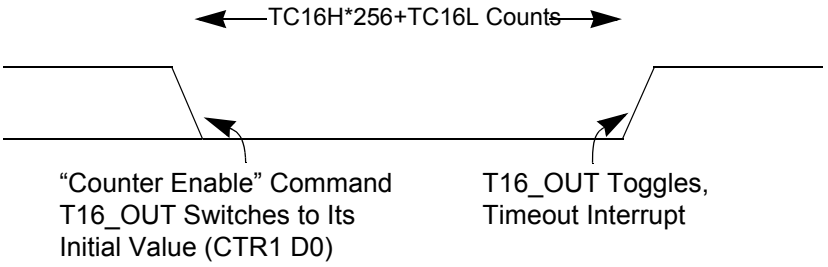


Figure 24. T16_OUT in SINGLE-PASS Mode

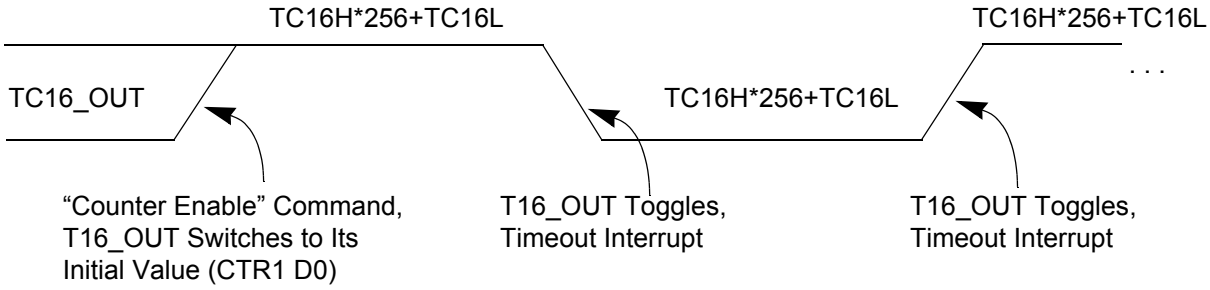


Figure 25. T16_OUT in MODULO-N Mode

T16 DEMODULATION Mode

You must program TC16L and TC16H to FFh. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFh and starts again.

counter/timers (see Table 11 on page 45) and one for low-voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in DIGITAL mode, Pin P33 is the source. When in ANALOG mode, the output of the Stop Mode Recovery source logic is used as the source for the interrupt, see Figure 33 on page 52.

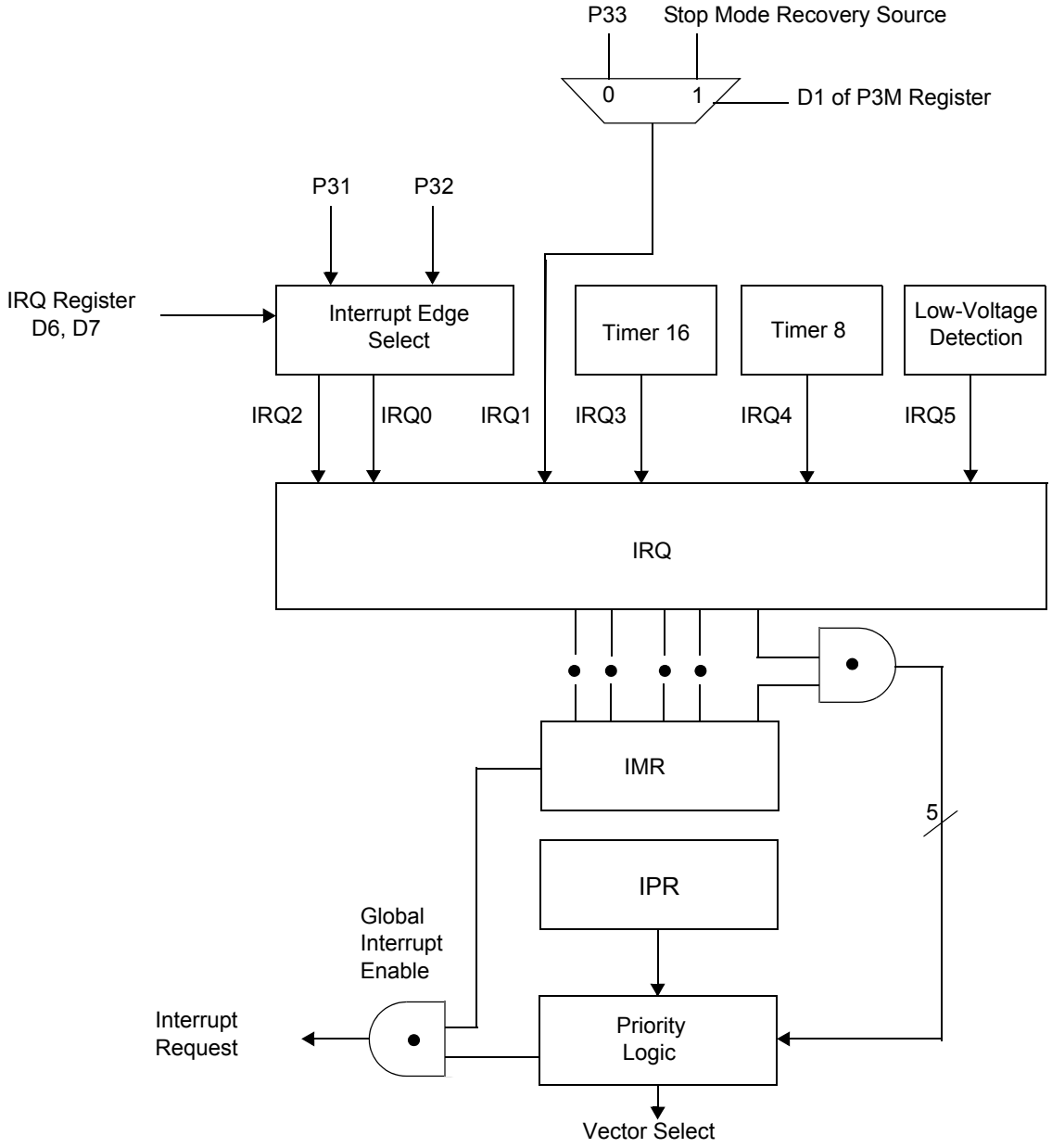
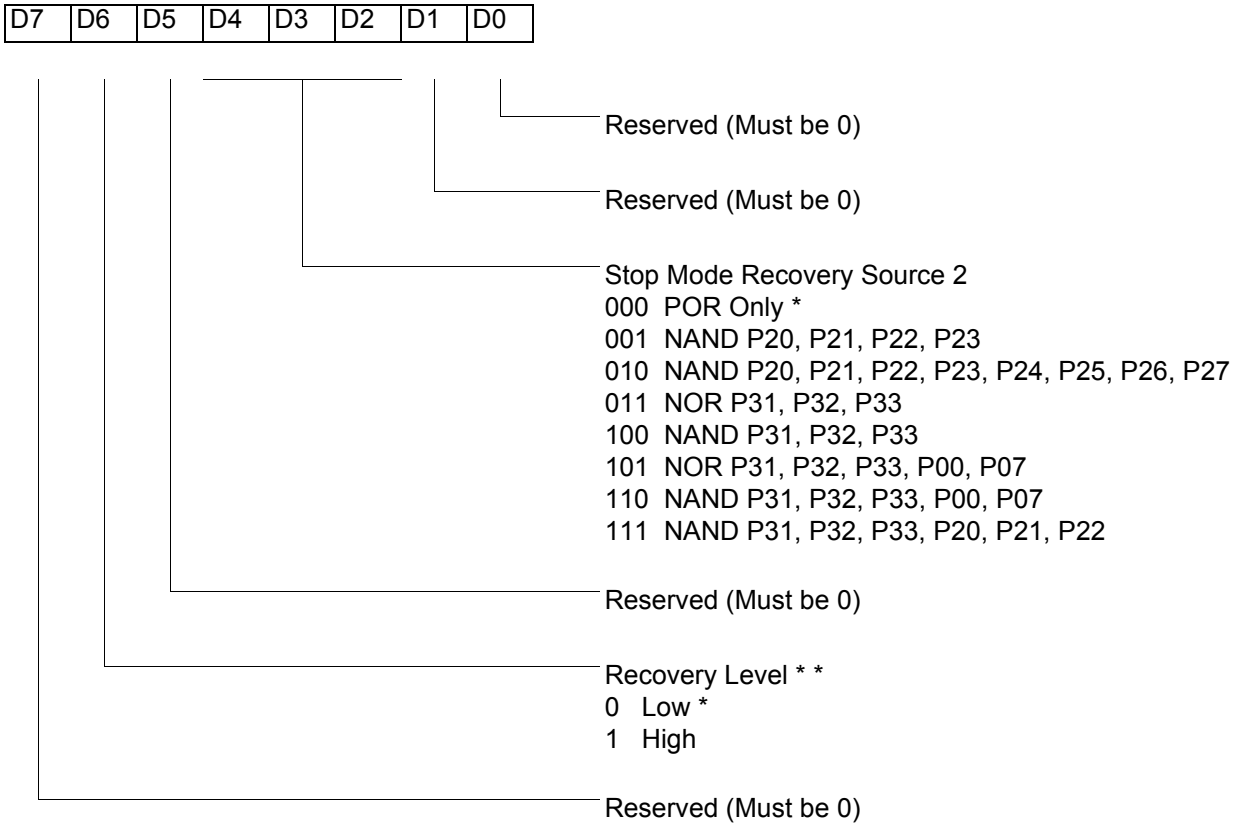


Figure 28. Interrupt Block Diagram

Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (see Figure 34).

SMR2(0F)Dh



If used in conjunction with SMR, either of the two specified events causes a Stop Mode Recovery.
*Default setting after reset.
* *At the XOR gate input.

Figure 34. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

Note: *Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.*

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 15.

Table 15. Watchdog Timer Time Select

D1	D0	Timeout of Internal RC-Oscillator
0	0	5 ms min
0	1	10 ms min
1	0	20 ms min
1	1	80 ms min

WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1, see Figure 36.

Table 16. EPROM Selectable Options

Port 00–03 Pull-Ups	ON/OFF
Port 04–07 Pull-Ups	ON/OFF
Port 10–13 Pull-Ups	ON/OFF
Port 14–17 Pull-Ups	ON/OFF
Port 20–27 Pull-Ups	ON/OFF
EPROM Protection	ON/OFF
Watchdog Timer at Power-On Reset	ON/OFF

Voltage Brownout/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO}. A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM}, the RAM content is preserved. When the power level is returned to above V_{BO}, the device performs a POR and functions normally.

Low-Voltage Detection

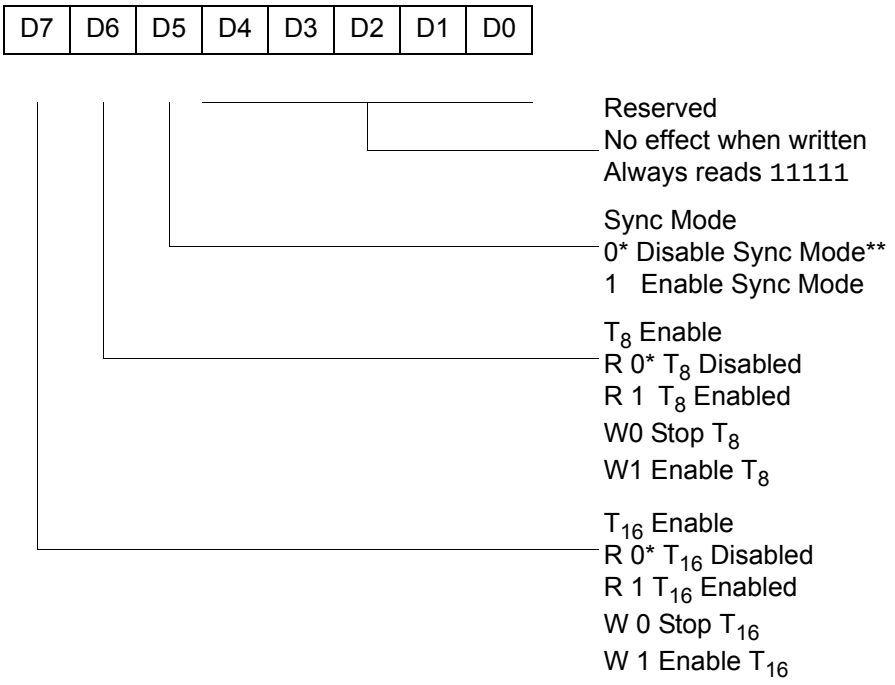
Low-Voltage Detection Register—LVD(D)0Ch

Note: *Voltage detection does not work at STOP mode.*

Field	Bit Position			Description
LVD	76543---			Reserved No Effect
	-----2--	R	1 0*	HVD Flag set HVD Flag reset
	------1-	R	1 0*	LVD Flag set LVD Flag reset
	-------0	R/W	1 0*	Enable VD Disable VD
*Default after POR				

Note: *Do not modify register P01M while checking a low-voltage condition. Switching noise of both Ports 0 and 1 together might trigger the LVD Flag.*

CTR3(0D)03H

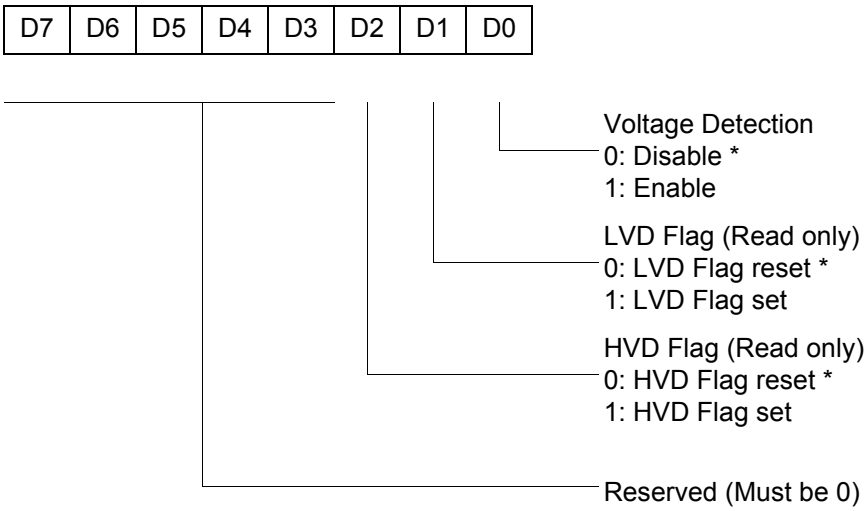


*Default setting after reset.
**Default setting after reset. Not reset with a Stop Mode Recovery.

Figure 40. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)

Note: *If Sync Mode is enabled, the first pulse of T8 carrier is always synchronized with T16 (demodulated signal). It can always provide a full carrier pulse.*

LVD(0D)0CH



*Default setting after reset.

Figure 41. Voltage Detection Register

Note: *Do not modify register P01M while checking a low-voltage condition. Switching noise of both Ports 0 and 1 together might trigger the LVD Flag.*

AC Characteristics

Figure 57 and Table 20 describe the Alternating Current (AC) characteristics.

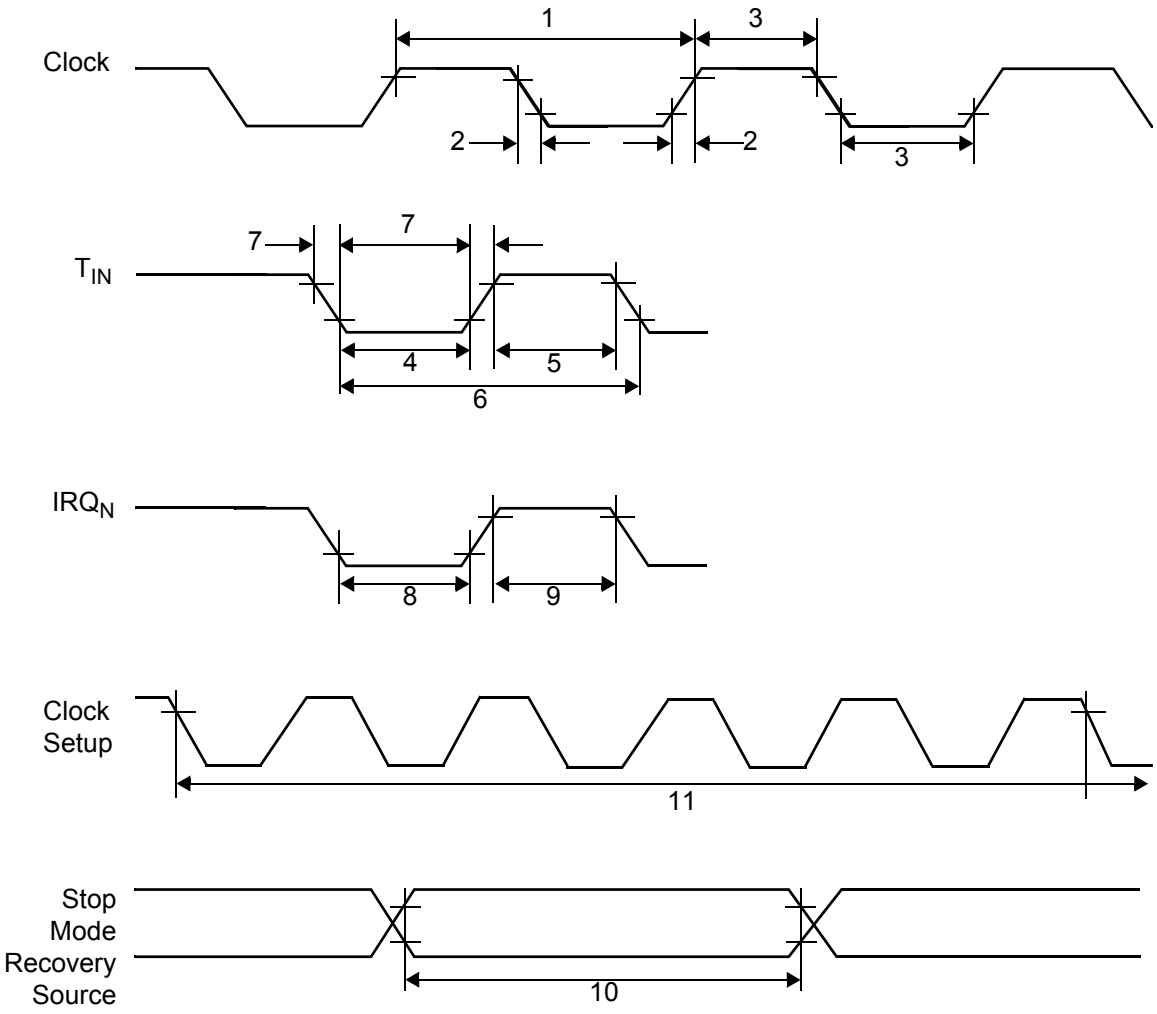


Figure 57. AC Timing Diagram

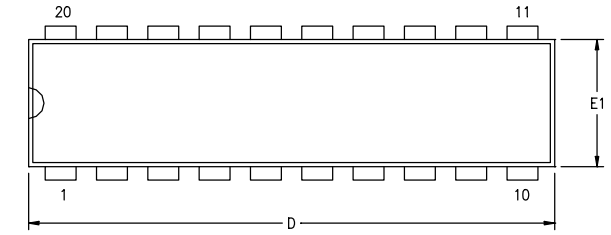
Table 20. AC Characteristics

			T_A=0 °C to +70 °C 8.0 MHz					Watchdog Timer Mode Register (D1, D0)
No	**Symbol**	**Parameter**	**V_{CC}**	**Minimum**	**Maximum**	**Units**	**Notes**	
1	TpC	Input Clock Period	2.0–3.6	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1	
3	TwC	Input Clock Width	2.0–3.6	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–3.6	3TpC			1	
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–3.6	5TpC			1, 2	
10	Twsm	Stop Mode Recovery Width Spec	2.0–3.6	12 10TpC		ns	3 4	
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4	
12	Twdt	Watchdog Timer Delay Time	2.0–3.6 2.0–3.6 2.0–3.6 2.0–3.6	5 10 20 80		ms ms ms ms		0, 0 0, 1 1, 0 1, 1
13	T_{POR}	Power-on reset	2.0–3.6	2.5	10	ms		

Notes
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR–D5 = 1.
4. SMR–D5 = 0.

Packaging

Package information for all versions of Crimzon ZLP32300 is displayed in Figure 58 through Figure 65.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	0.81	.015	.032
A2	3.25	3.68	.128	.145
B	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
e	2.54 BSC		.100 BSC	
eA	7.87	9.14	.310	.360
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

CONTROLLING DIMENSIONS : INCH

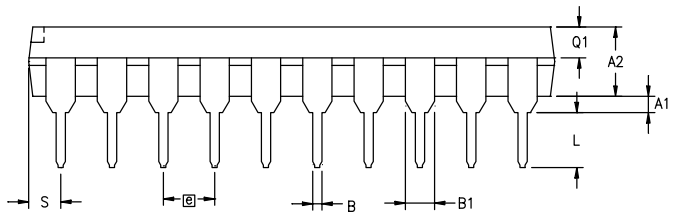


Figure 58. 20-Pin PDIP Package Diagram

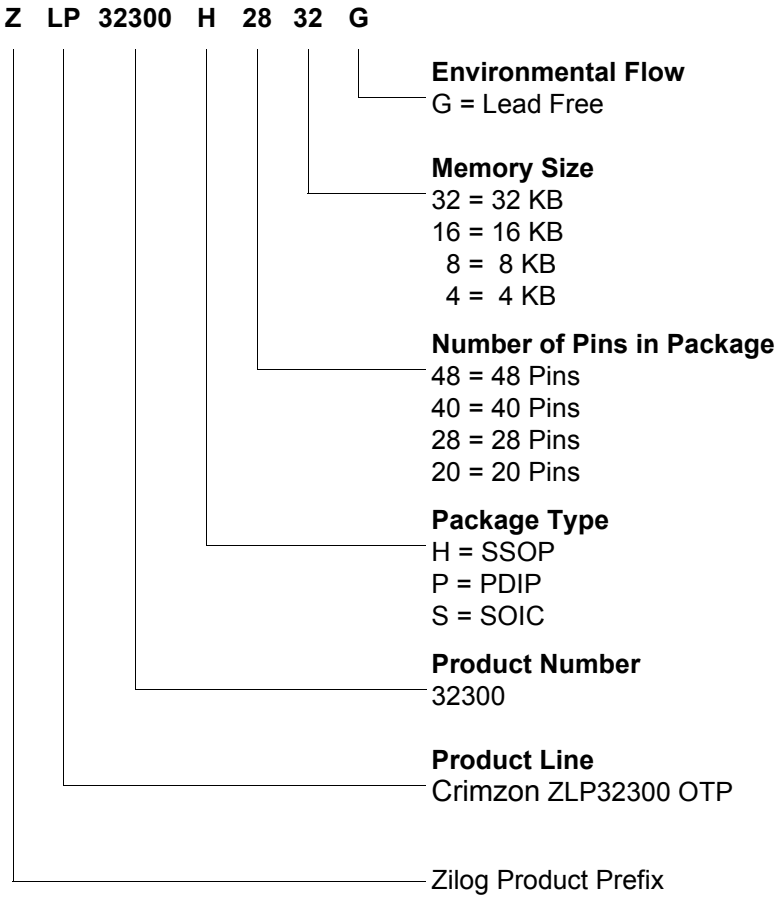
Ordering Information

The Crimzon ZLP32300 is available for the following parts:

Device	Part Number	Description
Crimzon ZLP32300	ZLP32300H4832G	48-pin SSOP 32 K OTP
	ZLP32300P4032G	40-pin PDIP 32 K OTP
	ZLP32300H2832G	28-pin SSOP 32 K OTP
	ZLP32300P2832G	28-pin PDIP 32 K OTP
	ZLP32300S2832G	28-pin SOIC 32 K OTP
	ZLP32300H2032G	20-pin SSOP 32 K OTP
	ZLP32300P2032G	20-pin PDIP 32 K OTP
	ZLP32300S2032G	20-pin SOIC 32 K OTP
	ZLP32300H4816G	48-pin SSOP 16 K OTP
	ZLP32300P4016G	40-pin PDIP 16 K OTP
	ZLP32300H2816G	28-pin SSOP 16 K OTP
	ZLP32300P2816G	28-pin PDIP 16 K OTP
	ZLP32300S2816G	28-pin SOIC 16 K OTP
	ZLP32300H2016G	20-pin SSOP 16 K OTP
	ZLP32300P2016G	20-pin PDIP 16 K OTP
	ZLP32300S2016G	20-pin SOIC 16 K OTP
	ZLP32300H4808G	48-pin SSOP 8 K OTP
	ZLP32300P4008G	40-pin PDIP 8 K OTP
	ZLP32300H2808G	28-pin SSOP 8 K OTP
	ZLP32300P2808G	28-pin PDIP 8 K OTP
	ZLP32300S2808G	28-pin SOIC 8 K OTP
	ZLP32300H2008G	20-pin SSOP 8 K OTP

Part Number Description

Zilog® part numbers consist of a number of components, as shown below. ZLP32300H2832G is a Crimzon ZLP32300 OTP product in a 28-pin SSOP package, with 32 KB of OTP and built with lead-free solder.



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