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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlp32300s2832g

Architectural Overview

Zilog's Crimzon® ZLP32300 is an OTP-based member of the MCU family of infrared microcontrollers. With 237 B of general-purpose RAM and 8 KB to 32 KB of OTP, Zilog's CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Crimzon ZLP32300 architecture (see Figure 1 on page 3) is based on Zilog's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® CPU offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations:

1. Program Memory
2. Register File
3. Expanded Register File

The register file is composed of 256 Bytes of RAM. It includes four I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Crimzon ZLP32300 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2 on page 4). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

▶ **Note:** *All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.*

Power connections use the conventional descriptions listed in Table 1.

Table 1. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is displayed in Figure 3 and described in Table 3. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 4. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are displayed in Figure 5, Figure 6, and described in Table 5.
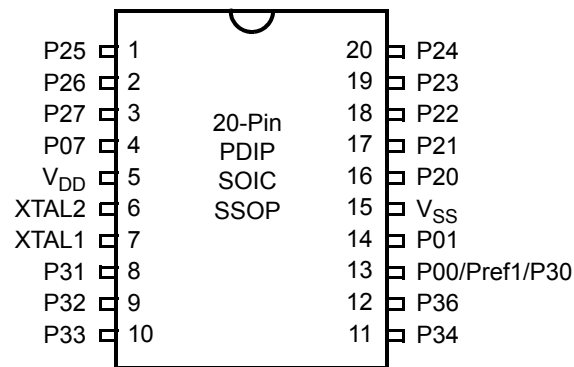

Figure 3. 20-Pin PDIP/SOIC/SSOP Pin Configuration

Table 3. 20-Pin PDIP/SOIC/SSOP Pin Identification

Pin No	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V_{DD}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34, P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V_{SS}	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output

```
          NC ⊏ 1            40 ⊐ NC
         P25 ⊏ 2            39 ⊐ P24
         P26 ⊏ 3            38 ⊐ P23
         P27 ⊏ 4            37 ⊐ P22
         P04 ⊏ 5            36 ⊐ P21
         P05 ⊏ 6            35 ⊐ P20
         P06 ⊏ 7            34 ⊐ P03
         P14 ⊏ 8            33 ⊐ P13
         P15 ⊏ 9            32 ⊐ P12
         P07 ⊏ 10  40-Pin   31 ⊐ VSS
         VDD ⊏ 11  PDIP     30 ⊐ P02
         P16 ⊏ 12           29 ⊐ P11
         P17 ⊏ 13           28 ⊐ P10
       XTAL2 ⊏ 14           27 ⊐ P01
       XTAL1 ⊏ 15           26 ⊐ P00
         P31 ⊏ 16           25 ⊐ Pref1/P30
         P32 ⊏ 17           24 ⊐ P36
         P33 ⊏ 18           23 ⊐ P37
         P34 ⊏ 19           22 ⊐ P35
          NC ⊏ 20           21 ⊐ RESET
```
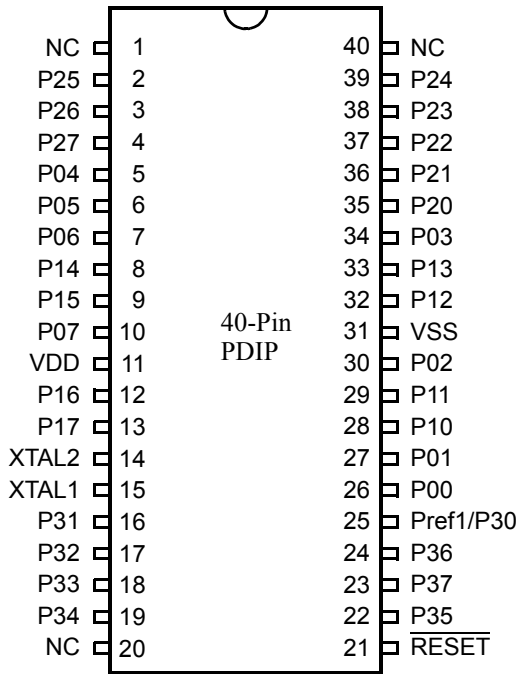
Figure 5. 40-Pin PDIP Pin Configuration

The upper nibble of the register file address provided by the register pointer specifies the active working-register group.

The lower nibble of the register file address provided by the instruction points to the specified register.

R15 to R0

R15 to R4 *

R3 to R0 *

* RP = 00: Selects Register Bank 0, Working Register Group 0
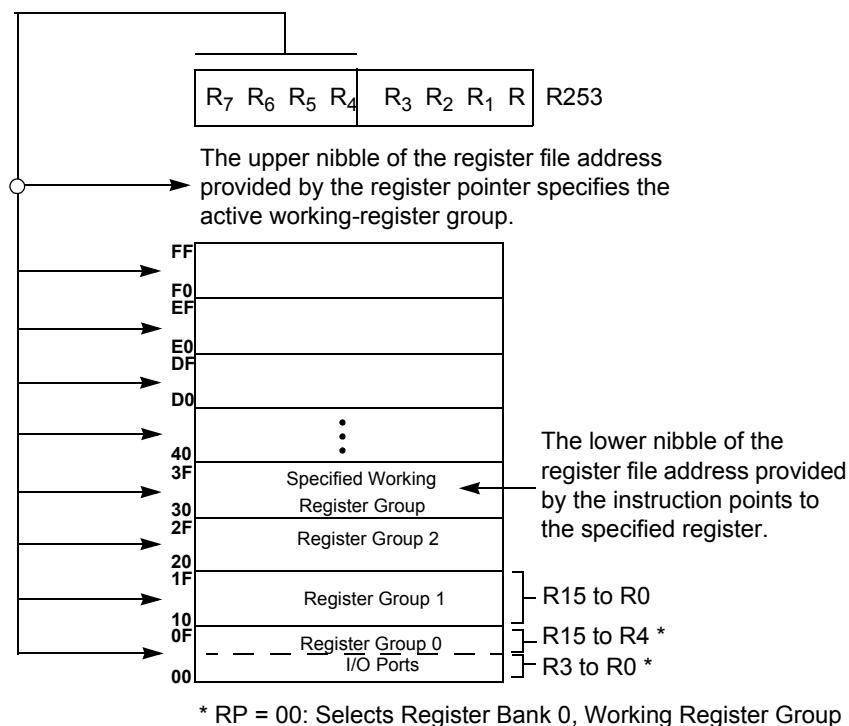
Figure 15. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

Timers

T8_Capture_HI—HI8(D)0Bh

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data—No Effect
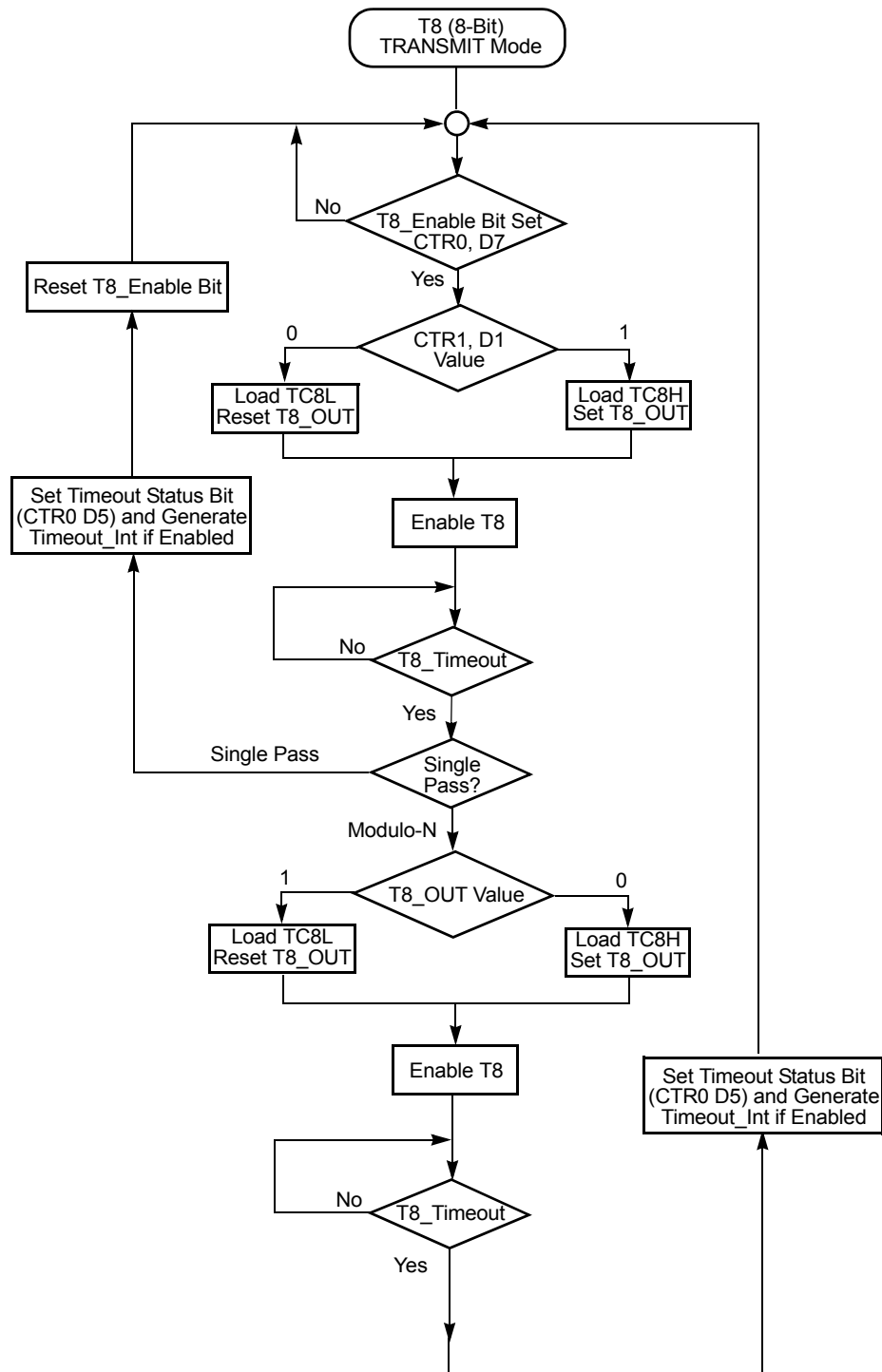
Figure 17. TRANSMIT Mode Flowchart
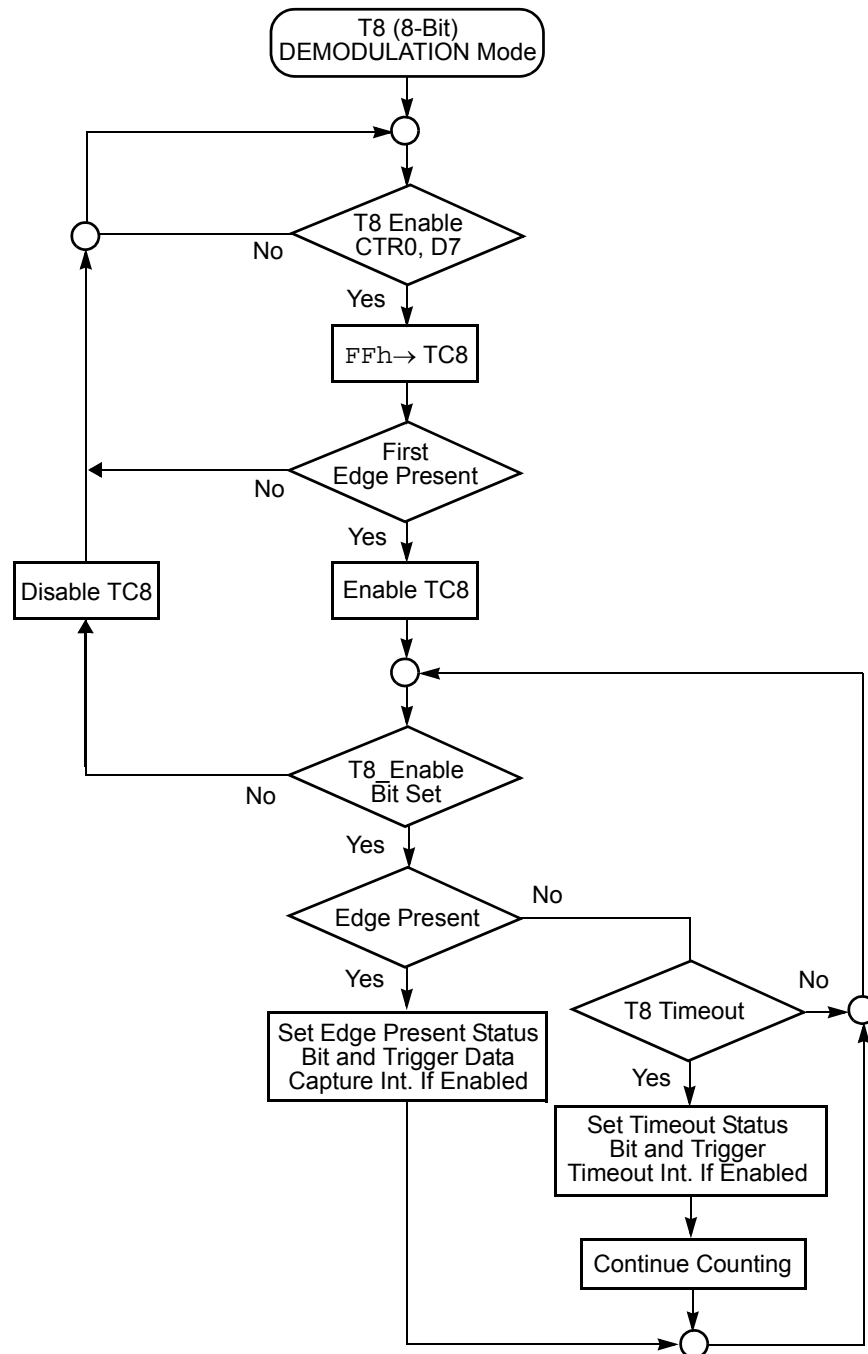
Figure 22. DEMODULATION Mode Flowchart

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

PING-PONG Mode

This operation mode is only valid in TRANSMIT mode. T8 and T16 must be programmed in SINGLE-PASS mode (CTR0, D6; CTR2, D6), and PING-PONG mode must be programmed in CTR1, D3; D2. You can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1, see Figure 26.

Note: *Enabling Ping-Pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status Flags before instituting this operation.*
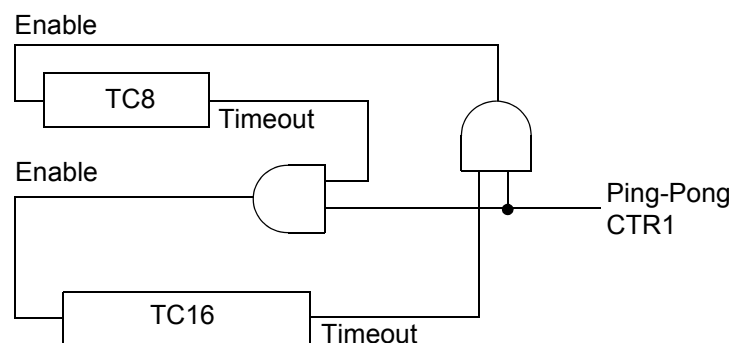

Figure 26. PING-PONG Mode Diagram

Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω. The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors from each pin to ground. The typical capacitor value is 10 pF for 8 MHz. Also check with the crystal supplier for the optimum capacitance.

Crystal
C1, C2 = 10 pF *
f = 8 MHz

External Clock

Ceramic Resonator f = 8 MHz
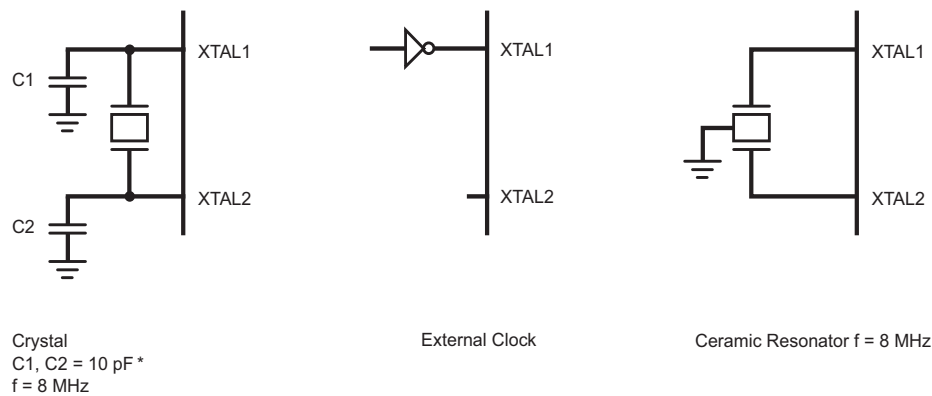
*Note: preliminary value.

Figure 29. Oscillator Configuration

Zilog's IR MCU supports crystal, resonator, and oscillator. Most resonators have a frequency tolerance of less than ±0.5%, which is enough for remote control application. Resonator has a very fast startup time, which is around few hundred microseconds. Most crystals have a frequency tolerance of less than 50 ppm (±0.005%). However, crystal needs longer startup time than the resonator. The large loading capacitance slows down the oscillation startup time. Zilog® suggests not to use more than 10 pF loading capacitor for the crystal. If the stray capacitance of the PCB or the crystal is high, the loading capacitance C1 and C2 must be reduced further to ensure stable oscillation before the T_{POR} (Power-On Reset time is typically 5-6 ms, see Table 20 on page 79).

For Stop Mode Recovery operation, bit 5 of SMR register allows you to select the Stop Mode Recovery delay, which is the T_{POR}. If Stop Mode Recovery delay is not selected, the MCU executes instruction immediately after it wakes up from the STOP mode. If resonator or crystal is used as a clock source then Stop Mode Recovery delay needs to be selected (bit 5 of SMR = 1).

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 15.

Table 15. Watchdog Timer Time Select

D1	D0	Timeout of Internal RC-Oscillator
0	0	5 ms min
0	1	10 ms min
1	0	20 ms min
1	1	80 ms min

WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1, see Figure 36.

Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are displayed in Figure 37 through Figure 41.

CTR0(0D)00H

D7	D6	D5	D4	D3	D2	D1	D0

0 P34 as Port Output *
1 Timer8 Output

0 Disable T8 Timeout Interrupt**
1 Enable T8 Timeout Interrupt

0 Disable T8 Data Capture Interrupt**
1 Enable T8 Data Capture Interrupt

00 SCLK on T8**
01 SCLK/2 on T8
10 SCLK/4 on T8
11 SCLK/8 on T8

R 0 No T8 Counter Timeout**
R 1 T8 Counter Timeout Occurred
W 0   No Effect
W 1   Reset Flag to 0

0 Modulo-N*
1 Single Pass

R 0 T8 Disabled *
R 1 T8 Enabled
W 0   Stop T8
W 1   Enable T8
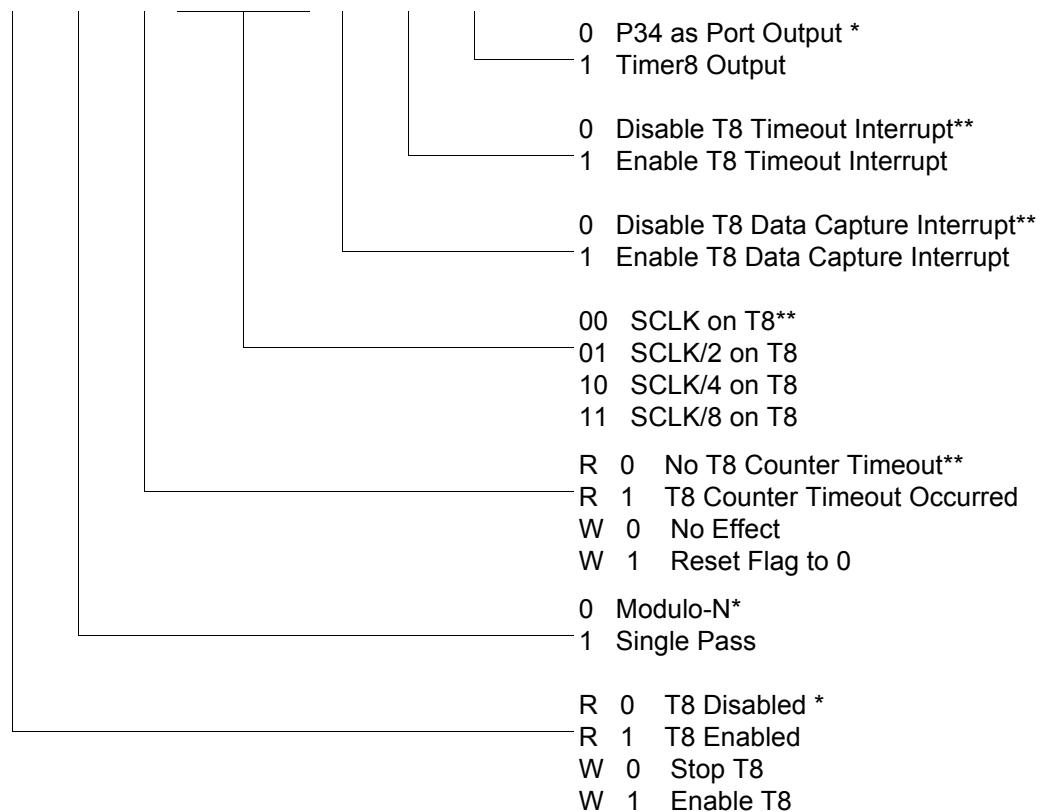
*Default setting after reset.
**Default setting after reset. Not reset with a Stop Mode Recovery.

Figure 37. TC8 Control Register ((0D)O0H: Read/Write Except Where Noted)

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are displayed in Figure 42 through Figure 55 on page 74.

PCON(0F)00H

D7	D6	D5	D4	D3	D2	D1	D0

Comparator Output Port 3
0   P34, P37 Standard Output *
1   P34, P37 Comparator Output

Port 1
0: Open-Drain
1: Push-Pull*

Port 0
0: Open-Drain
1: Push-Pull *

Reserved (Must be 1)
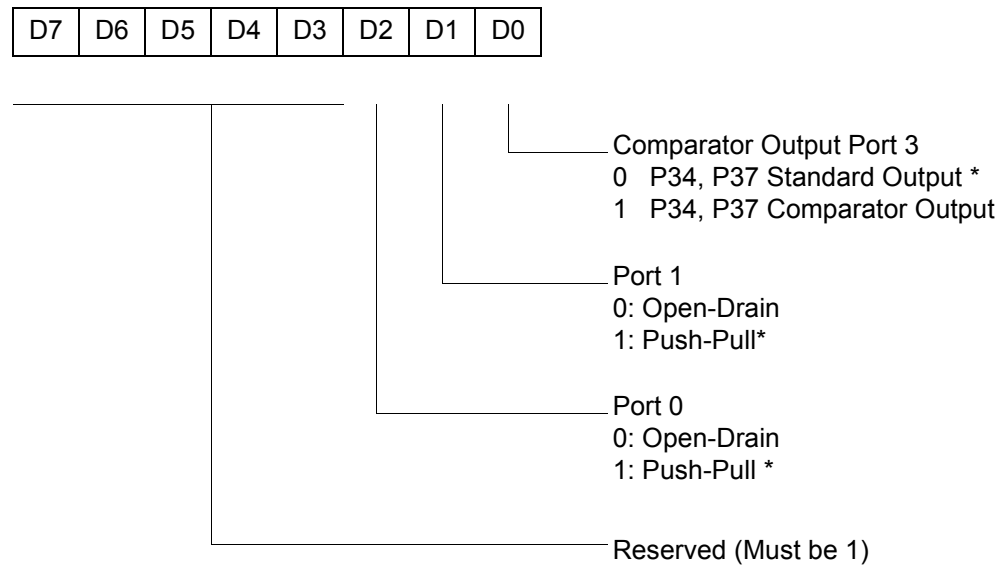
*Default setting after reset

Figure 42. Port Configuration Register (PCON)(0F)00H: Write Only)

R254 SPH(FEH)

D7	D6	D5	D4	D3	D2	D1	D0

General-Purpose Register

Figure 54. Stack Pointer High (FEH: Read/Write)

R255 SPL(FFH)

D7	D6	D5	D4	D3	D2	D1	D0

Stack Pointer Low
Byte (SP7–SP0)

Figure 55. Stack Pointer Low (FFH: Read/Write)

AC Characteristics

Figure 57 and Table 20 describe the Alternating Current (AC) characteristics.
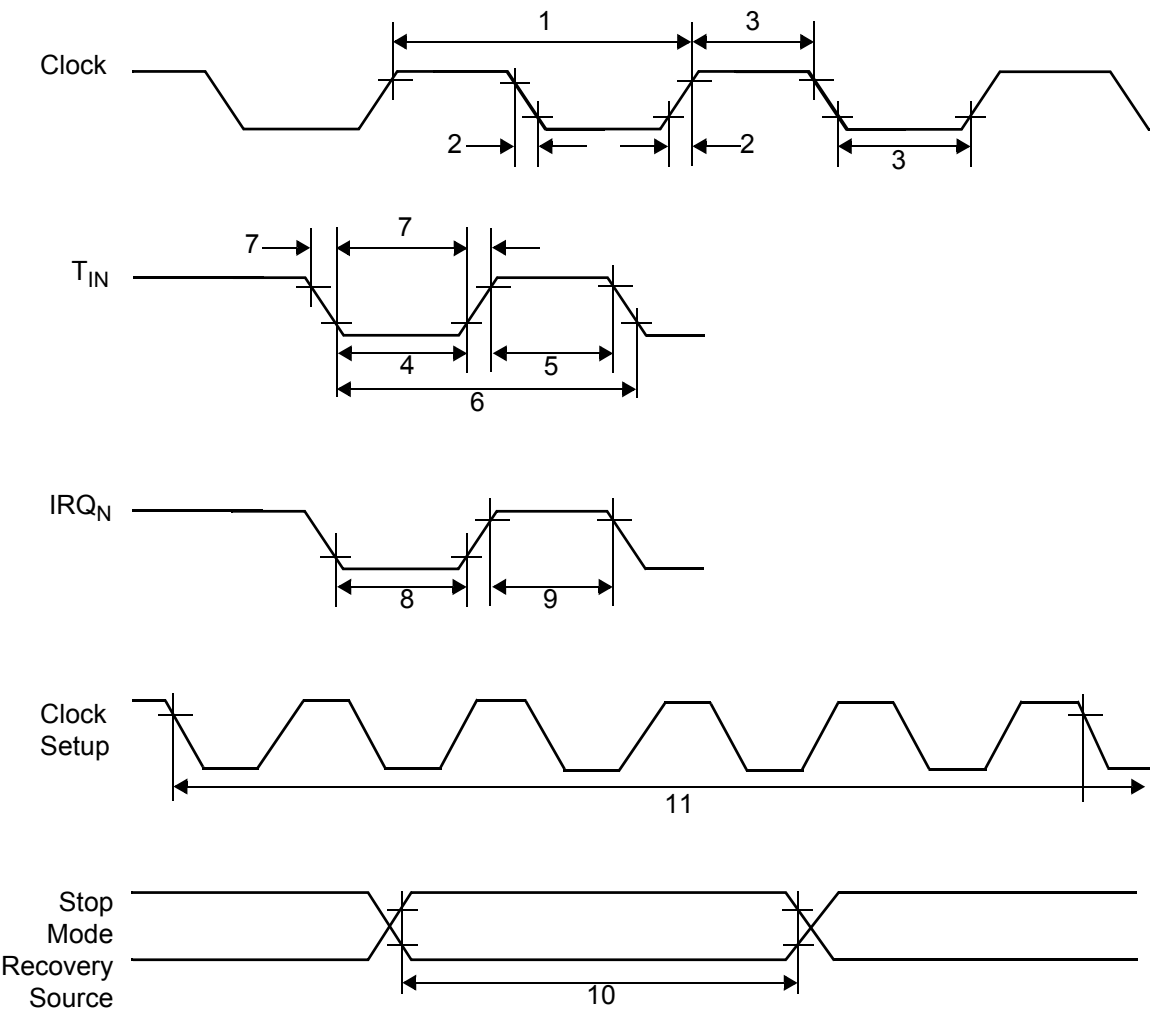
Figure 57. AC Timing Diagram

Packaging

Package information for all versions of Crimzon ZLP32300 is displayed in Figure 58 through Figure 65.

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	0.81	.015	.032
A2	3.25	3.68	.128	.145
B	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
e	2.54 BSC		.100 BSC	
eA	7.87	9.14	.310	.360
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

CONTROLLING DIMENSIONS : INCH
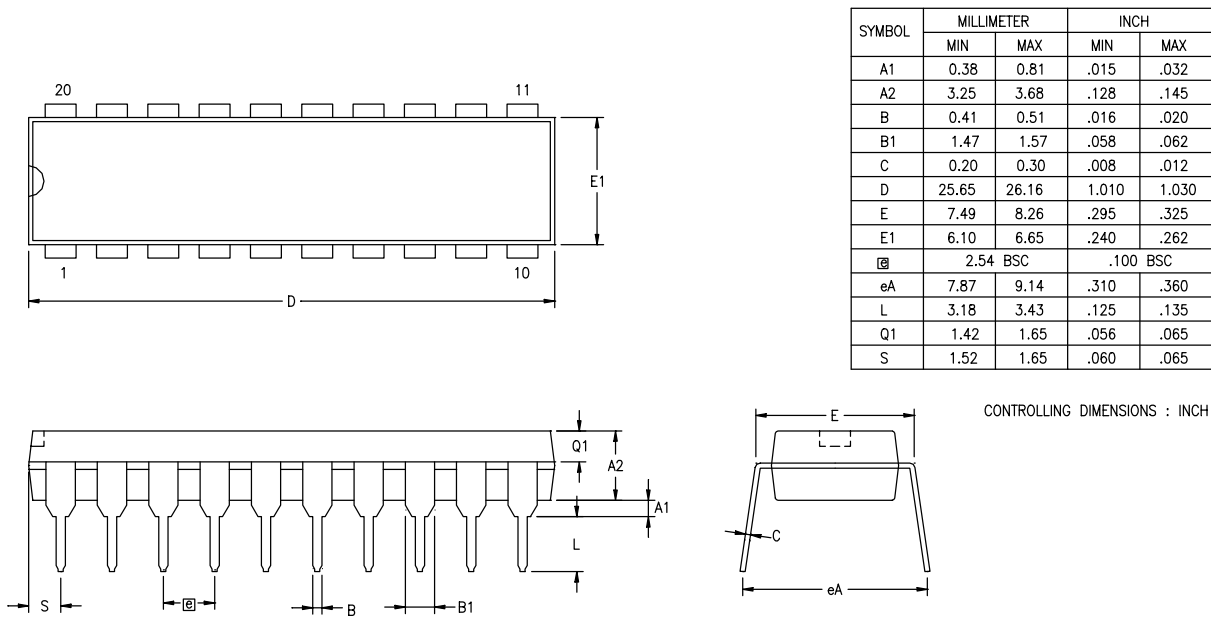
Figure 58. 20-Pin PDIP Package Diagram

Figure 59. 20-Pin SOIC Package Diagram
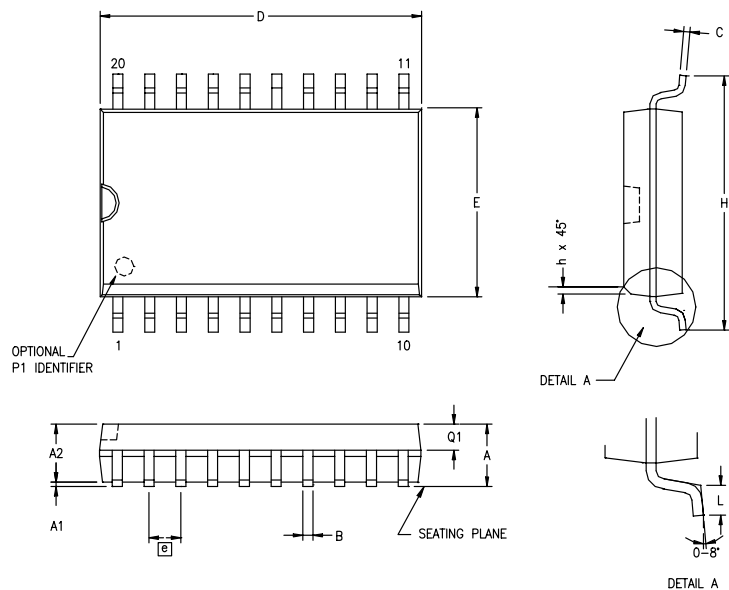
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	.496	.510
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 BSC	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Note: ZiLOG supplies both options for production. Component layout
PCB design should cover bigger option 01.

Figure 62. 28-Pin PDIP Package Diagram
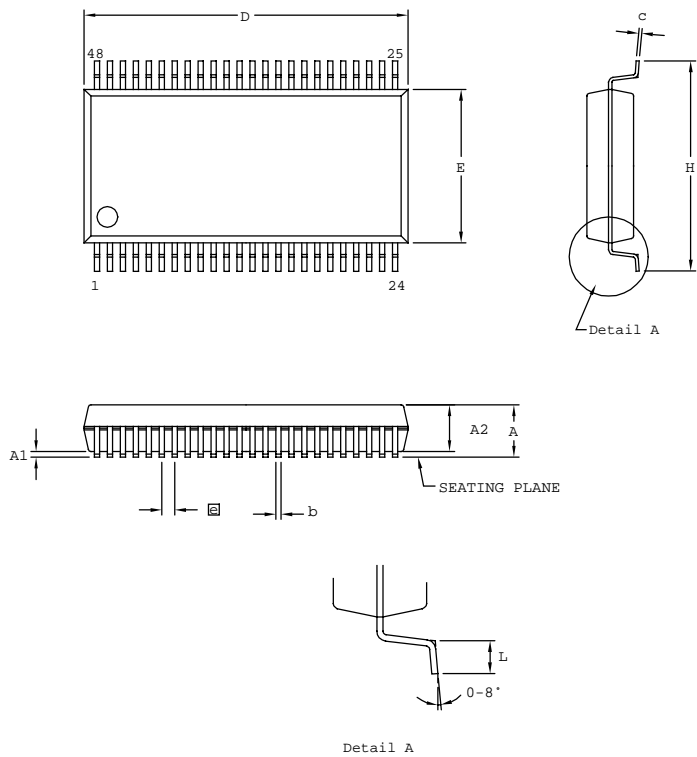
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.41	2.79	0.095	0.110
A1	0.23	0.38	0.009	0.015
A2	2.18	2.39	0.086	0.094
b	0.20	0.34	0.008	0.0135
c	0.13	0.25	0.005	0.010
D	15.75	16.00	0.620	0.630
E	7.39	7.59	0.291	0.299
e	0.635 BSC		0.025 BSC	
H	10.16	10.41	0.400	0.410
L	0.51	1.016	0.020	0.040

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

Figure 65. 48-Pin SSOP Package Design

Note: *Contact Zilog® on the actual bonding diagram and coordinate for chip-on-board assembly.*

Device	Part Number	Description
	ZLP32300P2008G	20-pin PDIP 8 K OTP
	ZLP32300S2008G	20-pin SOIC 8 K OTP
	ZLP32300H4804G	48-pin SSOP 4 K OTP
	ZLP32300P4004G	40-pin PDIP 4 K OTP
	ZLP32300H2804G	28-pin SSOP 4 K OTP
	ZLP32300P2804G	28-pin PDIP 4 K OTP
	ZLP32300S2804G	28-pin SOIC 4 K OTP
	ZLP32300H2004G	20-pin SSOP 4 K OTP
	ZLP32300P2004G	20-pin PDIP 4 K OTP
	ZLP32300S2004G	20-pin SOIC 4 K OTP
	ZLP323ICE01ZAC*	40-PDIP/48-SSOP Accessory Kit
	Note: *ZLP323ICE01ZAC has been replaced by an improved version, ZCRMZNICE02ZACG.	
	ZLP128ICE01ZEMG	In-Circuit Emulator
	Note: *ZLP128ICE01ZEMG has been replaced by an improved version, ZCRMZNICE01ZEMG.	
	ZCRMZNICE01ZEMG	Crimzon In-Circuit Emulator
	ZCRMZN00100KITG	Crimzon In-Circuit Emulator Development Kit
	ZCRMZNICE01ZACG	20-Pin Accessory Kit
	ZCRMZNICE02ZACG	40/48-Pin Accessory Kit

Notes
1. Replace C with G for Lead-Free Packaging.
2. Contact www.zilog.com for the die form.

For fast results, contact your local Zilog® sales office for assistance in ordering the part(s) desired.

Index

Numerics

A

B

C

D