Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, Serial Port
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w77l516a25fl

4. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
$\overline{EA}$	I	**EXTERNAL ACCESS ENABLE:** This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and data will not be present on the bus if $\overline{EA}$ pin is high. Otherwise they will be present on the bus.
$\overline{PSEN}$	O	**PROGRAM STORE ENABLE:** $\overline{PSEN}$ enables the external ROM data onto the Port 0 address/data bus during fetch and MOVC operations. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs from this pin.
ALE	O	**ADDRESS LATCH ENABLE:** ALE is used to enable the address latch that separates the address from the data on Port 0.
RST	I	**RESET:** A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	**CRYSTAL1:** This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	O	**CRYSTAL2:** This is the crystal oscillator output. It is the inversion of XTAL1.
V_{SS}	I	**GROUND:** Ground potential
V_{DD}	I	**POWER SUPPLY:** Supply voltage for operation.
P0.0–P0.7	I/O	**PORT 0:** Port 0 is an open-drain bi-directional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory. Port 0 has internal pull-up resisters enabled by software.
P1.0–P1.7	I/O	**PORT 1:** Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below: T2(P1.0): Timer/Counter 2 external count input T2EX(P1.1): Timer/Counter 2 Reload/Capture/Direction control RXD1(P1.2): Serial port 2 RXD TXD1(P1.3): Serial port 2 TXD INT2(P1.4): External Interrupt 2 $\overline{INT3}$ (P1.5): External Interrupt 3 INT4(P1.6): External Interrupt 4 $\overline{INT5}$ (P1.7): External Interrupt 5
P2.0–P2.7	I/O	**PORT 2:** Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory. The P2.6 and P2.7 also provide the alternate function /REBOOT which is H/W reboot from LD flash.

Pin Description, continued

SYMBOL	TYPE	DESCRIPTIONS
P3.0–P3.7	I/O	**PORT 3:** Port 3 is a bi-directional I/O port with internal pull-ups. All bits have alternate functions, which are described below: RXD(P3.0) : Serial Port 0 input TXD(P3.1) : Serial Port 0 output $\overline{INT0}$ (P3.2) : External Interrupt 0 $\overline{INT1}$ (P3.3) : External Interrupt 1 T0(P3.4) : Timer 0 External Input T1(P3.5) : Timer 1 External Input $\overline{WR}$ (P3.6) : External Data Memory Write Strobe $\overline{RD}$ (P3.7) : External Data Memory Read Strobe
P4.0–P4.3	I/O	**PORT 4:** Port 4 is a 4-bit bi-directional I/O port. The P4.0 also provides the alternate function $\overline{WAIT}$ which is the wait state control signal. The P4.3 also provide the alternate function /REBOOT which is H/W reboot from LD flash.

*** Note: TYPE** I: input, O: output, I/O: bi-directional.

新唐科技 NUVOTON INTELLECTUAL PROPERTY

Timers

The W77L516A has three 16-bit timers that are functionally similar to the timers of the 8052 family. When used as timers, they can be set to run at either 4 clocks or 12 clocks per count, thus providing the user with the option of operating in a mode that emulates the timing of the original 8052. The W77L516A has an additional feature, the watchdog timer. This timer is used as a System Monitor or as a very long time period timer.

Interrupts

The Interrupt structure in the W77L516A is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased. The W77L516A provides 12 interrupt resources with two priority level, including six external interrupt sources, timer interrupts, serial I/O interrupts.

Data Pointers

The original 8052 had only one 16-bit Data Pointer (DPL, DPH). In the W77L516A, there is an additional 16-bit Data Pointer (DPL1, DPH1). This new Data Pointer uses two SFR locations which were unused in the original 8052. In addition there is an added instruction, DEC DPTR (op-code A5H), which helps in improving programming flexibility for the user.

Power Management

Like the standard 80C52, the W77L516A also has IDLE and POWER DOWN modes of operation. The W77L516A provides a new Economy mode which allow user to switch the internal clock rate divided by either 4, 64 or 1024. In the IDLE mode, the clock to the CPU core is stopped while the timers, serial ports and interrupts clock continue to operate. In the POWER DOWN mode, all the clock are stopped and the chip operation is completely stopped. This is the lowest power consumption state.

On-chip Data SRAM

The W77L516A has 1K Bytes of data space SRAM which is read/write accessible and is memory mapped. This on-chip MOVX SRAM is reached by the MOVX instruction. It is not used for executable program memory. There is no conflict or overlap among the 256 bytes Scratchpad RAM and the 1K Bytes MOVX SRAM as they use different addressing modes and separate instructions. The on-chip MOVX SRAM is enabled by setting the DME0 bit in the PMR register. After a reset, the DME0 bit is cleared such that the on-chip MOVX SRAM is disabled, and all data memory spaces 0000H–FFFFH access to the external memory.

6. MEMORY ORGANIZATION

The W77L516A separates the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

Program Memory

The Program Memory on the standard 8052 can only be addressed to 64 Kbytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region. There is an auxiliary 4KB Flash EPROM bank (LDFLASH) resided user loader program for In-System Programming (ISP). APFLASH allows serial or parallel download according to user loader program in LDFLASH.

Data Memory

The W77L516A can access up to 64Kbytes of external Data Memory. This memory region is accessed by the MOVX instructions. Unlike the 8051 derivatives, the W77L516A contains on-chip 1K bytes MOVX SRAM of Data Memory, which can only be accessed by MOVX instructions. These 1K bytes of SRAM are between address 0000H and 03FFH. Access to the on-chip MOVX SRAM is optional under software control. When enabled by software, any MOVX instruction that uses this area will go to the on-chip RAM. MOVX addresses greater than 03FFH automatically go to external memory through Port 0 and 2. When disabled, the 1KB memory area is transparent to the system memory map. Any MOVX directed to the space between 0000H and FFFFH goes to the expanded bus on Port 0 and 2. This is the default condition. In addition, the W77L516A has the standard 256 bytes of on-chip Scratchpad RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing. Since the Scratchpad RAM is only 256 bytes, it can be used only when data contents are small. In the event that larger data contents are present, two selections can be used. One is on-chip MOVX SRAM , the other is the external Data Memory. The on-chip MOVX SRAM can only be accessed by a MOVX instruction, the same as that for external Data Memory. However, the on-chip RAM has the fastest access times.

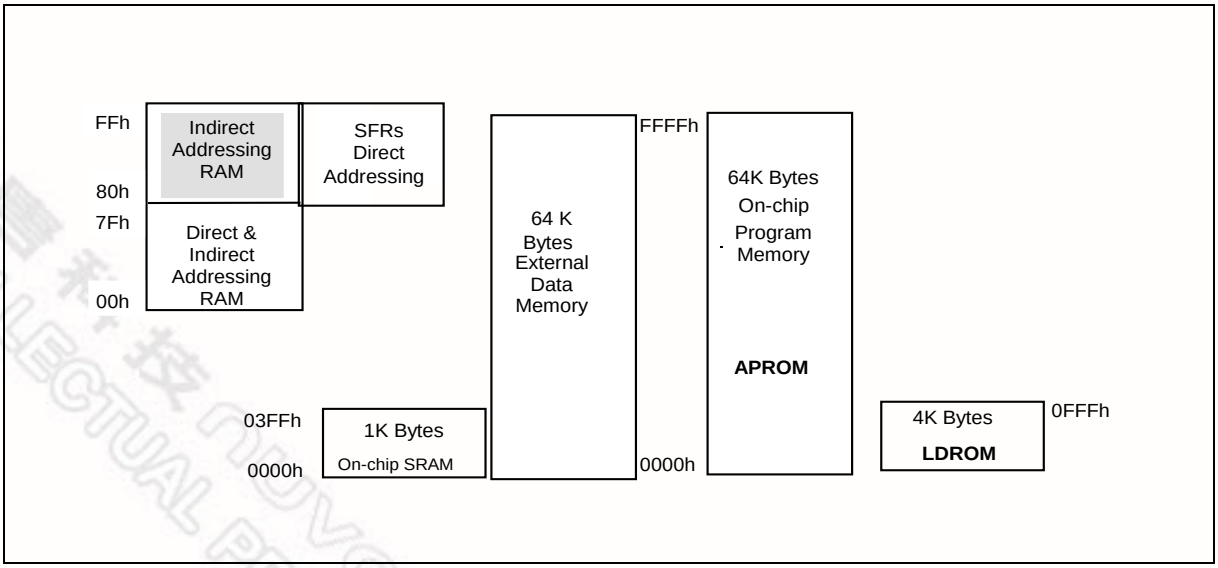

Figure 1. Memory Map

TIMER CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

TF1: Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.

TR1: Timer 1 run control: This bit is set or cleared by software to turn timer/counter on or off.

TF0: Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.

TR0: Timer 0 run control: This bit is set or cleared by software to turn timer/counter on or off.

IE1: Interrupt 1 edge detect: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.

IT1: Interrupt 1 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

IE0: Interrupt 0 edge detect: Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.

IT0: Interrupt 0 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C / $\overline{T}$	M1	M0	GATE	C / $\overline{T}$	M1	M0
			TIMER1				TIMER0	

Mnemonic: TMOD Address: 89h

GATE: Gating control: When this bit is set, Timer/counter x is enabled only while $\overline{INTx}$ pin is high and TRx control bit is set. When cleared, Timer x is enabled whenever TRx control bit is set.

C / $\overline{T}$: Timer or Counter Select: When cleared, the timer is incremented by internal clocks. When set , the timer counts high-to-low edges of the Tx pin.

PORT 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General purpose I/O port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. Some pins also have alternate input or output functions. This alternate functions are described below:

P1.0 : T2	External I/O for Timer/Counter 2
P1.1 : T2EX	Timer/Counter 2 Capture/Reload Trigger
P1.2 : RXD1	Serial Port 1 Receive
P1.3 : TXD1	Serial Port 1 Transmit
P1.4 : INT2	External Interrupt 2
P1.5 : $\overline{\text{INT3}}$	External Interrupt 3
P1.6 : INT4	External Interrupt 4
P1.7 : $\overline{\text{INT5}}$	External Interrupt 5

EXTERNAL INTERRUPT FLAG

Bit:	7	6	5	4	3	2	1	0
	IE5	IE4	IE3	IE2	-	-	-	-

Mnemonic: EXIF Address: 91h

IE5: External Interrupt 5 flag. Set by hardware when a falling edge is detected on $\overline{\text{INT5}}$.

IE4: External Interrupt 4 flag. Set by hardware when a rising edge is detected on INT4.

IE3: External Interrupt 3 flag. Set by hardware when a falling edge is detected on $\overline{\text{INT3}}$.

IE2: External Interrupt 2 flag. Set by hardware when a rising edge is detected on INT2.

PORT 4 CONTROL REGISTER A

Bit:	7	6	5	4	3	2	1	0
	P41M1	P41M0	P41C1	P41C0	P40M1	P40M0	P40C1	P40C0

Mnemonic: P4CONA Address: 92h

PORT 4 CONTROL REGISTER B

Bit:	7	6	5	4	3	2	1	0
	P43M1	P43M0	P43C1	P43C0	P42M1	P42M0	P42C1	P42C0

Mnemonic: P4CONB Address: 93h

P4.2 BASE ADDRESS LOW BYTE REGISTER

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P42AL Address: 9Ah

P4.2 BASE ADDRESS HIGH BYTE REGISTER

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P42AH Address: 9Bh

P4.3 BASE ADDRESS LOW BYTE REGISTER

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P43AL Address: 9Ch

P4.3 BASE ADDRESS HIGH BYTE REGISTER

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P43AH Address: 9Dh

ISP CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	SWRST/HWB	-	LDAP	-	-	-	LDSEL	ENP

Mnemonic: CHPCON Address: 9Fh

SWRST/HWB: Set this bit to launch a whole device reset that is same as asserting high to RST pin, micro controller will be back to initial state and clear this bit automatically. To read this bit, its alternate function to indicate the ISP hardware reboot mode is invoking when read it in high.

LDAP: This bit is Read Only. High: device is executing the program in LDFLASH. Low: device is executing the program in APFLASHs.

LDSEL: Loader program residence selection. Set to high to route the device fetching code from LDFLASH.

ENP: In System Programming Mode Enable. Set this be to launch the ISP mode. Device will operate ISP procedures, such as Erase, Program and Read operations, according to correlative SFRs settings. During ISP mode, device achieves ISP operations by the way of IDLE state. In the other

INTERRUPT PRIORITY

Bit:	7	6	5	4	3	2	1	0
	-	PS1	PT2	PS	PT1	PX1	PT0	PX0

Mnemonic: IP Address: B8h

IP.7: This bit is un-implemented and will read high.

PS1: This bit defines the Serial port 1 interrupt priority. PS = 1 sets it to higher priority level.

PT2: This bit defines the Timer 2 interrupt priority. PT2 = 1 sets it to higher priority level.

PS: This bit defines the Serial port 0 interrupt priority. PS = 1 sets it to higher priority level.

PT1: This bit defines the Timer 1 interrupt priority. PT1 = 1 sets it to higher priority level.

PX1: This bit defines the External interrupt 1 priority. PX1 = 1 sets it to higher priority level.

PT0: This bit defines the Timer 0 interrupt priority. PT0 = 1 sets it to higher priority level.

PX0: This bit defines the External interrupt 0 priority. PX0 = 1 sets it to higher priority level.

SLAVE ADDRESS MASK ENABLE

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SADEN Address: B9h

SADEN: This register enables the Automatic Address Recognition feature of the Serial port 0. When a bit in the SADEN is set to 1, the same bit location in SADDR will be compared with the incoming serial data. When SADEN.n is 0, then the bit becomes a "don't care" in the comparison. This register enables the Automatic Address Recognition feature of the Serial port 0. When all the bits of SADEN are 0, interrupt will occur for any incoming address.

SLAVE ADDRESS MASK ENABLE 1

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SADEN1 Address: BAh

SADEN1: This register enables the Automatic Address Recognition feature of the Serial port 1. When a bit in the SADEN1 is set to 1, the same bit location in SADDR1 will be compared with the incoming serial data. When SADEN1.n is 0, then the bit becomes a "don't care" in the comparison. This register enables the Automatic Address Recognition feature of the Serial port 1. When all the bits of SADEN1 are 0, interrupt will occur for any incoming address.

bit is 1, then timer 2 captures will occur when a falling edge is detected on T2EX pin if EXEN2 = 1.

TIMER 2 MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	HC5	HC4	HC3	HC2	T2CR	-	T2OE	DCEN

Mnemonic: T2MOD Address: C9h

HC5: Hardware Clear $\overline{INT5}$ flag. Setting this bit allows the flag of external interrupt 5 to be automatically cleared by hardware while entering the interrupt service routine.

HC4: Hardware Clear INT4 flag. Setting this bit allows the flag of external interrupt 4 to be automatically cleared by hardware while entering the interrupt service routine.

HC3: Hardware Clear $\overline{INT3}$ flag. Setting this bit allows the flag of external interrupt 3 to be automatically cleared by hardware while entering the interrupt service routine.

HC3: Hardware Clear INT2 flag. Setting this bit allows the flag of external interrupt 3 to be automatically cleared by hardware while entering the interrupt service routine.

T2CR: Timer 2 Capture Reset. In the Timer 2 Capture Mode this bit enables/disables hardware automatically reset Timer 2 while the value in TL2 and TH2 have been transferred into the capture register.

T2OE: Timer 2 Output Enable. This bit enables/disables the Timer 2 clock out function.

DCEN: Down Count Enable: This bit, in conjunction with the T2EX pin, controls the direction that timer 2 counts in 16-bit auto-reload mode.

TIMER 2 CAPTURE LSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Mnemonic: RCAP2L Address: CAh

RCAP2L:This register is used to capture the TL2 value when a timer 2 is configured in capture mode. RCAP2L is also used as the LSB of a 16-bit reload value when timer 2 is configured in auto-reload mode.

TIMER 2 CAPTURE MSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H Address: CBh

RCAP2H: This register is used to capture the TH2 value when a timer 2 is configured in capture mode. RCAP2H is also used as the MSB of a 16-bit reload value when timer 2 is configured in auto-reload mode.

WATCHDOG CONTROL

Bit:	7	6	5	4	3	2	1	0
	SMOD_1	POR	-	-	WDIF	WTRF	EWT	RWT

Mnemonic: WDCON Address: D8h

SMOD_1:This bit doubles the Serial Port 1 baud rate in mode 1, 2, and 3 when set to 1.

POR: Power-on reset flag. Hardware will set this flag on a power up condition. This flag can be read or written by software. A write by software is the only way to clear this bit once it is set.

WDIF: Watchdog Timer Interrupt Flag. If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software.

WTRF: Watchdog Timer Reset Flag. Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWT = 0, the watchdog timer will have no affect on this bit.

EWT: Enable Watchdog timer Reset. Setting this bit will enable the Watchdog timer Reset function.

RWT: Reset Watchdog Timer. This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWT before time-out will cause an interrupt, if EWDI (EIE.4) is set, and 512 clocks after that a watchdog timer reset will be generated if EWT is set. This bit is self-clearing by hardware.

The WDCON SFR is set to a 0x0x0xx0b on an external reset. WTRF is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF is not altered by an external reset. POR is set to 1 by a power-on reset. EWT is set to 0 on a Power-on reset and unaffected by other resets.

All the bits in this SFR have unrestricted read access. POR, EWT, WDIF and RWT require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register discription.

```
TA          EG    C7H
WDCON       REG   D8H
CKCON       REG   8EH
        MOV  TA,#AAH
        MOV  TA,#55H
        SETB  WDCON.0              ; Reset watchdog timer
        ORL  CKCON,#11000000B      ; Select 26 bits watchdog timer
        MOV  TA,#AAH
        MOV  TA,#55H
        ORL  WDCON,#00000010B      ; Enable watchdog
```

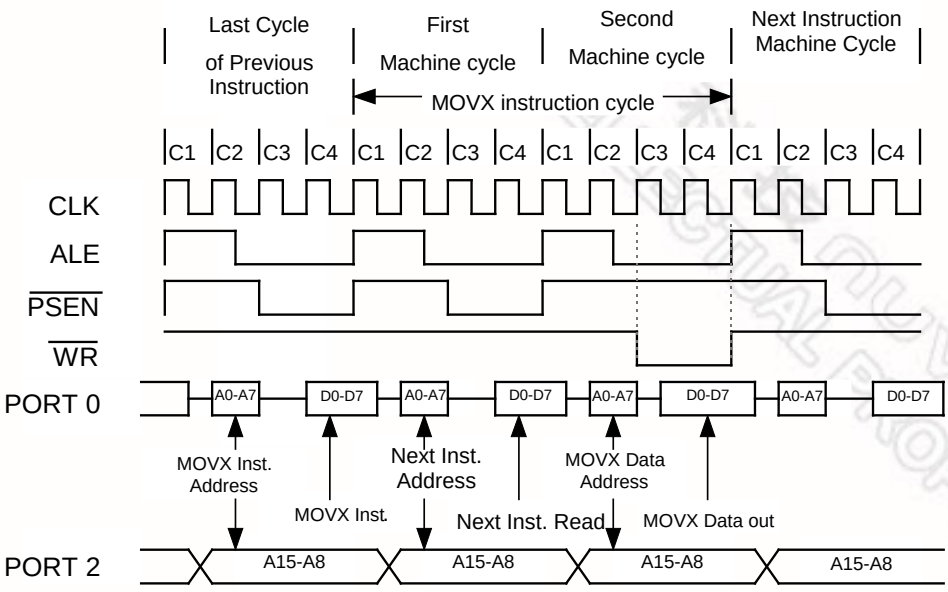

Figure 8. Data Memory Write with Stretch Value = 0

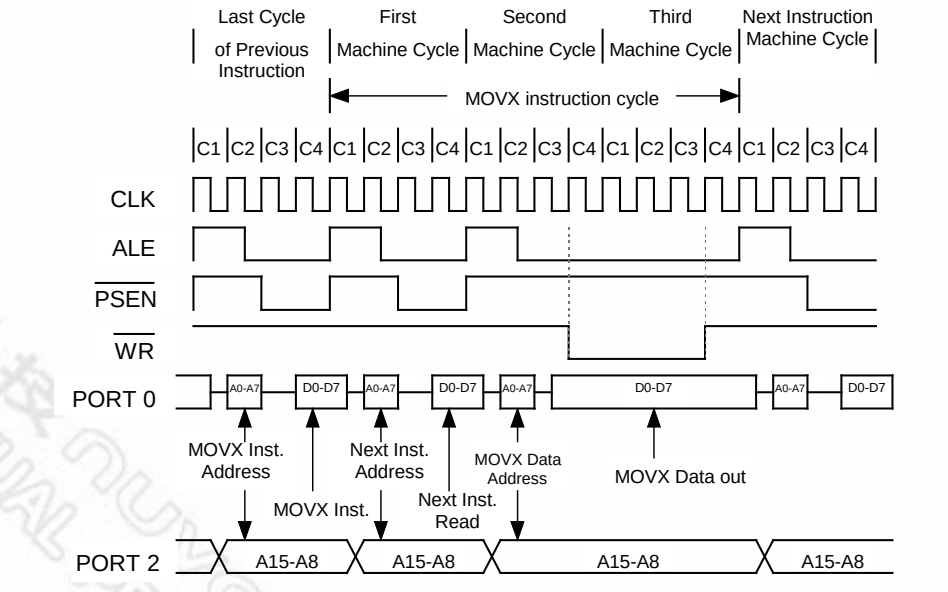

Figure 9. Data Memory Write with Stretch Value = 1

9. POWER MANAGEMENT

The W77L516A has several features that help the user to control the power consumption of the device. The power saving features are basically the POWER DOWN mode, ECONOMY mode and the IDLE mode of operation.

Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The ALE and PSEN pins are held high during the Idle state. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine(ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle mode.

The Idle mode can also be exited by activating the reset. The device can be put into reset either by applying a high on the external RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held high for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When the W77L516A is exiting from an Idle mode with a reset, the instruction following the one which put the device into Idle mode is not executed. So there is no danger of unexpected writes.

Economy Mode

The power consumption of microcontroller relates to operating frequency. The W77L516A offers a Economy mode to reduce the internal clock rate dynamically without external components. By default, one machine cycle needs 4 clocks. In Economy mode, software can select 4, 64 or 1024 clocks per machine cycle. It keeps the CPU operating at a acceptable speed but eliminates the power consumption. In the Idle mode, the clock of the core logic is stopped, but all clocked peripherals such as watchdog timer are still running at a rate of clock/4. In the Economy mode, all clocked peripherals run at the same reduced clocks rate as in core logic. So the Economy mode may provide a lower power consumption than idle mode.

Software invokes the Economy mode by setting the appropriate bits in the SFRs. Setting the bits CD0(PMR.6), CD1(PMR.7) decides the instruction cycle rate as below:

CD1	CD0	clocks/machine cycle
0	0	Reserved
0	1	4 (default)
1	0	64
1	1	1024

11. RESET STATE

Most of the SFRs and registers on the device will go to the same condition in the reset state. The Program Counter is forced to 0000h and is held there as long as the reset condition is applied. However, the reset state does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. However, the stack pointer is reset to 07h, and therefore the stack contents will be lost. The RAM contents will be lost if the V_{DD} falls below approximately 2V, as this is the minimum voltage level required for the RAM to operate normally. Therefore after a first time power on reset the RAM contents will be indeterminate. During a power fail condition, if the power falls below 2V, the RAM contents are lost.

After a reset most SFRs are cleared. Interrupts and Timers are disabled. The Watchdog timer is disabled if the reset source was a POR. The port SFRs have FFh written into them which puts the port pins in a high state. Port 0 floats as it does not have on-chip pull-ups.

Table 6. SFR Reset Value

SFR NAME	RESET VALUE	SFR NAME	RESET VALUE
P0	11111111b	IE	00000000b
SP	00000111b	SADDR	00000000b
DPL	00000000b	P3	11111111b
DPH	00000000b	IP	x0000000b
DPL1	00000000b	SADEN	00000000b
DPH1	00000000b	T2CON	00000000b
DPS	00000000b	T2MOD	00000x00b
PCON	00xx0000b	RCAP2L	00000000b
TCON	00000000b	RCAP2H	00000000b
TMOD	00000000b	TL2	00000000b
TL0	00000000b	TH2	00000000b
TL1	00000000b	TA	11111111b
TH0	00000000b	PSW	00000000b
TH1	00000000b	WDCON	0x0x0xx0b
CKCON	00000001b	ACC	00000000b
P1	11111111b	EIE	xxx00000b
P4CONA	00000000b	P4CONB	00000000b
P40AL	00000000b	P40AH	00000000b
P41AL	00000000b	P41AH	00000000b
P42AL	00000000b	P42AH	00000000b
P43Al	00000000b	P43AH	00000000b
CHPCON	00000000b	P4CSIN	00000000b
SFRCN	00111111b	SFRAL	00000000b
SFRAH	00000000b	SFRFD	00000000b

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Timer 2 interrupt is generated by a logical OR of the TF2 and the EXF2 flags. These flags are set by overflow or capture/reload events in the timer 2 operation. The hardware does not clear these flags when a timer 2 interrupt is executed. Software has to resolve the cause of the interrupt between TF2 and EXF2 and clear the appropriate flag.

The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit EIE.4, then an interrupt will occur.

The Serial block can generate interrupts on reception or transmission. There are two interrupt sources from the Serial block, which are obtained by the RI and TI bits in the SCON SFR and RI_1 and TI_1 in the SCON1 SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

All the bits that generate interrupts can be set or reset by hardware, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IE SFR. IE also has a global enable/disable bit EA, which can be cleared to disable all the interrupts, except PFI, at once.

Priority Level Structure

There are three priority levels for the interrupts, highest, high and low. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown below; the interrupts are numbered starting from the highest priority to the lowest.

Table 7. Priority structure of interrupts

SOURCE	FLAG	PRIORITY LEVEL
External Interrupt 0	IE0	1(highest)
Timer 0 Overflow	TF0	2
External Interrupt 1	IE1	3
Timer 1 Overflow	TF1	4
Serial Port	RI + TI	5
Timer 2 Overflow	TF2 + EXF2	6
Serial Port 1	RI_1 + TI_1	7
External Interrupt 2	IE2	8
External Interrupt 3	IE3	9
External Interrupt 4	IE4	10
External Interrupt 5	IE5	11
Watchdog Timer	WDIF	12 (lowest)

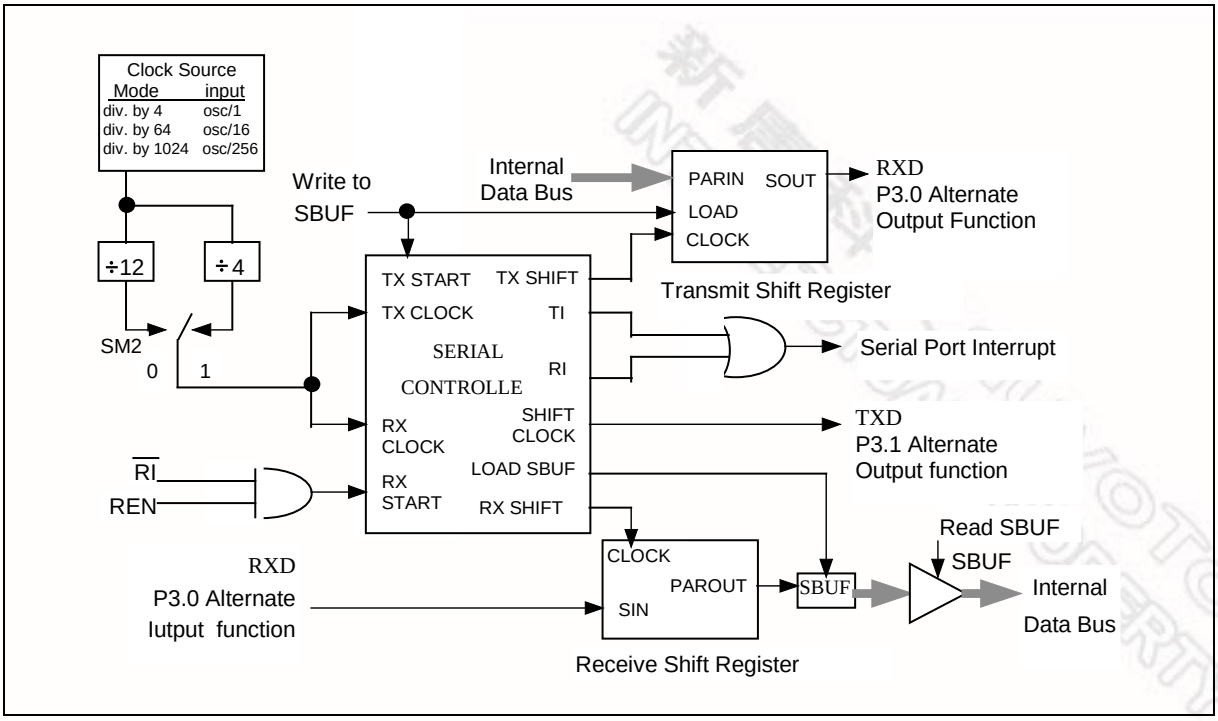

Figure 20. Serial Port Mode 1

The TI flag is set high in C1 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in C1 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

MODE 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counter after a write to SBUF.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counter.

divide by 16 counter, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 counter after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counter. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basis. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.

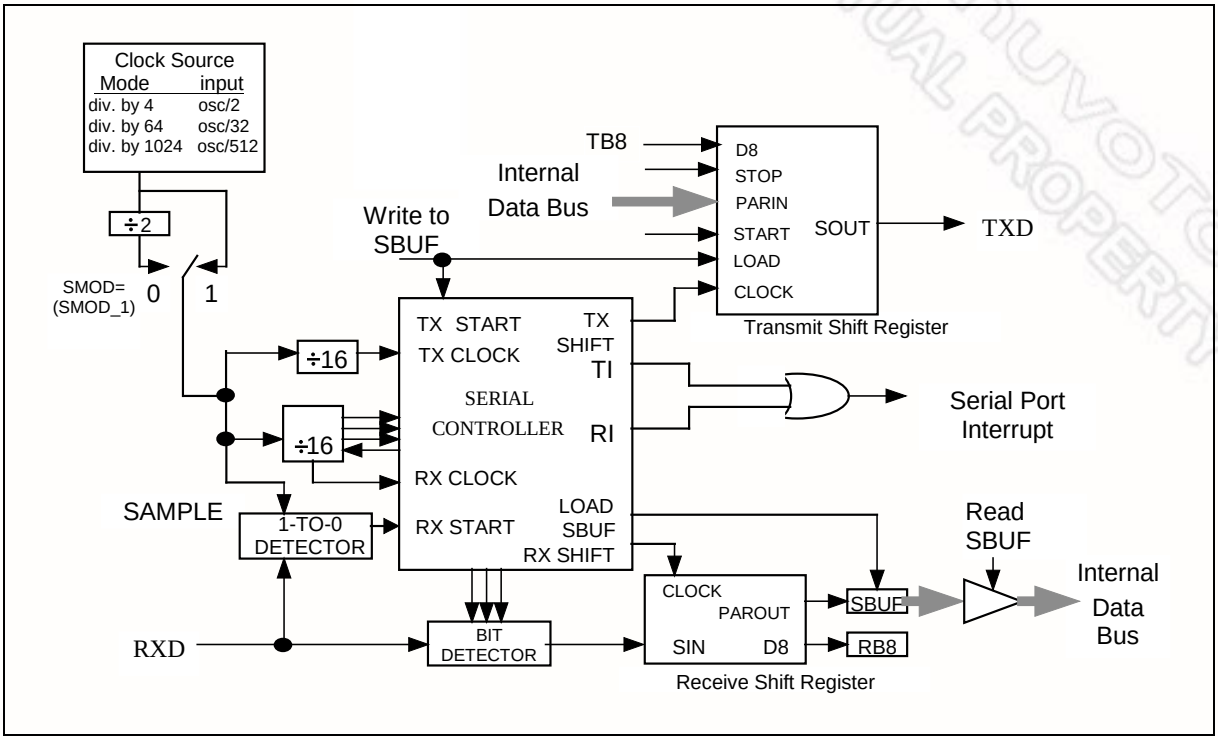

Figure 22. Serial Port Mode 2

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

DC Characteristics, continued

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Input High Voltage P0, P1, P2, P3, $\overline{EA}$	V_{IH1}	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.4	V_{DD} +0.2	V	V_{DD} = 2.7V
Input High Voltage RST	V_{IH2}	2.7	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	V_{DD} +0.2	V	V_{DD} = 2.7V
Input High Voltage XTAL1[*3]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.8	V_{DD} +0.2	V	V_{DD} = 2.7V
Sink current P1, P3	Isk1	6	9	mA	V_{DD} = 4.5V, V_{OL} = 0.45
		4.5	6.5	mA	V_{DD} = 2.7V, V_{OL} = 0.4
Sink current P0,P2, ALE, $\overline{PSEN}$	Isk2	10	14	mA	V_{DD} = 4.5V , V_{OL} = 0.45V
		6.5	9.5	mA	V_{DD} = 2.7V, V_{OL}=0.4
Source current P1, P3	Isr1	-180	-360	uA	V_{DD} = 4.5V, V_{OL} = 2.4V
		-75	-110	uA	V_{DD} = 2.7V, V_{OL} = 1.4V
Source current P0,P2, ALE, $\overline{PSEN}$	Isr2	-10	-18	mA	V_{DD} = 4.5V, V_{OL} = 2.4V
		-3	-8	mA	V_{DD} = 2.7V, V_{OL} = 1.4V
Output Low Voltage P1, P3	V_{OL1}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +6 mA
		-	0.4	V	V_{DD} = 2.7V, I_{OL} = +4.5 mA
Output Low Voltage P0, P2, ALE, $\overline{PSEN}$ [*2]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +10 mA
		-	0.4	V	V_{DD} = 2.7V, I_{OL} = +6.5 mA
Output High Voltage P1, P3	V_{OH1}	2.4	-	V	V_{DD} = 4.5V, I_{OH} = -180 μA
		1.4	-	V	V_{DD} = 2.7V, I_{OL} = -75 uA
Output High Voltage P0, P2, ALE, $\overline{PSEN}$ [*2]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V, I_{OH} = -10mA
		1.4	-	V	V_{DD} = 2.7V, I_{OL} = -3 mA

Notes:

*1. RST pin is a Schmitt trigger input.

*2. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

*3. XTAL1 is a CMOS input.

*4. Pins of P1, P2, P3 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when VIN approximates to 2V.

MOVX CHARACTERISTICS USING STRECH MEMORY CYCLES

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS	STRECH
Data Access ALE Pulse Width	t_{LLHL2}	$1.5t_{CLCL} - 5$ $2.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
Address Hold After ALE Low for MOVX write	t_{LLAX2}	$0.5t_{CLCL} - 5$		nS	
$\overline{RD}$ Pulse Width	t_{RLRH}	$2.0t_{CLCL} - 5$ $t_{MCS} - 10$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
$\overline{WR}$ Pulse Width	t_{WLWH}	$2.0t_{CLCL} - 5$ $t_{MCS} - 10$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2.0t_{CLCL} - 20$ $t_{MCS} - 20$	nS	$t_{MCS} = 0$ $t_{MCS}>0$
Data Hold after Read	t_{RHDX}	0		nS	
Data Float after Read	t_{RHDZ}		$t_{CLCL} - 5$ $2.0t_{CLCL} - 5$	nS	$t_{MCS} = 0$ $t_{MCS}>0$
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL} - 5$ $t_{MCS} + 2t_{CLCL} - 40$	nS	$t_{MCS} = 0$ $t_{MCS}>0$
Port 0 Address to Valid Data In	t_{AVDV1}		$3.0t_{CLCL} - 20$ $2.0t_{CLCL} - 5$	nS	$t_{MCS} = 0$ $t_{MCS}>0$
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL} - 5$ $1.5t_{CLCL} - 5$	$0.5t_{CLCL} + 5$ $1.5t_{CLCL} + 5$	nS	$t_{MCS} = 0$ $t_{MCS}>0$
Port 0 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL}	$t_{CLCL} - 5$ $2.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL} - 5$ $2.5t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
Data Valid to WR Transition	t_{QVWX}	-5 $1.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
Data Hold after Write	t_{WHQX}	$t_{CLCL} - 5$ $2.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
$\overline{RD}$ Low to Address Float	t_{RLAZ}		$0.5t_{CLCL} - 5$	nS	
$\overline{RD}$ or WR high to ALE high	t_{WHLH}	0 $1.0t_{CLCL} - 5$	10 $1.0t_{CLCL} + 5$	nS	$t_{MCS} = 0$ $t_{MCS}>0$

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the time period of t_{MCS} for each selection of the Stretch value.

```
;*******************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*******************************************************************************
        MOV  TA, #AAH
        MOV  TA, #55H
        MOV  CHPCON, #83H       ; SOFTWARE RESET. CPU will restart from APFLASH

ERROR_64K:
        DJNZ  R4,UPDATE_64K     ; IF ERROR OCCURS, REPEAT 3 TIMES.
.                               ; IN-SYST PROGRAMMING FAIL, USER'S PROCESS TO DEAL WITH IT.
                        .
                        .
                        .
```

22. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Nov. 10, 2003	-	Initial Issued
A2	March, 2005	2	Add lead free(ROHS) package part number
A3	April 19, 2005	86	Add Important Notice
A4	Aug 11, 2005	2, 4, 12 70	Add Port 0 pull-up resisters information Remove encrypt function of Security bits B2 description
A5	Dec 4, 2006	2	Remove all Leaded package parts
		73	Revise Operating speed to 20MHz
A6	February 1, 2007	15	Revise the Timer Mode Setting to “Mode 1: 16-bits, no prescale”.
A7	April 17, 2007	42	Revise that Power Down Mode is released by external interrupt configured as either level or edge detect.
A8	November 19, 2007	- 80	Remove W77LE516 part Change chapter 19.1 Figure A to crystal connections
A9	December 4, 2008	2	Revise 2nd item of Features from 25MHz to 20MHz.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, “Insecure Usage”.

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer’s risk, and in the event that third parties lay claims to Nuvoton as a result of customer’s Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

Please note that all data and specifications are subject to change without notice.
All the trademarks of products and companies mentioned in this datasheet belong to their respective owners.