Nuvoton Technology Corporation - W77L516A25PL Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, Serial Port
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w77l516a25pl

4. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
$\overline{EA}$	I	**EXTERNAL ACCESS ENABLE:** This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and data will not be present on the bus if $\overline{EA}$ pin is high. Otherwise they will be present on the bus.
$\overline{PSEN}$	O	**PROGRAM STORE ENABLE:** $\overline{PSEN}$ enables the external ROM data onto the Port 0 address/data bus during fetch and MOVC operations. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs from this pin.
ALE	O	**ADDRESS LATCH ENABLE:** ALE is used to enable the address latch that separates the address from the data on Port 0.
RST	I	**RESET:** A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	**CRYSTAL1:** This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	O	**CRYSTAL2:** This is the crystal oscillator output. It is the inversion of XTAL1.
V_{SS}	I	**GROUND:** Ground potential
V_{DD}	I	**POWER SUPPLY:** Supply voltage for operation.
P0.0–P0.7	I/O	**PORT 0:** Port 0 is an open-drain bi-directional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory. Port 0 has internal pull-up resisters enabled by software.
P1.0–P1.7	I/O	**PORT 1:** Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below: T2(P1.0): Timer/Counter 2 external count input T2EX(P1.1): Timer/Counter 2 Reload/Capture/Direction control RXD1(P1.2): Serial port 2 RXD TXD1(P1.3): Serial port 2 TXD INT2(P1.4): External Interrupt 2 $\overline{INT3}$ (P1.5): External Interrupt 3 INT4(P1.6): External Interrupt 4 $\overline{INT5}$ (P1.7): External Interrupt 5
P2.0–P2.7	I/O	**PORT 2:** Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory. The P2.6 and P2.7 also provide the alternate function /REBOOT which is H/W reboot from LD flash.

Timers

The W77L516A has three 16-bit timers that are functionally similar to the timers of the 8052 family. When used as timers, they can be set to run at either 4 clocks or 12 clocks per count, thus providing the user with the option of operating in a mode that emulates the timing of the original 8052. The W77L516A has an additional feature, the watchdog timer. This timer is used as a System Monitor or as a very long time period timer.

Interrupts

The Interrupt structure in the W77L516A is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased. The W77L516A provides 12 interrupt resources with two priority level, including six external interrupt sources, timer interrupts, serial I/O interrupts.

Data Pointers

The original 8052 had only one 16-bit Data Pointer (DPL, DPH). In the W77L516A, there is an additional 16-bit Data Pointer (DPL1, DPH1). This new Data Pointer uses two SFR locations which were unused in the original 8052. In addition there is an added instruction, DEC DPTR (op-code A5H), which helps in improving programming flexibility for the user.

Power Management

Like the standard 80C52, the W77L516A also has IDLE and POWER DOWN modes of operation. The W77L516A provides a new Economy mode which allow user to switch the internal clock rate divided by either 4, 64 or 1024. In the IDLE mode, the clock to the CPU core is stopped while the timers, serial ports and interrupts clock continue to operate. In the POWER DOWN mode, all the clock are stopped and the chip operation is completely stopped. This is the lowest power consumption state.

On-chip Data SRAM

The W77L516A has 1K Bytes of data space SRAM which is read/write accessible and is memory mapped. This on-chip MOVX SRAM is reached by the MOVX instruction. It is not used for executable program memory. There is no conflict or overlap among the 256 bytes Scratchpad RAM and the 1K Bytes MOVX SRAM as they use different addressing modes and separate instructions. The on-chip MOVX SRAM is enabled by setting the DME0 bit in the PMR register. After a reset, the DME0 bit is cleared such that the on-chip MOVX SRAM is disabled, and all data memory spaces 0000H–FFFFH access to the external memory.

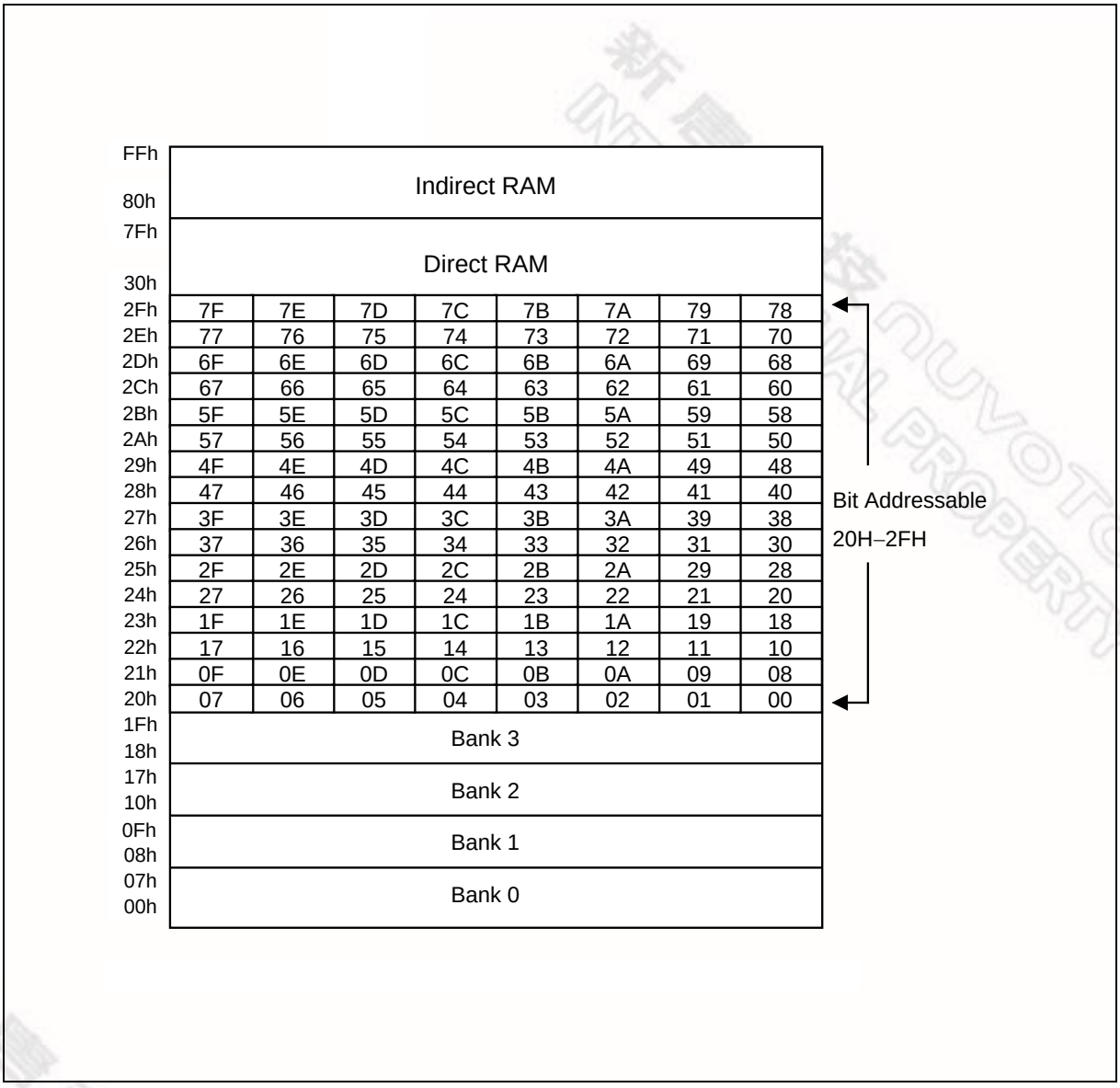


Figure 2. Scratchpad RAM/Register Addressing

This is the low byte of the new additional 16-bit data pointer that has been added to the W77L516A. The user can switch between DPL, DPH and DPL1, DPH1 simply by setting register DPS = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH. If they are not required they can be used as conventional register locations by the user.

DATA POINTER HIGH1

Bit:	7	6	5	4	3	2	1	0
	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0

Mnemonic: DPH1 Address: 85h

This is the high byte of the new additional 16-bit data pointer that has been added to the W77L516A. The user can switch between DPL, DPH and DPL1, DPH1 simply by setting register DPS = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH. If they are not required they can be used as conventional register locations by the user.

DATA POINTER SELECT

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DPS.0

Mnemonic: DPS Address: 86h

DPS.0: This bit is used to select either the DPL,DPH pair or the DPL1,DPH1 pair as the active Data Pointer. When set to 1, DPL1, DPH1 will be selected, otherwise DPL,DPH will be selected.

DPS.1-7:These bits are reserved, but will read 0.

POWER CONTROL

Bit:	7	6	5	4	3	2	1	0
	SM0D	SMOD0	-	-	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

SMOD : This bit doubles the serial port baud rate in mode 1, 2, and 3 when set to 1.

SMOD0: Framing Error Detection Enable: When SMOD0 is set to 1, then SCON.7(SCON1.7) indicates a Frame Error and acts as the FE(FE_1) flag. When SMOD0 is 0, then SCON.7(SCON1.7) acts as per the standard 8052 function.

GF1-0: These two bits are general purpose user flags.

PD: Setting this bit causes the W77L516A to go into the POWER DOWN mode. In this mode all the clocks are stopped and program execution is frozen.

IDL: Setting this bit causes the W77L516A to go into the IDLE mode. In this mode the clocks to the CPU are stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0

Mnemonic: CKCON Address: 8Eh

WD1-0: Watchdog timer mode select bits: These bits determine the time-out period for the watchdog timer. In all four time-out options the reset time-out is 512 clocks more than the interrupt time-out period.

WD1	WD0	INTERRUPT TIME-OUT	RESET TIME-OUT
0	0	2^{17}	2^{17} + 512
0	1	2^{20}	2^{20} + 512
1	0	2^{23}	2^{23} + 512
1	1	2^{26}	2^{26} + 512

T2M: Timer 2 clock select: When T2M is set to 1, timer 2 uses a divide by 4 clock, and when set to 0 it uses a divide by 12 clock.

T1M: Timer 1 clock select: When T1M is set to 1, timer 1 uses a divide by 4 clock, and when set to 0 it uses a divide by 12 clock.

T0M: Timer 0 clock select: When T0M is set to 1, timer 0 uses a divide by 4 clock, and when set to 0 it uses a divide by 12 clock.

MD2-0: Stretch MOVX select bits: These three bits are used to select the stretch value for the MOVX instruction. Using a variable MOVX length enables the user to access slower external memory devices or peripherals without the need for external circuits. The $\overline{RD}$ or $\overline{WR}$ strobe will be stretched by the selected interval. When accessing the on-chip SRAM, the MOVX instruction is always in 2 machine cycles regardless of the stretch setting. By default, the stretch has value of 1. If the user needs faster accessing, then a stretch value of 0 should be selected.

MD2	MD1	MD0	Stretch value	MOVX duration
0	0	0	0	2 machine cycles
0	0	1	1	3 machine cycles *(Default)*
0	1	0	2	4 machine cycles
0	1	1	3	5 machine cycles
1	0	0	4	6 machine cycles
1	0	1	5	7 machine cycles
1	1	0	6	8 machine cycles
1	1	1	7	9 machine cycles

PORT 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General purpose I/O port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. Some pins also have alternate input or output functions. This alternate functions are described below:

P1.0 : T2	External I/O for Timer/Counter 2
P1.1 : T2EX	Timer/Counter 2 Capture/Reload Trigger
P1.2 : RXD1	Serial Port 1 Receive
P1.3 : TXD1	Serial Port 1 Transmit
P1.4 : INT2	External Interrupt 2
P1.5 : $\overline{\text{INT3}}$	External Interrupt 3
P1.6 : INT4	External Interrupt 4
P1.7 : $\overline{\text{INT5}}$	External Interrupt 5

EXTERNAL INTERRUPT FLAG

Bit:	7	6	5	4	3	2	1	0
	IE5	IE4	IE3	IE2	-	-	-	-

Mnemonic: EXIF Address: 91h

IE5: External Interrupt 5 flag. Set by hardware when a falling edge is detected on $\overline{\text{INT5}}$.

IE4: External Interrupt 4 flag. Set by hardware when a rising edge is detected on INT4.

IE3: External Interrupt 3 flag. Set by hardware when a falling edge is detected on $\overline{\text{INT3}}$.

IE2: External Interrupt 2 flag. Set by hardware when a rising edge is detected on INT2.

PORT 4 CONTROL REGISTER A

Bit:	7	6	5	4	3	2	1	0
	P41M1	P41M0	P41C1	P41C0	P40M1	P40M0	P40C1	P40C0

Mnemonic: P4CONA Address: 92h

PORT 4 CONTROL REGISTER B

Bit:	7	6	5	4	3	2	1	0
	P43M1	P43M0	P43C1	P43C0	P42M1	P42M0	P42C1	P42C0

Mnemonic: P4CONB Address: 93h

BIT NAME	FUNCTION
P4xM1, P4xM0	Port 4 alternate modes. =00: Mode 0. P4.x is a general purpose I/O port which is the same as Port 1. =01: Mode 1. P4.x is a Read Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0. =10: Mode 2. P4.x is a Write Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0. =11: Mode 3. P4.x is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0
P4xC1,P4xC0	Port 4 Chip-select Mode address comparison: =00: Compare the full address (16 bits length) with the base address registers P4xAH and P4xAL. =01: Compare the 15 high bits (A15-A1) of address bus with the base address registers P4xAH and P4xAL. =10: Compare the 14 high bits (A15-A2) of address bus with the base address registers P4xAH and P4xAL. =11: Compare the 8 high bits (A15-A8) of address bus with the base address registers P4xAH and P4xAL.

P4.0 BASE ADDRESS LOW BYTE REGISTER

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P40AL Address: 94h

P4.0 BASE ADDRESS HIGH BYTE REGISTER

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P40AH Address: 95h

P4.1 BASE ADDRESS LOW BYTE REGISTER

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P41AL Address: 96h

P4.1 BASE ADDRESS HIGH BYTE REGISTER

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P41AH Address: 97h

SERIAL PORT CONTROL

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

SM0/FE: Serial port 0, Mode 0 bit or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.

SM1: Serial port Mode bit 1:

SM0	SM1	Mode	Description	Length	Baud rate
0	0	0	Synchronous	8	4/12 Tclk
0	1	1	Asynchronous	10	Variable
1	0	2	Asynchronous	11	64/32 Tclk
1	1	3	Asynchronous	11	Variable

SM2: Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.

REN: Receive enable: When set to 1 serial reception is enabled, otherwise reception is disabled.

TB8: This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.

RB8: In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.

TI: Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.

RI: Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SERIAL DATA BUFFER

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

SBUF.7-0: Serial data on the serial port 0 is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

words, device is not indeed in IDLE mode is set bit PCON.1 while ISP is enabled. Clear this bit to disable ISP mode, device get back to normal operation including IDLE state.

Software Reset

Set CHPCON = 0X83, timer and enter IDLE mode. CPU will reset and restart from APFLASH after time out.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

P2.7-0: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.

PORT 4 CHIP-SELECT POLARITY

Bit:	7	6	5	4	3	2	1	0
	P43INV	P42INV	P42INV	P40INV	-	-	-	P0UP

Mnemonic: P4CSIN Address: A2h

P4xINV: The active polarity of P4.x when set it as chip-select signal. High = Active High. Low = Active Low.

P0UP: Enable Port 0 weak pull up.

PORT 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: A5h

P4.3-0: Port 4 is a bi-directional I/O port with internal pull-ups. Port 4 can not use bit-addressable instruction (SETB or CLR).

INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	EA	ES1	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

EA: Global enable. Enable/disable all interrupts except for PFI.
ES1: Enable Serial Port 1 interrupt.
ET2: Enable Timer 2 interrupt.
ES: Enable Serial Port 0 interrupt.
ET1: Enable Timer 1 interrupt
EX1: Enable external interrupt 1
ET0: Enable Timer 0 interrupt
EX0: Enable external interrupt 0

INTERRUPT PRIORITY

Bit:	7	6	5	4	3	2	1	0
	-	PS1	PT2	PS	PT1	PX1	PT0	PX0

Mnemonic: IP Address: B8h

IP.7: This bit is un-implemented and will read high.

PS1: This bit defines the Serial port 1 interrupt priority. PS = 1 sets it to higher priority level.

PT2: This bit defines the Timer 2 interrupt priority. PT2 = 1 sets it to higher priority level.

PS: This bit defines the Serial port 0 interrupt priority. PS = 1 sets it to higher priority level.

PT1: This bit defines the Timer 1 interrupt priority. PT1 = 1 sets it to higher priority level.

PX1: This bit defines the External interrupt 1 priority. PX1 = 1 sets it to higher priority level.

PT0: This bit defines the Timer 0 interrupt priority. PT0 = 1 sets it to higher priority level.

PX0: This bit defines the External interrupt 0 priority. PX0 = 1 sets it to higher priority level.

SLAVE ADDRESS MASK ENABLE

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SADEN Address: B9h

SADEN: This register enables the Automatic Address Recognition feature of the Serial port 0. When a bit in the SADEN is set to 1, the same bit location in SADDR will be compared with the incoming serial data. When SADEN.n is 0, then the bit becomes a "don't care" in the comparison. This register enables the Automatic Address Recognition feature of the Serial port 0. When all the bits of SADEN are 0, interrupt will occur for any incoming address.

SLAVE ADDRESS MASK ENABLE 1

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SADEN1 Address: BAh

SADEN1: This register enables the Automatic Address Recognition feature of the Serial port 1. When a bit in the SADEN1 is set to 1, the same bit location in SADDR1 will be compared with the incoming serial data. When SADEN1.n is 0, then the bit becomes a "don't care" in the comparison. This register enables the Automatic Address Recognition feature of the Serial port 1. When all the bits of SADEN1 are 0, interrupt will occur for any incoming address.

7. INSTRUCTION

The W77L516A executes all the instructions of the standard 8032 family. The operation of these instructions, their effect on the flag bits and the status bits is exactly the same. However, timing of these instructions is different. The reason for this is two fold. Firstly, in the W77L516A, each machine cycle consists of 4 clock periods, while in the standard 8032 it consists of 12 clock periods. Also, in the W77L516A there is only one fetch per machine cycle i.e. 4 clocks per fetch, while in the standard 8032 there can be two fetches per machine cycle, which works out to 6 clocks per fetch.

The advantage the W77L516A has is that since there is only one fetch per machine cycle, the number of machine cycles in most cases is equal to the number of operands that the instruction has. In case of jumps and calls there will be an additional cycle that will be needed to calculate the new address. But overall the W77L516A reduces the number of dummy fetches and wasted cycles, thereby improving efficiency as compared to the standard 8032.

Table 2. Instructions that affect Flag settings

INSTRUCTION	CARRY	OVERFLOW	AUXILIARY CARRY	INSTRUCTION	CARRY	OVERFLOW	AUXILIARY CARRY
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	0	X		ANL C, bit	X		
DIV	0	X		ORL C, bit	X		
DA A	X			ORL C, bit	X		
RRC A	X			MOV C, bit	X		
RLC A	X			CJNE	X		
SETB C	1						

A "X" indicates that the modification is as per the result of instruction.

The selection of instruction rate is going to take effect after a delay of one instruction cycle. Switching to divide by 64 or 1024 mode must first go from divide by 4 mode. This means software can not switch directly between clock/64 and clock/1024 mode. The CPU has to return clock/4 mode first, then go to clock/64 or clock/1024 mode.

In Economy mode, the serial port can not receive/transmit data correctly because the baud rate is changed. In some systems, the external interrupts may require the fastest process such that the reducing of operating speed is restricted. In order to solve these dilemmas, the W77L516A offers a switchback feature which allows the CPU back to clock/4 mode immediately when triggered by serial operation or external interrupts. The switchback feature is enabled by setting the SWB bit (PMR.5). A serial port reception/transmission or qualified external interrupt which is enabled and acknowledged without block conditions will cause CPU to return to divide by 4 mode. For the serial port reception, a switchback is generated by a falling edge associated with start bit if the serial port reception is enabled. When a serial port transmission, an instruction which writes a byte of data to serial port buffer will cause a switchback to ensure the correct transmission. The switchback feature is unaffected by serial port interrupt flags. After a switchback is generated, the software can manually return the CPU to Economy mode. Note that the modification of clock control bits CD0 and CD1 will be ignored during serial port transmit/receive when switchback is enabled. The Watchdog timer reset, power-on/fail reset or external reset will force the CPU to return to divide by 4 mode.

Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. In this state the ALE and $\overline{\text{PSEN}}$ pins are pulled low. The port pins output the values held by their respective SFRs.

The W77L516A will exit the Power Down mode with a reset or by an external interrupt pin enabled as either level or edge detect. An external reset can be used to exit the Power down state. The high on RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode.

The W77L516A can be woken from the Power Down mode by forcing an external interrupt pin activated, provided the corresponding interrupt is enabled, while the global enable(EA) bit is set. If these conditions are met, then the low level on the external pin re-starts the oscillator. Then device executes the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after the one which put the device into Power Down mode and continues from there.

Table 5. Status of external pins during Idle and Power Down

MODE	PROGRAM MEMORY	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

10. RESET CONDITIONS

Interrupt Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{INT0}$ to $\overline{INT5}$, they are sampled at C3 of every machine cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine cycle in which overflow has occurred. These flag values are polled only in the next machine cycle. If a request is active and all three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine cycles to be completed. Thus there is a minimum time of five machine cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the service routine currently being executed. If the polling cycle is not the last machine cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the W77L516A is performing a write to IE, IP, EIE or EIP and then executes a MUL or DIV instruction. From the time an interrupt source is activated, the longest reaction time is 12 machine cycles. This includes 1 machine cycle to detect the interrupt, 2 machine cycles to complete the IE, IP, EIE or EIP access, 5 machine cycles to complete the MUL or DIV instruction and 4 machine cycles to complete the hardware LCALL to the interrupt vector location.

Thus in a single-interrupt system the interrupt response time will always be more than 5 machine cycles and not more than 12 machine cycles. The maximum latency of 12 machine cycle is 48 clock cycles. Note that in the standard 8051 the maximum latency is 8 machine cycles which equals 96 machine cycles. This is a 50% reduction in terms of clock periods.

12. PROGRAMMABLE TIMERS/COUNTERS

The W77L516A has three 16-bit programmable timer/counters and one programmable Watchdog timer. The Watchdog timer is operationally quite different from the other two timers.

TIMER/COUNTERS 0 & 1

The W77L516A has two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

Time-Base Selection

The W77L516A gives the user two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on the W77L516A and the standard 8051 can be matched. This is the default mode of operation of the W77L516A timers. The user also has the option to count in the turbo mode, where the timers will increment at the rate of 1/4 clock speed. This will straight-away increase the counting speed three times. This selection is done by the T0M and T1M bits in CKCON SFR. A reset sets these bits to 0, and the timers then operate in the standard 8051 mode. The user should set these bits to 1 if the timers are to operate in turbo mode.

MODE 0

In Mode 0, the timer/counters act as a 8 bit counter with a 5 bit, divide by 32 pre-scale. In this mode we have a 13 bit timer/counter. The 13 bit counter consists of 8 bits of THx and 5 lower bits of TLx. The upper 3 bits of TLx are ignored.

The negative edge of the clock increments the count in the TLx register. When the fifth bit in TLx moves from 1 to 0, then the count in the THx register is incremented. When the count in THx moves from FFh to 00h, then the overflow flag TFx in TCON SFR is set. The counted input is enabled only if TRx is set and either GATE = 0 or $\overline{INTx}$ = 1. When $C/\overline{T}$ is set to 0, then it will count clock cycles, and if $C/\overline{T}$ is set to 1, then it will count 1 to 0 transitions on T0 (P3.4) for timer 0 and T1 (P3.5) for timer 1. When the 13 bit count reaches 1FFFh the next count will cause it to roll-over to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupts will occur. Note that when

watchdog timer reset is enabled and the watchdog interrupt may be disabled. If any errant code is executed now, then the reset watchdog timer instructions will not be executed at the required instants and watchdog reset will occur.

The watchdog time-out selection will result in different time-out values depending on the clock speed. The reset, when enabled, will occur 512 clocks after the time-out has occurred.

Table 9. Time-out values for the Watchdog timer

WD1	WD0	WATCHDOG INTERVAL	NUMBER OF CLOCKS	TIME @ 1.8432 MHZ	TIME @ 10 MHZ	TIME @ 25 MHZ
0	0	2^{17}	131072	71.11 mS	13.11 mS	5.24 mS
0	1	2^{20}	1048576	568.89 mS	104.86 mS	41.94 mS
1	0	2^{23}	8388608	4551.11 mS	838.86 mS	335.54 mS
1	1	2^{26}	67108864	36408.88 mS	6710.89 mS	2684.35 mS

The Watchdog timer will de disabled by a power-on/fail reset. The Watchdog timer reset does not disable the watchdog timer, but will restart it. In general, software should restart the timer to put it into a known state.

The control bits that support the Watchdog timer are discussed below.

WATCHDOG CONTROL

WDIF: WDCON.3 - Watchdog Timer Interrupt flag. This bit is set whenever the time-out occurs in the watchdog timer. If the Watchdog interrupt is enabled (EIE.4), then an interrupt will occur (if the global interrupt enable is set and other interrupt requirements are met). Software or any reset can clear this bit.

WTRF: WDCON.2 - Watchdog Timer Reset flag. This bit is set whenever a watchdog reset occurs. This bit is useful for determined the cause of a reset. Software must read it, and clear it manually. A Power-fail reset will clear this bit. If EWT = 0, then this bit will not be affected by the watchdog timer.

EWT: WDCON.1 - Enable Watchdog timer Reset. This bit when set to 1 will enable the Watchdog timer reset function. Setting this bit to 0 will disable the Watchdog timer reset function, but will leave the timer running.

RWT: WDCON.0 - Reset Watchdog Timer. This bit is used to clear the Watchdog timer and to restart it. This bit is self-clearing, so after the software writes 1 to it the hardware will automatically clear it. If the Watchdog timer reset is enabled, then the RWT has to be set by the user within 512 clocks of the time-out. If this is not done then a Watchdog timer reset will occur.

18. ELECTRICAL CHARACTERISTIC

18.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITION	RATING	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	+70	°C
Storage Temperature	Tst	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

18.2 DC Characteristics

(T_A = 25°C, unless otherwise specified.)

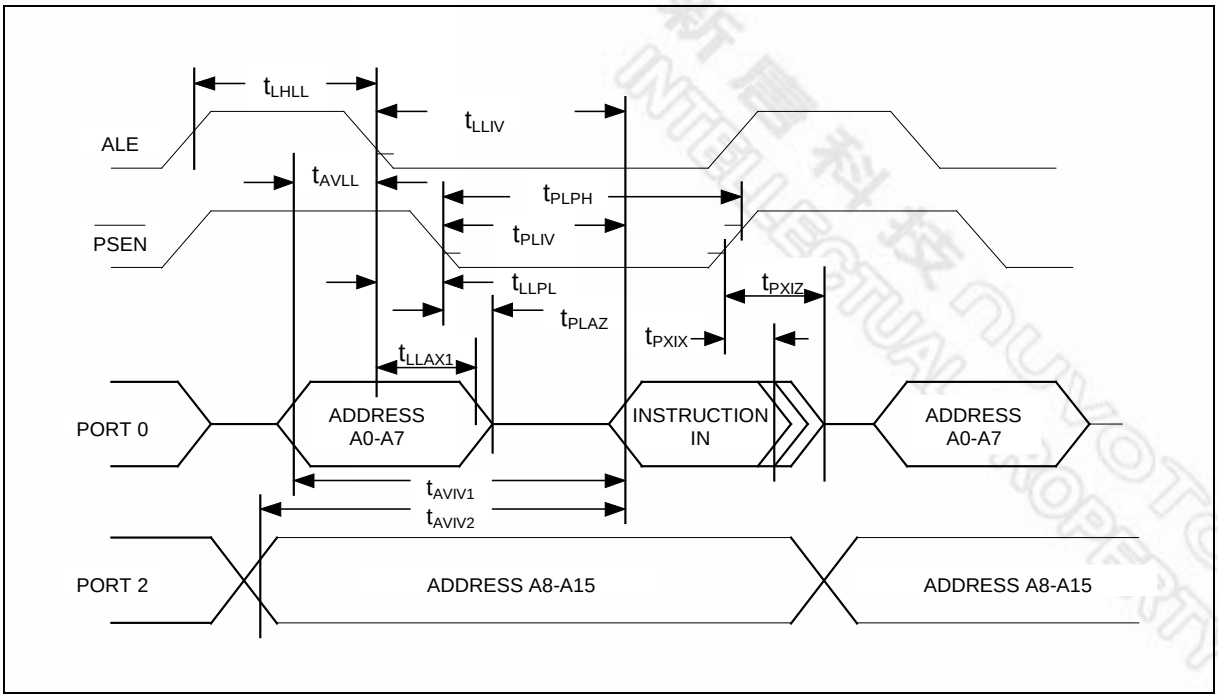
PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Operating Voltage	V_{DD}	2.7	5.5	V	Without ISP
		3.0	5.5	V	With ISP
Operating Current	I_{DD}	-	30	mA	V_{DD} = 5.5V, Fosc = 20 MHz
			6.5	mA	V_{DD} = 2.7V, Fosc = 12 MHz
Idle Current	I_{IDLE}	-	24	mA	V_{DD} = 5.5V, Fosc=20 MHz
			5.8	mA	V_{DD} = 2.7V, Fosc=12 MHz
Power Down Current	I_{PWDN}	-	10	μA	V_{DD} = 2.7 ~ 5.5V
Input Current P1, P2, P3	I_{IN1}	-50	+10	μA	V_{DD} = 2.7 ~ 5.5V V_{IN} = 0V or V_{DD}
Input Current RST[*1]	I_{IN2}	-10	120	μA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
		-10	50	μA	V_{DD} = 2.7V, 0<V_{IN}<V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	μA	V_{DD} = 2.7 ~ 5.5V 0V<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3	I_{TL}[*4]	-500	-200	μA	V_{DD} = 5.5V V_{IN} = 2.0V
		-150	-50	μA	V_{DD} = 2.7V V_{IN} = 1.0V
Input Low Voltage P0, P1, P2, P3, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
		0	0.5	V	V_{DD} = 2.7V
Input Low Voltage RST[*1]	V_{IL2}	0	0.8	V	V_{DD} = 4.5V
		0	1	V	V_{DD} = 2.7V
Input Low Voltage XTAL1[*3]	V_{IL3}	0	0.8	V	V_{DD} = 4.5V
		0	0.4	V	V_{DD} = 2.7V

MOVX CHARACTERISTICS USING STRECH MEMORY CYCLES

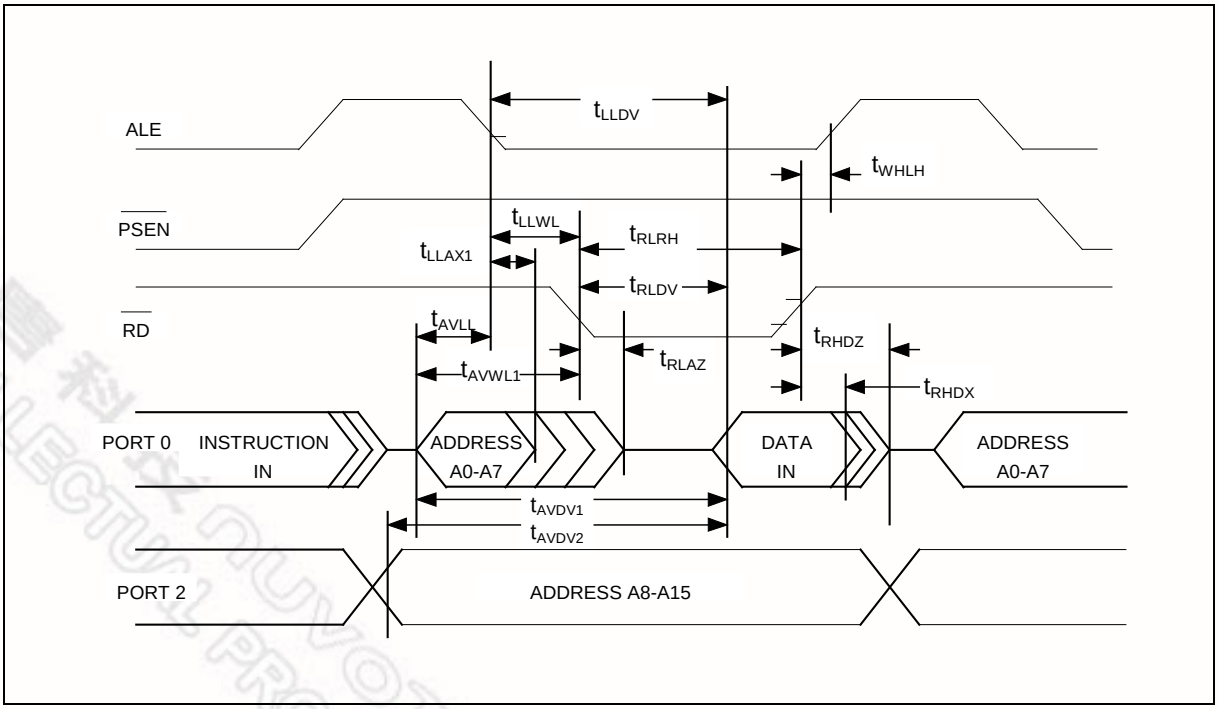
PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS	STRECH
Data Access ALE Pulse Width	t_{LLHL2}	$1.5t_{CLCL} - 5$ $2.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
Address Hold After ALE Low for MOVX write	t_{LLAX2}	$0.5t_{CLCL} - 5$		nS	
$\overline{RD}$ Pulse Width	t_{RLRH}	$2.0t_{CLCL} - 5$ $t_{MCS} - 10$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
$\overline{WR}$ Pulse Width	t_{WLWH}	$2.0t_{CLCL} - 5$ $t_{MCS} - 10$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2.0t_{CLCL} - 20$ $t_{MCS} - 20$	nS	$t_{MCS} = 0$ $t_{MCS}>0$
Data Hold after Read	t_{RHDX}	0		nS	
Data Float after Read	t_{RHDZ}		$t_{CLCL} - 5$ $2.0t_{CLCL} - 5$	nS	$t_{MCS} = 0$ $t_{MCS}>0$
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL} - 5$ $t_{MCS} + 2t_{CLCL} - 40$	nS	$t_{MCS} = 0$ $t_{MCS}>0$
Port 0 Address to Valid Data In	t_{AVDV1}		$3.0t_{CLCL} - 20$ $2.0t_{CLCL} - 5$	nS	$t_{MCS} = 0$ $t_{MCS}>0$
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL} - 5$ $1.5t_{CLCL} - 5$	$0.5t_{CLCL} + 5$ $1.5t_{CLCL} + 5$	nS	$t_{MCS} = 0$ $t_{MCS}>0$
Port 0 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL}	$t_{CLCL} - 5$ $2.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL} - 5$ $2.5t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
Data Valid to WR Transition	t_{QVWX}	-5 $1.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
Data Hold after Write	t_{WHQX}	$t_{CLCL} - 5$ $2.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
$\overline{RD}$ Low to Address Float	t_{RLAZ}		$0.5t_{CLCL} - 5$	nS	
$\overline{RD}$ or WR high to ALE high	t_{WHLH}	0 $1.0t_{CLCL} - 5$	10 $1.0t_{CLCL} + 5$	nS	$t_{MCS} = 0$ $t_{MCS}>0$

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the time period of t_{MCS} for each selection of the Stretch value.

PROGRAM MEMORY READ CYCLE



DATA MEMORY READ CYCLE



```
;*******************************************************************************
;* RE-PROGRAMMING 64KB APFLASH BANK
;*******************************************************************************
PROGRAM_64KROM:
        MOV  R2, #00H           ; TARGET LOW BYTE ADDRESS
        MOV  R1, #00H           ; TARGET HIGH BYTE ADDRESS
        MOV  DPTR, #0H
        MOV  SFRAH, R1          ; SFRAH, TARGET  HIGH ADDRESS
        MOV  SFRCN, #21H        ; SFRCN = 21H, PROGRAM 64K APFLASH
        MOV  R6, #9CH           ; SET TIMER FOR PROGRAMMING, ABOUT 50 μS.
        MOV  R7, #FFH
        MOV  TL0, R6
        MOV  TH0, R7

PROG_D_64K:
        MOV  SFRAL, R2          ; SFRAL = LOW BYTE ADDRESS
        CALL  GET_BYTE_FROM_PC_TO_ACC     ; THIS PROGRAM IS BASED ON USER'S CIRCUIT.
        MOV  @DPTR, A           ; SAVE DATA  INTO SRAM TO VERIFY CODE.
        MOV  SFRFD, A           ; SFRFD = DATA IN
        MOV  TCON, #10H         ; TCON = 10H, TR0 = 1,GO
        MOV  PCON, #01H         ; ENTER IDLE MODE (PRORGAMMING)
        INC  DPTR
        INC  R2
        CJNE  R2, #0H, PROG_D_64K
        INC  R1
        MOV  SFRAH, R1
        CJNE  R1, #0H, PROG_D_64K

;*******************************************************************************
; * VERIFY 64KB APFLASH BANK
;*******************************************************************************
        MOV  R4, #03H           ; ERROR COUNTER
        MOV  R6, #FDH           ; SET TIMER FOR READ VERIFY, ABOUT 1.5 μS.
        MOV  R7, #FFH
        MOV  TL0, R6
        MOV  TH0, R7
        MOV  DPTR, #0H          ; The start address of sample code
        MOV  R2, #0H            ; Target  low byte address
        MOV  R1, 0H             ; Target  high byte address
        MOV  SFRAH, R1          ; SFRAH, Target high address
        MOV  SFRCN, #00H        ; SFRCN = 00H, Read APFLASH
READ_VERIFY_64K:
        MOV  SFRAL, R2          ; SFRAL = LOW ADDRESS
        MOV  TCON, #10H         ; TCON = 10H, TR0 = 1,GO
        MOV  PCON, #01H
        INC  R2
        MOVX  A, @DPTR
        INC  DPTR
        CJNE  A, SFRFD,ERROR_64K
        CJNE  R2, #0H, READ_VERIFY_64K
        INC  R1
        MOV  SFRAH, R1
        CJNE  R1, #0H, READ_VERIFY_64K
```

```
;*******************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*******************************************************************************
        MOV  TA, #AAH
        MOV  TA, #55H
        MOV  CHPCON, #83H       ; SOFTWARE RESET. CPU will restart from APFLASH

ERROR_64K:
        DJNZ  R4,UPDATE_64K     ; IF ERROR OCCURS, REPEAT 3 TIMES.
.                               ; IN-SYST PROGRAMMING FAIL, USER'S PROCESS TO DEAL WITH IT.
                        .
                        .
                        .
```