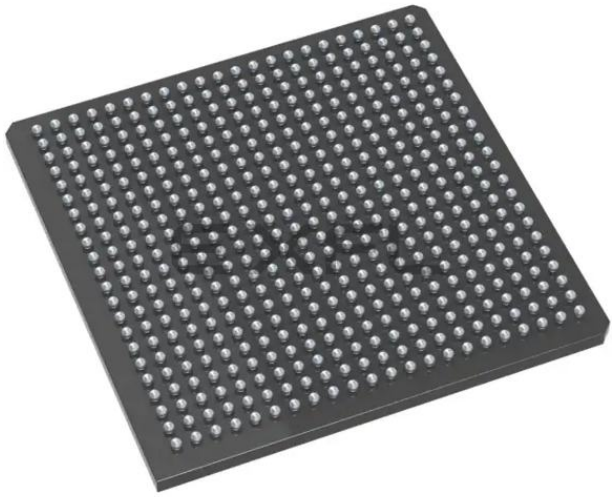


Welcome to E-XFL.COM

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-1fg484m

Table of Contents

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Military)

Sophisticated power-up management circuitry is designed into every SmartFusion cSoC. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-2 on page 2-6.

There are five regions to consider during power-up.

SmartFusion I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCxxxxIOBx are above the minimum specified trip points (Figure 2-2 on page 2-6).
2. VCCxxxxIOBx > VCC – 0.75 V (typical)
3. Chip is in the SoC Mode.

VCCxxxxIOBx Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCxxxxIOBx ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCxxxxIOBx.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

The Microsemi SoC Products Group recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLx exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-2 on page 2-6 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation

Table 2-12 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings* Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

	C_{LOAD} (pF)	VCCFPGAIOBx (V)	Static Power PDC8 (mW)	Dynamic Power PAC10 (µW/MHz)
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	475.66
2.5 V LVCMOS	35	2.5	–	270.50
1.8 V LVCMOS	35	1.8	–	152.17
1.5 V LVCMOS (JESD8-11)	35	1.5	–	104.44
3.3 V PCI	10	3.3	–	202.69
3.3 V PCI-X	10	3.3	–	202.69
Differential				
LVDS	–	2.5	7.75	88.26
LVPECL	–	3.3	19.54	164.99

*Note: *Dynamic power consumption is given for standard load and software default drive strength and output slew.*

Table 2-13 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks

	C_{LOAD} (pF)	VCCMSSIOBx (V)	Static Power PDC8 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	10	3.3	–	19.67
2.5 V LVCMOS	10	2.5	–	11.23
1.8 V LVCMOS	10	1.8	–	5.82
1.5 V LVCMOS (JESD8-11)	10	1.5	–	4.07

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-48 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	2	2	11	9	15	15
4 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	4	4	22	17	15	15
6 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	6	6	44	35	15	15
8 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	8	8	51	45	15	15
12 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	12	12	74	91	15	15
16 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	16	16	74	91	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-49 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
4 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	4	4	22	17	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

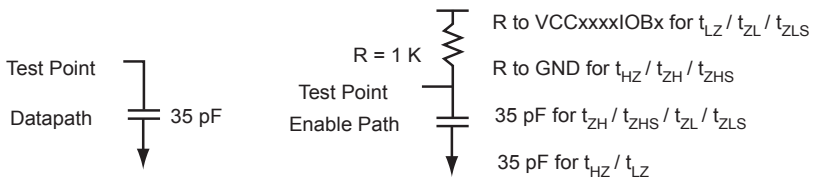


Figure 2-9 • AC Loading

Table 2-50 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	35

*Note: *Measuring point = Vtrip. See Table 2-22 on page 2-25 for a complete table of trip points.*

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by SoC Products Group Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-12. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, SmartFusion cSoCs also support bus LVDS structure and multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

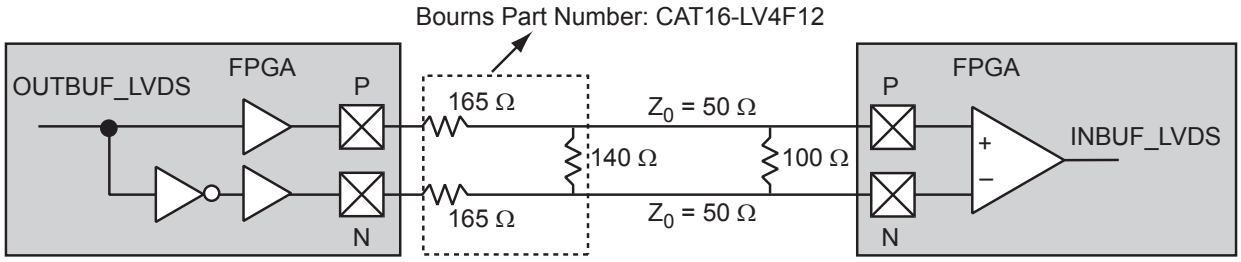


Figure 2-12 • **LVDS Circuit Diagram and Board-Level Implementation**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-14. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

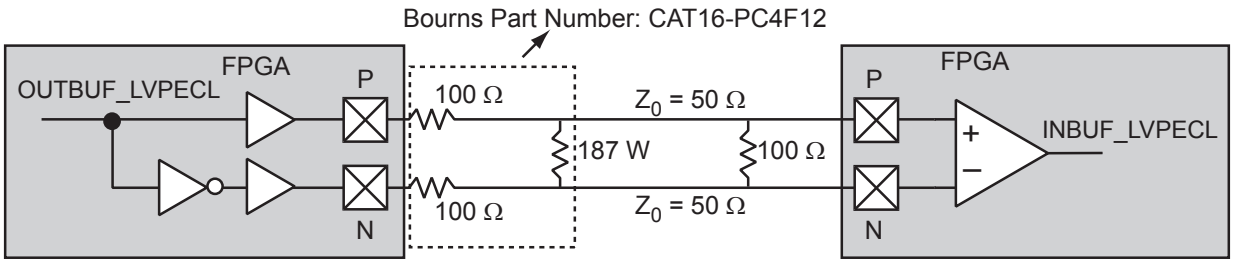


Figure 2-14 • **LVPECL Circuit Diagram and Board-Level Implementation**

Table 2-67 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCFPGAIOBx	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-68 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.64	1.94	Cross point	–

*Note: *Measuring point = Vtrip. See Table 2-22 on page 2-25 for a complete table of trip points.*

Timing Characteristics

Table 2-69 • **LVPECL**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCFPGAIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.62	1.88	0.04	1.38	ns
–1	0.52	1.57	0.03	1.15	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Output Register

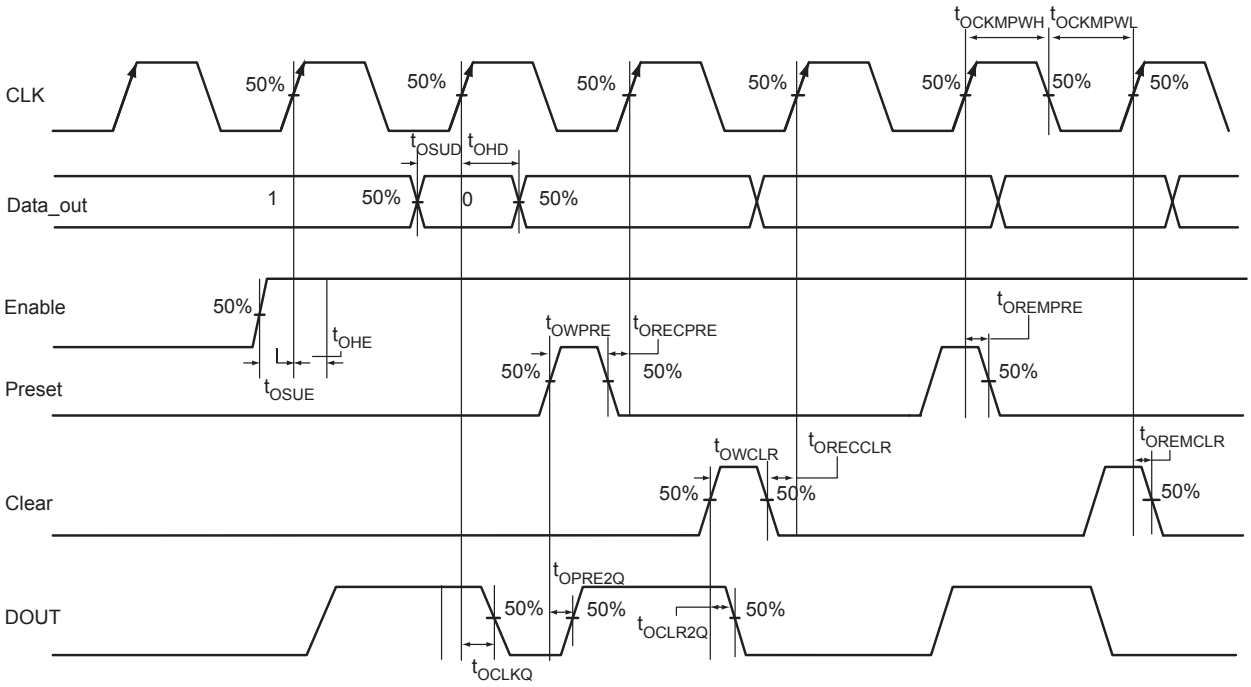


Figure 2-18 • **Output Register Timing Diagram**

Timing Characteristics

Table 2-73 • **Output Data Register Propagation Delays**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.62	0.75	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.33	0.40	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.46	0.56	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.85	1.02	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.85	1.02	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	0.28	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	0.28	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.26	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.26	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.42	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.38	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Output Enable Register

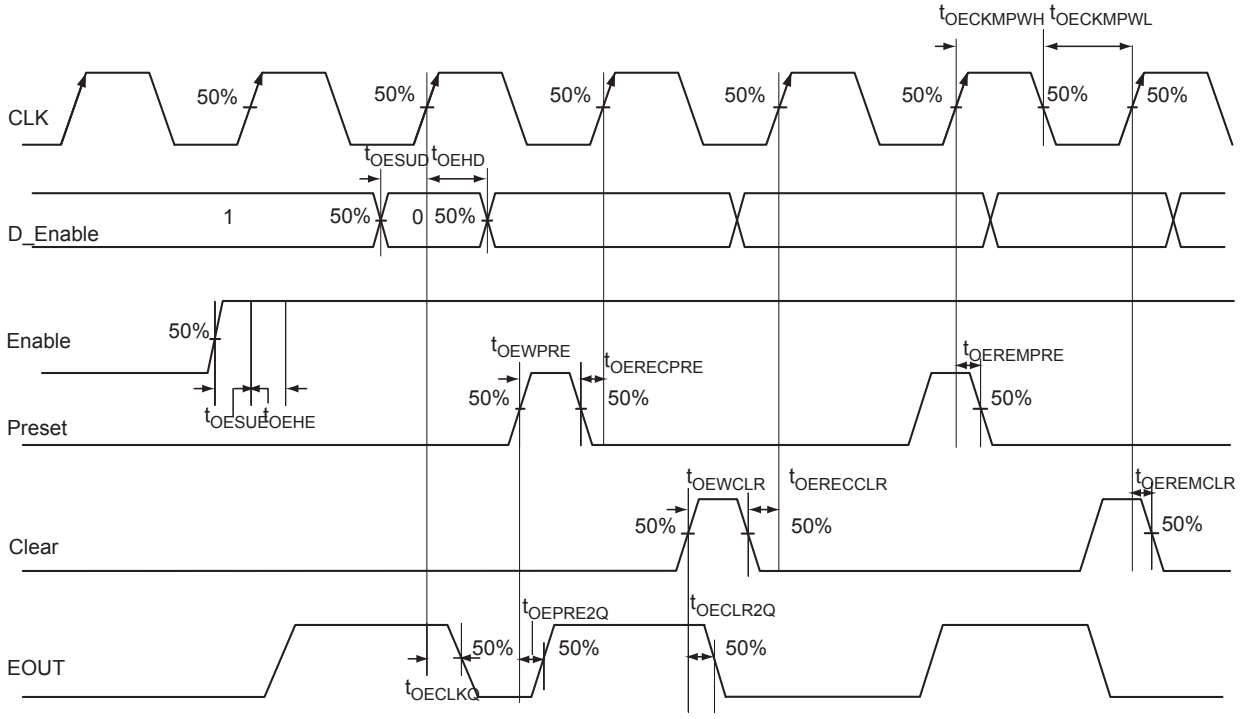


Figure 2-19 • **Output Enable Register Timing Diagram**

Timing Characteristics

Table 2-74 • **Output Enable Register Propagation Delays**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.47	0.56	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.33	0.40	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.46	0.55	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.70	0.84	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.70	0.84	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	0.28	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	0.28	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.26	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.26	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.42	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.38	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The SmartFusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

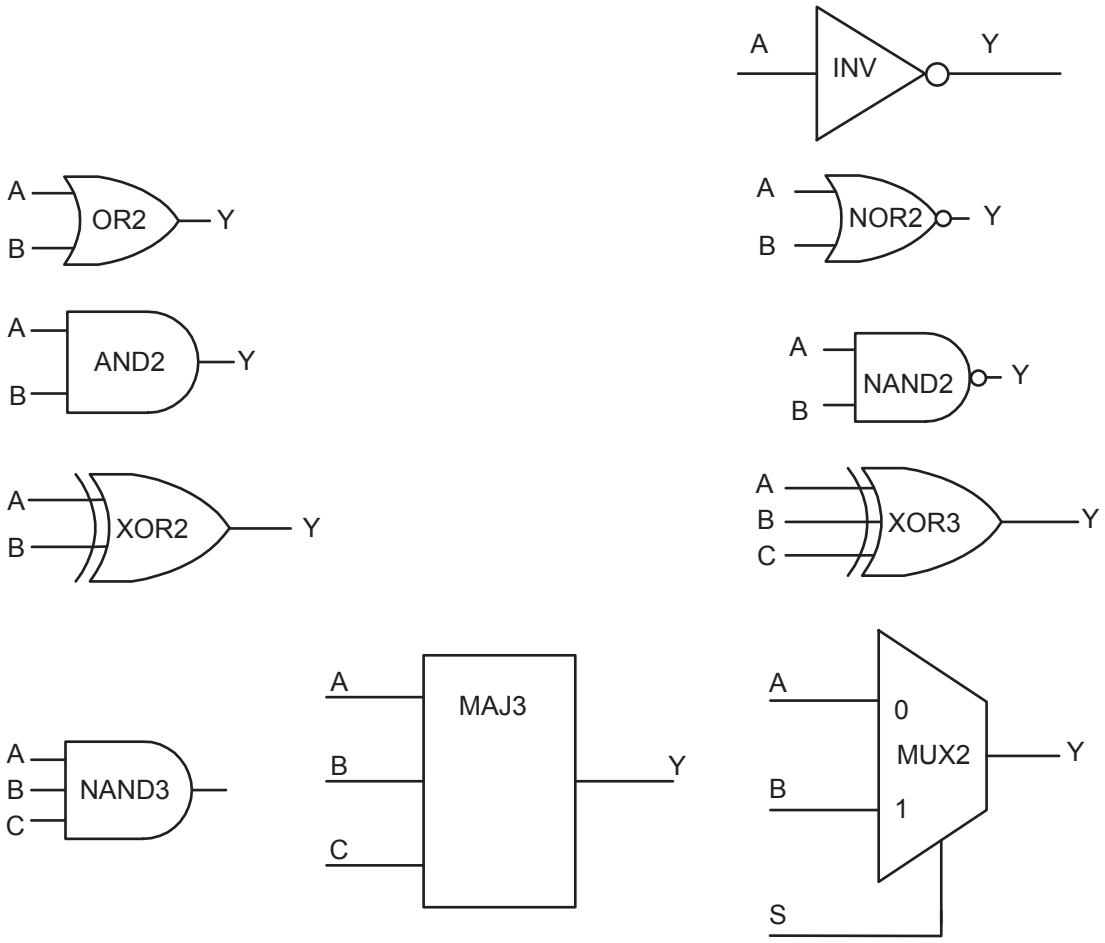


Figure 2-24 • **Sample of Combinatorial Cells**

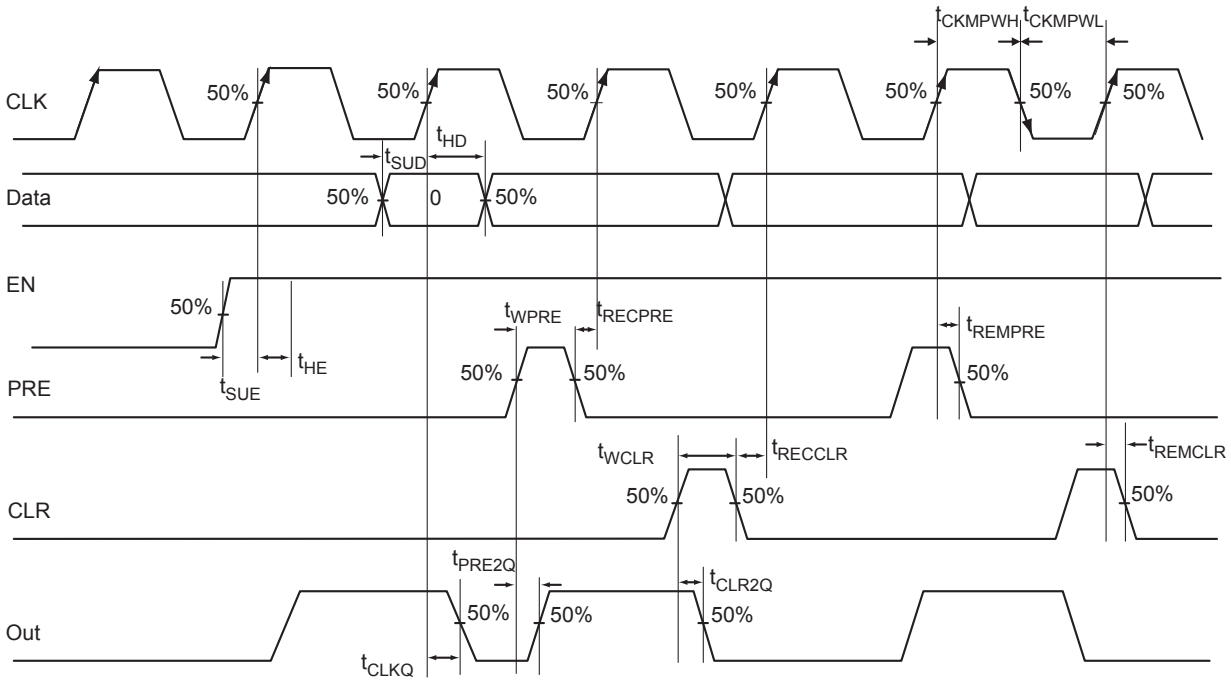


Figure 2-27 • **Timing Model and Waveforms**

Timing Characteristics

Table 2-80 • **Register Delays**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.58	0.70	ns
t_{SUD}	Data Setup Time for the Core Register	0.45	0.54	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.48	0.58	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.42	0.51	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.42	0.51	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	0.28	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	0.28	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	0.26	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	0.26	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.32	0.38	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.36	0.42	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

RC Oscillator

The table below describes the electrical characteristics of the RC oscillator.

RC Oscillator Characteristics

Table 2-83 • **Electrical Characteristics of the RC Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
FRC	Operating frequency			100		MHz
	Accuracy	Temperature: –40°C to 100°C Voltage: 3.3 V ± 5%		1		%
		Temperature: –55°C to 125°C Voltage: 3.3 V ± 5%	–3		3	%
	Output jitter	Period jitter (at 5 K cycles)		100		ps RMS
		Cycle-to-cycle jitter (at 5 K cycles)		100		ps RMS
		Period jitter (at 5 K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps RMS
		Cycle-to-cycle jitter (at 5 K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps RMS
	Output duty cycle			50		%
IDYNRC	Operating current	3.3 V domain		1		mA
		1.5 V domain		2		mA

Main and Lower Power Crystal Oscillator

The tables below describes the electrical characteristics of the main and low power crystal oscillator.

Table 2-84 • **Electrical Characteristics of the Main Crystal Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
	Operating frequency	Using external crystal	0.032		20	MHz
		Using ceramic resonator	0.5		8	MHz
		Using RC Network	0.032		4	MHz
	Output duty cycle			50		%
	Output jitter	With 10 MHz crystal		1		ns RMS
IDYNXTAL	Operating current	RC		0.6		mA
		0.032–0.2		0.6		mA
		0.2–2.0		0.6		mA
		2.0–20.0		0.6		mA
ISTBXTAL	Standby current of crystal oscillator			10		µA
PSRRXTAL	Power supply noise tolerance			0.5		Vp-p
VIHXTAL	Input logic level High		90% of VCC			V
VILXTAL	Input logic level Low				10% of VCC	V
	Startup time	RC [tested at 3.24 MHz]		300	550	ns
		0.032–0.2 [tested at 32 KHz]		500	3,000	ms
		0.2–2.0 [tested at 2 MHz]		8	15	ms
		2.0–20.0 [tested at 20 MHz]		160	180	ns

Table 2-85 • **Electrical Characteristics of the Low Power Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
	Operating frequency			32		KHz
	Output duty cycle			50		%
	Output jitter			30		ns RMS
IDYNXTAL	Operating current	32 KHz		10		µA
ISTBXTAL	Standby current of crystal oscillator			2		µA
PSRRXTAL	Power supply noise tolerance			0.5		Vp-p
VIHXTAL	Input logic level High		90% of VCC			V
VILXTAL	Input logic level Low				10% of VCC	V
	Startup time	Test load used: 20 pF		2.5		s
		Test load used: 30 pF		3.7	13	s

Table 2-95 • ADC Specifications (continued)

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input leakage current	–40°C to +100°C		1		µA
Power supply rejection ratio	DC	44	53		dB
ADC power supply operational current requirements	VCC33ADCx			2.5	mA
	VCC15A			2	mA

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

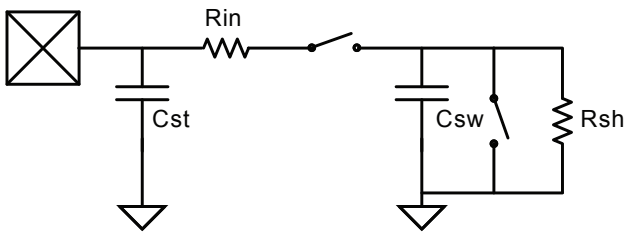


Figure 2-43 • ADC Input Model

Table 2-96 • VAREF Stabilization Time

VAREF Capacitor Value (µF)	Required Settling Time for 8-Bit and 10-Bit Mode (ms)	Required Settling Time for 12-Bit Mode (ms)
0.01	1	1
0.1	3	4
0.2	6	8
0.3	10	11
0.5	17	20
0.7	18	21
1	32	37
2.2	62	73
3.3	99	117
10	275	325
22	635	751
47	1318	1557

Comparator

Unless otherwise specified, performance is specified at 25°C with nominal power supply voltages.

Table 2-98 • **Comparator Performance Specifications**

Specification	Test Conditions		Min.	Typ.	Max.	Units
Input voltage range	Minimum			0		V
	Maximum			2.56		V
Input offset voltage	HYS[1:0] = 00 (no hysteresis)			±1	±3	mV
Input bias current	Comparator 1, 3, 5, 7, 9 (measured at 2.56 V)			40	60	nA
	Comparator 0, 2, 4, 6, 8 (measured at 2.56 V)			150	300	nA
Input resistance			10			MΩ
Power supply rejection ratio	DC (0 – 10 KHz)		50	60		dB
Propagation delay	100 mV overdrive					
	HYS[1:0] = 00					
	(no hysteresis)			15	18	ns
	100 mV overdrive					
	HYS[1:0] = 10					
	(with hysteresis)			25	30	ns
Hysteresis (± refers to rising and falling threshold shifts, respectively)	HYS[1:0] = 00	Typical (25°C)	0	0	±5	mV
		Across all corners (–55ºC to +125ºC)	0		±5	mV
	HYS[1:0] = 01	Typical (25°C)	±3	± 16	±30	mV
		Across all corners (–55ºC to +125ºC)	0		±36	mV
	HYS[1:0] = 10	Typical (25°C)	±19	± 31	±48	mV
		Across all corners (–40ºC to +100ºC)	±12		±54	mV
		Across all corners (–55ºC to +125ºC)	±5		±54	mV
	HYS[1:0] = 11	Typical (25°C)	±80	± 105	±190	mV
		Across all corners (–40ºC to +100ºC)	±80		±194	mV
		Across all corners (–55ºC to +125ºC)	±60		±194	mV
Comparator current requirements (per comparator)	VCC33A = 3.3 V (operational mode); COMP_EN = 1					
	VCC33A			150	165	µA
	VCC33AP			140	165	µA
	VCC15A			1	15	µA

Emcraft Systems provides porting of the open-source U-boot firmware and uClinux™ kernel to the SmartFusion cSoC, a Linux®-based cross-development framework, and other complementary components. Combined with the release of its A2F-Linux Evaluation Kit, this provides a low-cost platform for evaluation and development of Linux (uClinux) on the Cortex-M3 CPU core of the Microsemi SmartFusion cSoC.

- Emcraft Linux on Microsemi's SmartFusion cSoC

Keil offers the RTX Real-Time Kernel as a royalty-free, deterministic RTOS designed for ARM and Cortex-M devices. It allows you to create programs that simultaneously perform multiple functions and helps to create applications which are better structured and more easily maintained.

- The RTX Real-Time Kernel is included with MDK-ARM. Download the Evaluation version of Keil MDK-ARM.
- RTX source code is available as part of Keil/ARM Real-Time Library (RL-ARM), a group of tightly-coupled libraries designed to solve the real-time and communication challenges of embedded systems based on ARM-powered microcontroller devices. The RL-ARM library now supports SmartFusion cSoCs and designers with additional key features listed in the "Middleware" section on page 3-5.

Micrium supports SmartFusion cSoCs with the company's flagship µC/OS family, recognized for a variety of features and benefits, including unparalleled reliability, performance, dependability, impeccable source code and vast documentation. Micrium supports the following products for SmartFusion cSoCs and continues to work with Microsemi on additional projects.

- SmartFusion Quickstart Guide for Micrium µC/OS-III Examples
  - Design Files

µC/OS-III™, Micrium's newest RTOS, is designed to save time on your next embedded project and puts greater control of the software in your hands.

RoweBots provides an ultra tiny Linux-compatible RTOS called Unison for SmartFusion. Unison consists of a set of modular software components, which, like Linux, are either free or commercially licensed. Unison offers POSIX® and Linux compatibility with hard real-time performance, complete I/O modules and an easily understood environment for device driver programming. Seamless integration with FPGA and analog features are fast and easy.

- Unison V4-based products include a free Unison V4 Linux and POSIX-compatible kernel with serial I/O, file system, six demonstration programs, upgraded documentation and source code for Unison V4, and free (for non-commercial use) Unison V4 TCP/IP server. Commercial license upgrade is available for Unison V4 TCP/IP server with three demonstration programs, DHCP client and source code.
- Unison V5-based products include commercial Unison V5 Linux- and POSIX-compatible kernel with serial I/O, file system, extensive feature set, full documentation, source code and more than 20 demonstration programs, Unison V5 TCP/IPv4 with extended feature set, sockets interface, multiple network interfaces, PPP support, DHCP client, documentation, source code and six demonstration programs, and multiple other features.

Middleware

Microsemi has ported both uIP and lwIP for Ethernet support as well as including TFTP file service.

- SmartFusion Webserver Demo Using uIP and FreeRTOS
- SmartFusion: Running Webserver, TFTP on lwIP TCP/IP Stack Application Note

The Keil/ARM Real-Time Library (RL-ARM)[1], in addition to RTX source, includes the following:

- RL-TCPnet (TCP/IP) – The Keil RL-TCPnet library, supporting full TCP/IP and UDP protocols, is a full networking suite specifically written for small ARM and Cortex-M processor-based microcontrollers. TCPnet is now ported to and supports SmartFusion Cortex-M3. It is highly optimized, has a small code footprint, and gives excellent performance, providing a wide range of application level protocols and examples such as FTP, SNMP, SOAP and AJAX. An HTTP server example of TCPnet working in a SmartFusion design is available.

1. The CAN and USB functions within RL-ARM are not supported for SmartFusion cSoC.

- Flash File System (RL-Flash) allows your embedded applications to create, save, read, and modify files in standard storage devices such as ROM, RAM, or FlashROM, using a standard serial peripheral interface (SPI). Many ARM-based microcontrollers have a practical requirement for a standard file system. With RL-FlashFS you can implement new features in embedded applications such as data logging, storing program state during standby modes, or storing firmware upgrades.

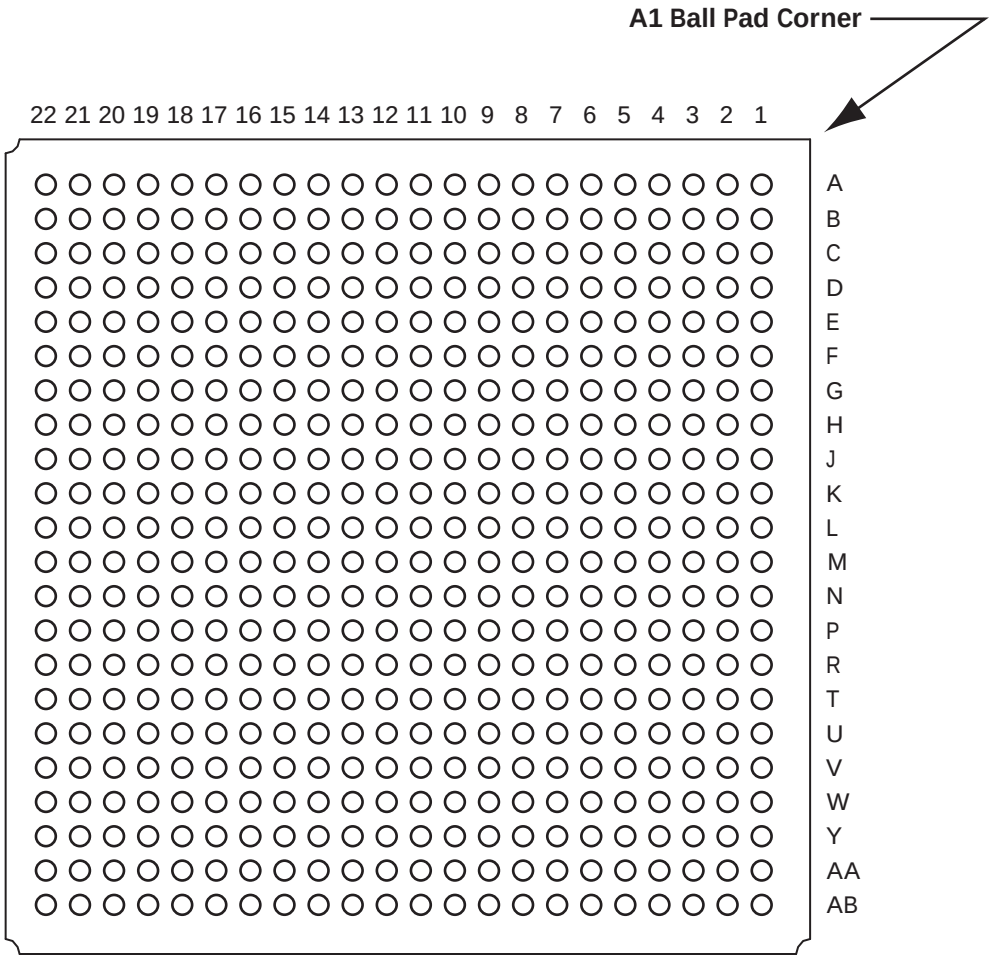
Micrium, in addition to µC/OS-III®, offers the following support for SmartFusion cSoC:

- µC/TCP-IP™ is a compact, reliable, and high-performance stack built from the ground up by Micrium and has the quality, scalability, and reliability that translates into a rapid configuration of network options, remarkable ease-of-use, and rapid time-to-market.
- µC/Probe™ is one of the most useful tools in embedded systems design and puts you in the driver's seat, allowing you to take charge of virtually any variable, memory location, and I/O port in your embedded product, while your system is running.

Name	Type	Polarity/Bus Size	Description
PCAP		1	Positive Capacitor connection. This is the positive terminal of the charge pump. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP. If this pin is not used, it must be left unconnected/floating. In this case, no capacitor is needed. Analog charge pump capacitors are not needed if none of the analog SCB features are used, and none of the SDDs are used.
PTBASE		1	Pass transistor base connection This is the control signal of the voltage regulator. This pin should be connected to the base of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.
PTEM		1	Pass transistor emitter connection. This is the feedback input of the voltage regulator. This pin should be connected to the emitter of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.
MSS_RESET_N		Low	Low Reset signal which can be used as an external reset and can also be used as a system level reset under control of the Cortex-M3 processor. MSS_RESET_N is an output asserted low after power-on reset. The direction of MSS_RESET_N changes during the execution of the Microsemi System Boot when chip-level reset is enabled. The Microsemi System Boot reconfigures MSS_RESET_N to become a reset input signal when chip-level reset is enabled. It has an internal pull-up so it can be left floating. In the current software, the MSS_RESET_N is modeled as an external input signal only.
PU_N	In	Low	Push-button is the connection for the external momentary switch used to turn on the 1.5 V voltage regulator and can be floating if not used.

Name	Type	Polarity/ Bus Size	Description
SPI_1_DO	Out	1	Data output. Second SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
SPI_1_SS	Out	1	Slave select (chip select). Second SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
Universal Asynchronous Receiver/Transmitter (UART) Peripherals			
UART_0_RXD	In	1	Receive data. First UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
UART_0_TXD	Out	1	Transmit data. First UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
UART_1_RXD	In	1	Receive data. Second UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
UART_1_TXD	Out	1	Transmit data. Second UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
Ethernet MAC			
MAC_CLK	In	Rise	Receive clock. 50 MHz ± 50 ppm clock source received from RMII PHY. Can be left floating when unused.
MAC_CRSDV	In	High	Carrier sense/receive data valid for RMII PHY Can also be used as an FPGA User IO (see "IO" on page 5-5).
MAC_MDC	Out	Rise	RMII management clock Can also be used as an FPGA User IO (see "IO" on page 5-5).
MAC_MDIO	In/Out	1	RMII management data input/output Can also be used as an FPGA User IO (see "IO" on page 5-5).
MAC_RXDx	In	2	Ethernet MAC receive data. Data recovered and decoded by PHY. The RXD[0] signal is the least significant bit. Can also be used as an FPGA User I/O (see "IO" on page 5-5).
MAC_RXER	In	HIGH	Ethernet MAC receive error. If MACRX_ER is asserted during reception, the frame is received and status of the frame is updated with MACRX_ER. Can also be used as an FPGA user I/O (see "IO" on page 5-5).
MAC_TXDx	Out	2	Ethernet MAC transmit data. The TXD[0] signal is the least significant bit. Can also be used as an FPGA user I/O (see "IO" on page 5-5).
MAC_TXEN	Out	HIGH	Ethernet MAC transmit enable. When asserted, indicates valid data for the PHY on the TXD port. Can also be used as an FPGA User I/O (see "IO" on page 5-5).

FG484



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

FG484	
Pin Number	A2F500 Function
J3	EMC_DB[4]/GEA0/IO78NDB5V0
J4	EMC_DB[3]/GEC2/IO77PPB5V0
J5	VCCFPGAIOB5
J6	GFA0/IO81NDB5V0
J7	VCCFPGAIOB5
J8	GND
J9	VCC
J10	GND
J11	VCC
J12	GND
J13	VCC
J14	GND
J15	VCC
J16	GND
J17	IO37PDB1V0
J18	VCCFPGAIOB1
J19	GCA0/IO36NDB1V0
J20	GCA1/IO36PDB1V0
J21	GCC1/IO35PPB1V0
J22	GCB1/IO34PDB1V0
K1	GND
K2	EMC_DB[0]/GEA2/IO76NDB5V0
K3	EMC_DB[1]/GEB2/IO76PDB5V0
K4	IO74PPB5V0
K5	EMC_DB[2]/IO77NPB5V0
K6	IO75PDB5V0
K7	GND
K8	VCC
K9	GND
K10	VCC
K11	GND
K12	VCC
K13	GND
K14	VCC
K15	GND
K16	VCCFPGAIOB1
K17	IO37NDB1V0

FG484	
Pin Number	A2F500 Function
K18	GDA1/IO40PDB1V0
K19	GDA0/IO40NDB1V0
K20	GDC1/IO38PDB1V0
K21	GDC0/IO38NDB1V0
K22	GND
L1	IO73PDB5V0
L2	IO73NDB5V0
L3	IO72PPB5V0
L4	GND
L5	IO74NPB5V0
L6	IO75NDB5V0
L7	VCCFPGAIOB5
L8	GND
L9	VCC
L10	GND
L11	VCC
L12	GND
L13	VCC
L14	GND
L15	VCC
L16	GND
L17	GNDQ
L18	GDA2/IO42NDB1V0
L19	VCCFPGAIOB1
L20	GDB1/IO39PDB1V0
L21	GDB0/IO39NDB1V0
L22	GDC2/IO41PDB1V0
M1	IO71PDB5V0
M2	IO71NDB5V0
M3	VCCFPGAIOB5
M4	IO72NPB5V0
M5	GNDQ
M6	IO68PDB5V0
M7	GND
M8	VCC
M9	GND
M10	VCC