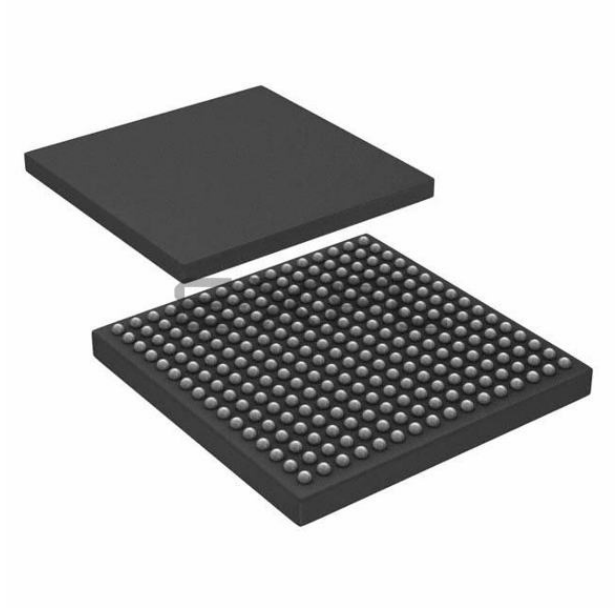

Welcome to E-XFL.COM

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	100MHz
Primary Attributes	ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-1fgg256m

detection devices from the PCB design. Flash-based SmartFusion cSoCs simplify total system design and reduce cost and design risk, while increasing system reliability.

Immunity to Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O configuration behavior in an unpredictable way.

Another source of radiation-induced firm errors is alpha particles. For alpha radiation to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in SmartFusion cSoCs. Once it is programmed, the flash cell configuration element of SmartFusion cSoCs cannot be altered by high energy neutrons and is therefore immune to errors from them. Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-1 on page 1-4).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated

Thermal Characteristics

Introduction

The temperature variable in the SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - \theta_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 2-6 • **Package Thermal Resistance**

Product	θ_{JA}			θ_{JC}	θ_{JB}	Units
	Still Air	1.0 m/s	2.5 m/s			
A2F060-FG256	36.9	31.1	29.4	TBD	23.7	°C/W
A2F500-FG256	26.2	20.6	18.9	TBD	13.2	°C/W
A2F500-FG484	21.9	18.6	16.4	7.5	11	°C/W

Detailed I/O DC Characteristics

Table 2-26 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	V_{IN} = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	V_{IN} = 0, f = 1.0 MHz		8	pF

Table 2-27 • **I/O Output Buffer Maximum Resistances[1]**
Applicable to FPGA I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at http://www.microsemi.com/soc/download/ibis/default.aspx (also generated by the SoC Products Group Libero SoC toolset).*
2. *$R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec*
3. *$R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec*

Table 2-30 • I/O Short Currents IOSH/IOSL Applicable to FPGA I/O Banks

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
	16 mA	87	83
	24 mA	124	169
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	51	45
	12 mA	74	91
	16 mA	74	91
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
	6 mA	39	32
	8 mA	55	66
	12 mA	55	66
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

*Note: *T_J = 100°C.*

Table 2-31 • I/O Short Currents IOSH/IOSL Applicable to MSS I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	54	51
2.5 V LVCMOS	8 mA	37	32
1.8 V LVCMOS	4 mA	22	17
1.5 V LVCMOS	2 mA	16	13

*Note: *T_J = 100°C*

Timing Characteristics

Table 2-51 • 1.8 V LVCMOS High Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.62	11.85	0.04	1.22	0.41	9.22	11.85	2.80	1.70	11.42	14.05	ns
	–1	0.52	9.87	0.03	1.02	0.34	7.68	9.87	2.33	1.42	9.52	11.71	ns
4 mA	Std.	0.62	6.91	0.04	1.22	0.41	5.92	6.91	3.26	2.85	8.13	9.12	ns
	–1	0.52	5.76	0.03	1.02	0.34	4.94	5.76	2.72	2.38	6.77	7.60	ns
6 mA	Std.	0.62	4.46	0.04	1.22	0.41	4.27	4.46	3.58	3.40	6.48	6.66	ns
	–1	0.52	3.71	0.03	1.02	0.34	3.56	3.71	2.98	2.84	5.40	5.55	ns
8 mA	Std.	0.62	3.95	0.04	1.22	0.41	4.02	3.93	3.65	3.55	6.23	6.14	ns
	–1	0.52	3.29	0.03	1.02	0.34	3.35	3.28	3.04	2.96	5.19	5.12	ns
12 mA	Std.	0.62	3.62	0.04	1.22	0.41	3.68	3.06	3.75	4.09	5.89	5.26	ns
	–1	0.52	3.01	0.03	1.02	0.34	3.07	2.55	3.12	3.41	4.91	4.39	ns
16 mA	Std.	0.62	3.62	0.04	1.22	0.41	3.68	3.06	3.75	4.09	5.89	5.26	ns
	–1	0.52	3.01	0.03	1.02	0.34	3.07	2.55	3.12	3.41	4.91	4.39	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-52 • 1.8 V LVCMOS Low Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.62	15.25	0.04	1.22	0.41	14.43	15.25	2.80	1.65	16.63	17.46	ns
	–1	0.52	12.71	0.03	1.02	0.34	12.02	12.71	2.34	1.37	13.86	14.55	ns
4 mA	Std.	0.62	10.43	0.04	1.22	0.41	10.62	10.31	3.27	2.75	12.82	12.51	ns
	–1	0.52	8.69	0.03	1.02	0.34	8.85	8.59	2.72	2.29	10.69	10.42	ns
6 mA	Std.	0.62	8.21	0.04	1.22	0.41	8.36	7.75	3.58	3.30	10.57	9.96	ns
	–1	0.52	6.84	0.03	1.02	0.34	6.97	6.46	2.98	2.75	8.81	8.30	ns
8 mA	Std.	0.62	7.66	0.04	1.22	0.41	7.80	7.22	3.65	3.44	10.01	9.43	ns
	–1	0.52	6.38	0.03	1.02	0.34	6.50	6.02	3.04	2.87	8.34	7.86	ns
12 mA	Std.	0.62	7.24	0.04	1.22	0.41	7.38	7.23	3.75	3.96	9.58	9.43	ns
	–1	0.52	6.04	0.03	1.02	0.34	6.15	6.02	3.13	3.30	7.98	7.86	ns
16 mA	Std.	0.62	7.24	0.04	1.22	0.41	7.38	7.23	3.75	3.96	9.58	9.43	ns
	–1	0.52	6.04	0.03	1.02	0.34	6.15	6.02	3.13	3.30	7.98	7.86	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

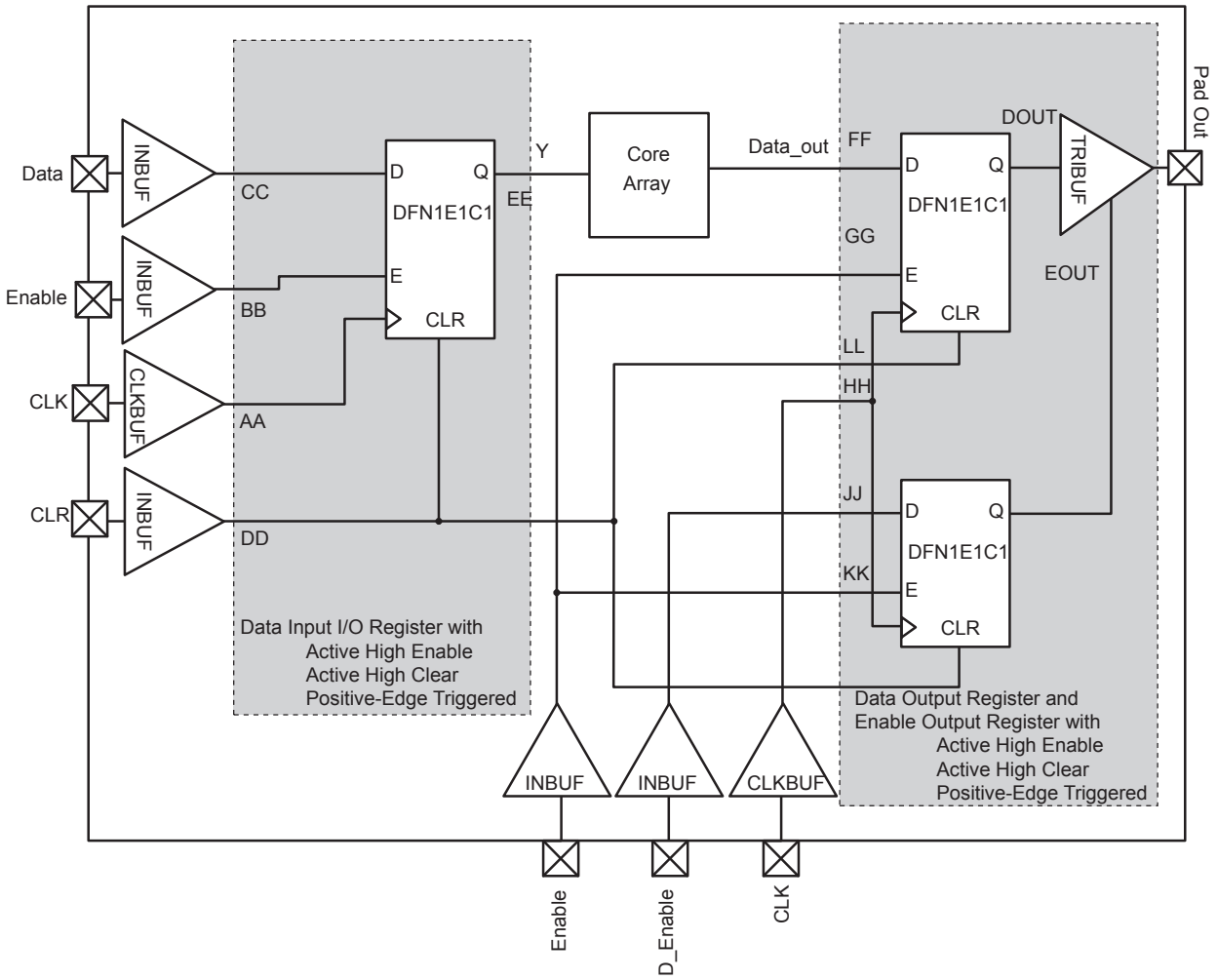

***Figure 2-16* • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Analog Sigma-Delta Digital to Analog Converter (DAC)

Unless otherwise noted, sigma-delta DAC performance is specified at 25°C with nominal power supply voltages, using the internal sigma-delta modulators with 16-bit inputs, HCLK = 100 MHz, modulator inputs updated at a 100 KHz rate, in voltage output mode with an external 160 pF capacitor to ground, after trimming and digital [pre-]compensation.

Table 2-99 • **Analog Sigma-Delta DAC**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Resolution		8		24	Bits
Output range			0 to 2.56		V
	Current output mode		0 to 256		µA
Output Impedance		6	10	12	KΩ
	Current output mode	10			MΩ
Output voltage compliance	Current output mode		0–3.0		V
	–40ºC to +100ºC	0–2.7		0–3.4	V
Gain error	Voltage output mode		0.3	±2	%
	–40ºC to +100ºC		0.3	±2	%
	–55ºC to +125ºC		0.3	±6	%
	Current output mode		0.3	±2	%
	–40ºC to +100ºC		0.3	±2	%
	–55ºC to +125ºC		0.3	±6	%
Output referred offset	DACBYTE0 = h'00 (8-bit)		0.25	±1	mV
	–40ºC to +100ºC		1	±2.5	mV
	Current output mode		0.3	±1	µA
	–40ºC to +100ºC		1	±2.5	µA
Integral non-linearity	RMS deviation from BFSL		0.1	0.4	% FS*
Differential non-linearity			0.05	0.4	% FS*
Analog settling time			Refer to Figure 2-44 on page 2-87		µs
Power supply rejection ratio	DC, full scale output	33	34		dB

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

Table 2-99 • Analog Sigma-Delta DAC (continued)

Specification	Test Conditions	Min.	Typ.	Max.	Units
Sigma-delta DAC power supply current requirements (not including VAREFx)	Input = 0, EN = 1 (operational mode)				
	VCC33SDDx		30	40	µA
	VCC15A		3	5	µA
	Input = Half scale, EN = 1 (operational mode)				
	VCC33SDDx		160	165	µA
	VCC15A		33	35	µA
	Input = Full scale, EN = 1 (operational mode)				
	VCC33SDDx		280	285	µA
	VCC15A		70	75	µA

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

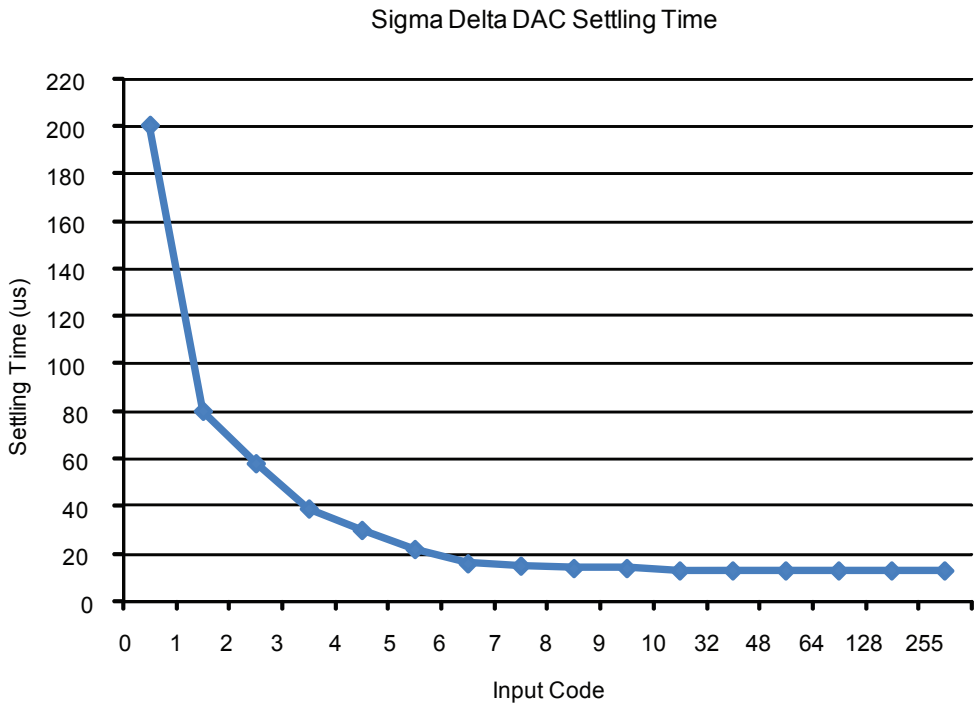

Figure 2-44 • Sigma-Delta DAC Setting Time

Voltage Regulator

***Table 2-100* • Voltage Regulator**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
VOUT	Output voltage	T_J = 25°C		1.425	1.5	1.575	V
VOS	Output offset voltage	T_J = 25°C			11		mV
ICC33A	Operation current	T_J = 25°C	I_{LOAD} = 1 mA		3.4		mA
			I_{LOAD} = 100 mA		11		mA
			I_{LOAD} = 0.5 A		21		mA
ΔVOUT	Load regulation	T_J = 25°C	I_{LOAD} = 1 mA to 0.5 A		5.8		mV
ΔVOUT	Line regulation	T_J = 25°C	VCC33A = 2.97 V to 3.63 V I_{LOAD} = 1 mA		8		mV/V
			VCC33A = 2.97 V to 3.63 V I_{LOAD}= 100 mA		8		mV/V
			VCC33A = 2.97 V to 3.63 V I_{LOAD} = 500 mA		8		mV/V
	Dropout voltage[1]	T_J = 25°C	I_{LOAD} = 1 mA		0.65		V
			I_{LOAD} = 100 mA		0.84		V
			I_{LOAD} = 0.5 A		1.35		V
IPTBASE	PTBase current	T_J = 25°C	I_{LOAD} = 1 mA		48		µA
			I_{LOAD} = 100 mA		736		µA
			I_{LOAD} = 0.5 A		12		mA
	Startup time[2]	T_J = 25°C			200		ms

Notes:

1. *Dropout voltage is defined as the minimum VCC33A voltage. The parameter is specified with respect to the output voltage. The specification represents the minimum input-to-output differential voltage required to maintain regulation.*
2. *Assumes 10 µF.*

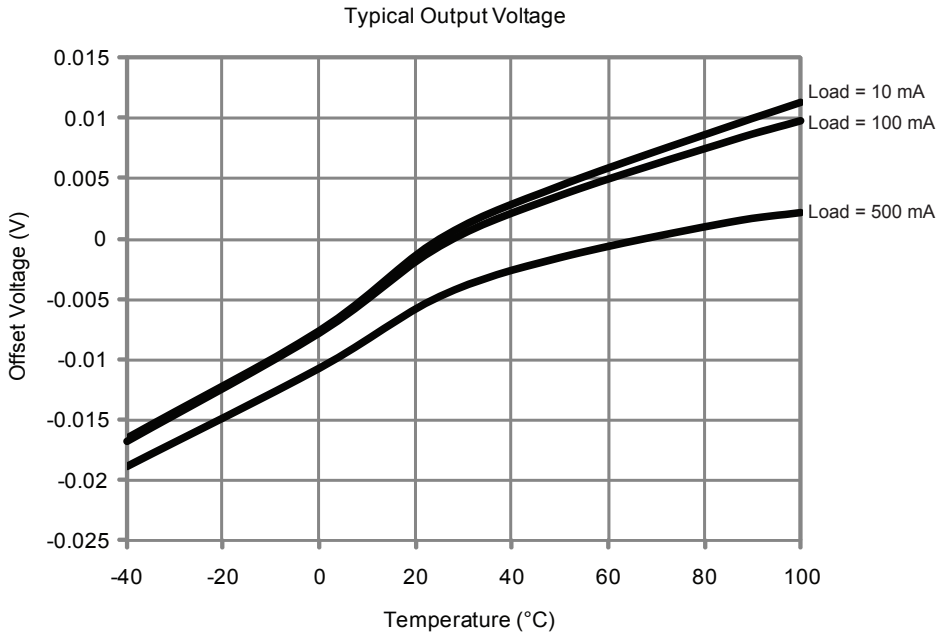

Figure 2-45 • **Typical Output Voltage**

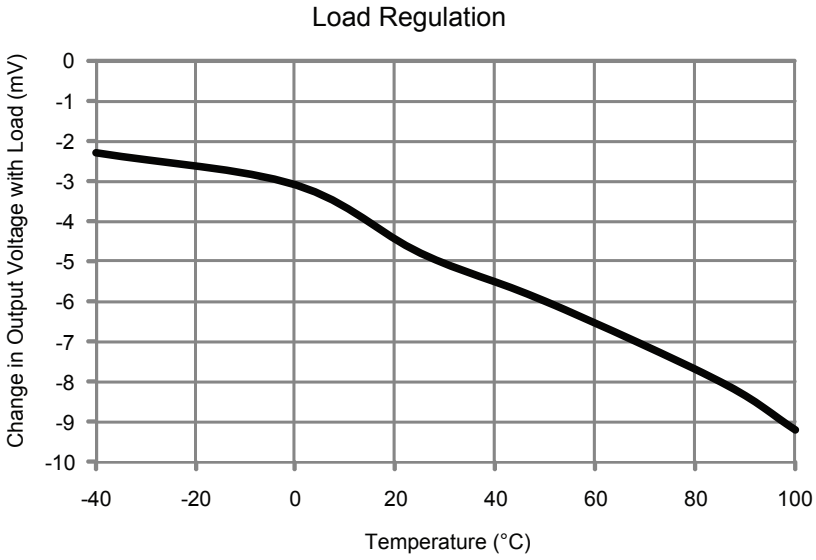

Figure 2-46 • **Load Regulation**

Emcraft Systems provides porting of the open-source U-boot firmware and uClinux™ kernel to the SmartFusion cSoC, a Linux®-based cross-development framework, and other complementary components. Combined with the release of its A2F-Linux Evaluation Kit, this provides a low-cost platform for evaluation and development of Linux (uClinux) on the Cortex-M3 CPU core of the Microsemi SmartFusion cSoC.

- Emcraft Linux on Microsemi's SmartFusion cSoC

Keil offers the RTX Real-Time Kernel as a royalty-free, deterministic RTOS designed for ARM and Cortex-M devices. It allows you to create programs that simultaneously perform multiple functions and helps to create applications which are better structured and more easily maintained.

- The RTX Real-Time Kernel is included with MDK-ARM. Download the Evaluation version of Keil MDK-ARM.
- RTX source code is available as part of Keil/ARM Real-Time Library (RL-ARM), a group of tightly-coupled libraries designed to solve the real-time and communication challenges of embedded systems based on ARM-powered microcontroller devices. The RL-ARM library now supports SmartFusion cSoCs and designers with additional key features listed in the "Middleware" section on page 3-5.

Micrium supports SmartFusion cSoCs with the company's flagship µC/OS family, recognized for a variety of features and benefits, including unparalleled reliability, performance, dependability, impeccable source code and vast documentation. Micrium supports the following products for SmartFusion cSoCs and continues to work with Microsemi on additional projects.

- SmartFusion Quickstart Guide for Micrium µC/OS-III Examples
  - Design Files

µC/OS-III™, Micrium's newest RTOS, is designed to save time on your next embedded project and puts greater control of the software in your hands.

RoweBots provides an ultra tiny Linux-compatible RTOS called Unison for SmartFusion. Unison consists of a set of modular software components, which, like Linux, are either free or commercially licensed. Unison offers POSIX® and Linux compatibility with hard real-time performance, complete I/O modules and an easily understood environment for device driver programming. Seamless integration with FPGA and analog features are fast and easy.

- Unison V4-based products include a free Unison V4 Linux and POSIX-compatible kernel with serial I/O, file system, six demonstration programs, upgraded documentation and source code for Unison V4, and free (for non-commercial use) Unison V4 TCP/IP server. Commercial license upgrade is available for Unison V4 TCP/IP server with three demonstration programs, DHCP client and source code.
- Unison V5-based products include commercial Unison V5 Linux- and POSIX-compatible kernel with serial I/O, file system, extensive feature set, full documentation, source code and more than 20 demonstration programs, Unison V5 TCP/IPv4 with extended feature set, sockets interface, multiple network interfaces, PPP support, DHCP client, documentation, source code and six demonstration programs, and multiple other features.

Middleware

Microsemi has ported both uIP and lwIP for Ethernet support as well as including TFTP file service.

- SmartFusion Webserver Demo Using uIP and FreeRTOS
- SmartFusion: Running Webserver, TFTP on lwIP TCP/IP Stack Application Note

The Keil/ARM Real-Time Library (RL-ARM)[1], in addition to RTX source, includes the following:

- RL-TCPnet (TCP/IP) – The Keil RL-TCPnet library, supporting full TCP/IP and UDP protocols, is a full networking suite specifically written for small ARM and Cortex-M processor-based microcontrollers. TCPnet is now ported to and supports SmartFusion Cortex-M3. It is highly optimized, has a small code footprint, and gives excellent performance, providing a wide range of application level protocols and examples such as FTP, SNMP, SOAP and AJAX. An HTTP server example of TCPnet working in a SmartFusion design is available.

1. The CAN and USB functions within RL-ARM are not supported for SmartFusion cSoC.

- Flash File System (RL-Flash) allows your embedded applications to create, save, read, and modify files in standard storage devices such as ROM, RAM, or FlashROM, using a standard serial peripheral interface (SPI). Many ARM-based microcontrollers have a practical requirement for a standard file system. With RL-FlashFS you can implement new features in embedded applications such as data logging, storing program state during standby modes, or storing firmware upgrades.

Micrium, in addition to µC/OS-III®, offers the following support for SmartFusion cSoC:

- µC/TCP-IP™ is a compact, reliable, and high-performance stack built from the ground up by Micrium and has the quality, scalability, and reliability that translates into a rapid configuration of network options, remarkable ease-of-use, and rapid time-to-market.
- µC/Probe™ is one of the most useful tools in embedded systems design and puts you in the driver's seat, allowing you to take charge of virtually any variable, memory location, and I/O port in your embedded product, while your system is running.

4 – SmartFusion Programming

SmartFusion cSoCs have three separate flash areas that can be programmed:

1. The FPGA fabric
2. The embedded nonvolatile memories (eNVMs)
3. The embedded flash ROM (eFROM)

There are essentially three methodologies for programming these areas:

1. In-system programming (ISP)
2. In-application programming (IAP)
   – FPGA fabric, eNVM, and eFROM
3. Pre-programming (non-ISP)

Programming, whether ISP or IAP methodologies are employed, can be done in two ways:

1. Securely using the on chip AES decryption logic
2. In plain text

In-System Programming

In-System Programming is performed with the aid of external JTAG programming hardware. Table 4-1 describes the JTAG programming hardware that will program a SmartFusion cSoC and Table 4-2 defines the JTAG pins that provide the interface for the programming hardware.

***Table 4-1* • Supported JTAG Programming Hardware**

Dongle	Source	JTAG	SWD[1]	SWV[2]	Program FPGA	Program eFROM	Program eNVM
FlashPro3/4	SoC Products Group	Yes	No	No	Yes	Yes	Yes
ULINK Pro	Keil	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes
ULINK2	Keil	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes
IAR J-Link	IAR	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes

Notes:

1. *SWD = ARM Serial Wire Debug*
2. *SWV = ARM Serial Wire Viewer*
3. *Planned support*

***Table 4-2* • JTAG Pin Descriptions**

Pin Name	Description
JTAGSEL	ARM Cortex-M3 or FPGA test access port (TAP) controller selection
TRSTB	Test reset bar
TCK	Test clock
TMS	Test mode select
TDI	Test data input
TDO	Test data output

Re-Programming the eNVM Blocks Using the Cortex-M3

In this mode the Cortex-M3 is executing the eNVM programming algorithm from eSRAM. Since individual pages (132 bytes) of the eNVM can be write-protected, the programming algorithm software can be protected from inadvertent erasure. When reprogramming the eNVM, both MSS I/Os and FPGA I/Os are available as interfaces for sourcing the new eNVM image. The SoC Products Group provides working example projects for SoftConsole, IAR, and Keil development environments. These can be downloaded via the SoC Products Group Firmware Catalog.

Alternately, the eNVM can be reprogrammed by the Cortex-M3 via the IAP driver. This is necessary when using an encrypted image.

Secure Programming

For background, refer to the "Security in Low Power Flash Devices" chapter of the *Fusion FPGA Fabric User's Guide* on the SoC Products Group website. SmartFusion ISP behaves identically to Fusion ISP. IAP of SmartFusion cSoCs is accomplished by using the IAP driver. Only the FPGA fabric and the eNVM can be reprogrammed with the protection of security measures by using the IAP driver.

Typical Programming and Erase Times

Table 4-3 documents the typical programming and erase times for two components of SmartFusion cSoCs, FPGA fabric and eNVM, using the SoC Products Group's FlashPro hardware and software. These times will be different for other ISP and IAP methods. The **Program** action in FlashPro software includes erase, program, and verify to complete.

The typical programming (including erase) time per page of the eNVM is 8 ms.

Table 4-3 • **Typical Programming and Erase Times**

	FPGA Fabric (seconds)	eNVM (seconds)
Device	**A2F500**	**A2F500**
Erase	21	N/A
Program	15	26
Verify	16	42

References

User's Guides

DirectC User's Guide

http://www.microsemi.com/soc/documents/DirectC_UG.pdf

Fusion FPGA Fabric User's Guide

http://www.microsei.com/soc/documents/Fusion_UG.pdf

Chapters:

"In-System Programming (ISP) of Actel's Low-Power Flash Devices Using FlashPro4/3/3X"

"Security in Low Power Flash Devices"

"Programming Flash Devices"

"Microprocessor Programming of Actel's Low-Power Flash Devices"

5 – Pin Descriptions

Supply Pins

Name	Type	Description
GND	Ground	Digital ground to the FPGA fabric, microcontroller subsystem and GPIOs
GND15ADC0	Ground	Quiet analog ground to the 1.5 V circuitry of the first analog-to-digital converter (ADC)
GND15ADC1	Ground	Quiet analog ground to the 1.5 V circuitry of the second ADC
GND15ADC2	Ground	Quite analog ground to the 1.5 V circuitry of the third ADC
GND33ADC0	Ground	Quiet analog ground to the 3.3 V circuitry of the first ADC
GND33ADC1	Ground	Quiet analog ground to the 3.3 V circuitry of the second ADC
GND33ADC2	Ground	Quiet analog ground to the 3.3 V circuitry of the third ADC
GNDA	Ground	Quiet analog ground to the analog front-end
GNDAQ	Ground	Quiet analog ground to the analog I/O of SmartFusion cSoCs
GNDENVM	Ground	Digital ground to the embedded nonvolatile memory (eNVM)
GNDLPXTAL	Ground	Analog ground to the low power 32 KHz crystal oscillator circuitry
GNDMAINXTAL	Ground	Analog ground to the main crystal oscillator circuitry
GNDQ	Ground	Quiet digital ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND.
GNDRCOSC	Ground	Analog ground to the integrated RC oscillator circuit
GNDSDD0	Ground	Analog ground to the first sigma-delta DAC
GNDSDD1	Ground	Common analog ground to the second and third sigma-delta DACs
GNDTM0	Ground	Analog temperature monitor common ground for signal conditioning blocks SCB 0 and SCB 1 (see information for pins "TM0" and "TM1" in the "Analog Front-End (AFE)" section on page 5-13).
GNDTM1	Ground	Analog temperature monitor common ground for signal conditioning block SCB 2 and SBCB 3 (see information for pins "TM2" and "TM3" in the "Analog Front-End (AFE)" section on page 5-13).
GNDTM2	Ground	Analog temperature monitor common ground for signal conditioning block SCB4
GNDVAREF	Ground	Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.
VCC	Supply	Digital supply to the FPGA fabric and MSS, nominally 1.5 V. VCC is also required for powering the JTAG state machine, in addition to VJTAG. Even when a SmartFusion cSoC is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the SmartFusion cSoC.
VCC15A	Supply	Clean analog 1.5 V supply to the analog circuitry. Always power this pin.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*

Analog Front-End (AFE)

Name	Type	Description	Associated With	
			ADC/SDD	SCB
ABPS0	In	SCB 0 / active bipolar prescaler input 1. See the Active Bipolar Prescaler (ABPS) section in the *SmartFusion Programmable Analog User's Guide*.	ADC0	SCB0
ABPS1	In	SCB 0 / active bipolar prescaler Input 2	ADC0	SCB0
ABPS2	In	SCB 1 / active bipolar prescaler Input 1	ADC0	SCB1
ABPS3	In	SCB 1 / active bipolar prescaler Input 2	ADC0	SCB1
ABPS4	In	SCB 2 / active bipolar prescaler Input 1	ADC1	SCB2
ABPS5	In	SCB 2 / active bipolar prescaler Input 2	ADC1	SCB2
ABPS6	In	SCB 3 / active bipolar prescaler Input 1	ADC1	SCB3
ABPS7	In	SCB 3 / active bipolar prescaler input 2	ADC1	SCB3
ABPS8	In	SCB 4 / active bipolar prescaler input 1	ADC2	SCB4
ABPS9	In	SCB 4 / active bipolar prescaler input 2	ADC2	SCB4
ADC0	In	ADC 0 direct input 0 / FPGA Input. See the "Sigma-Delta Digital-to-Analog Converter (DAC)" section in the *SmartFusion Programmable Analog User's Guide*.	ADC0	SCB0
ADC1	In	ADC 0 direct input 1 / FPGA input	ADC0	SCB0
ADC2	In	ADC 0 direct input 2 / FPGA input	ADC0	SCB1
ADC3	In	ADC 0 direct input 3 / FPGA input	ADC0	SCB1
ADC4	In	ADC 1 direct input 0 / FPGA input	ADC1	SCB2
ADC5	In	ADC 1 direct input 1 / FPGA input	ADC1	SCB2
ADC6	In	ADC 1 direct input 2 / FPGA input	ADC1	SCB3
ADC7	In	ADC 1 direct input 3 / FPGA input	ADC1	SCB3
ADC8	In	ADC 2 direct input 0 / FPGA input	ADC2	SCB4
ADC9	In	ADC 2 direct input 1 / FPGA input	ADC2	SCB4
ADC10	In	ADC 2 direct input 2 / FPGA input	ADC2	N/A
ADC11	In	ADC 2 direct input 3 / FPGA input	ADC2	N/A
CM0	In	SCB 0 / high side of current monitor / comparator Positive input. See the Current Monitor section in the *SmartFusion Programmable Analog User's Guide*.	ADC0	SCB0
CM1	In	SCB 1 / high side of current monitor / comparator. Positive input.	ADC0	SCB1
CM2	In	SCB 2 / high side of current monitor / comparator. Positive input.	ADC1	SCB2
CM3	In	SCB 3 / high side of current monitor / comparator. Positive input.	ADC1	SCB3
CM4	In	SCB 4 / high side of current monitor / comparator. Positive input.	ADC2	SCB4

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

Pin No.	FG256	
	A2F060 Function	A2F500 Function
J5	NC	GNDQ
J6	GND	GND
J7	VCC	VCC
J8	GND	GND
J9	VCC	VCC
J10	GND	GND
J11	VCCMSSIOB2	VCCMSSIOB2
J12	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
J13	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
J14	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
J15	VCCMSSIOB2	VCCMSSIOB2
J16	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
K1	GPIO_1/IO32RSB4V0	MAC_MDIO/IO58RSB4V0
K2	GPIO_0/IO33RSB4V0	MAC_MDC/IO57RSB4V0
K3	VCCMSSIOB4	VCCMSSIOB4
K4	MSS_RESET_N	MSS_RESET_N
K5	VCCRCOSC	VCCRCOSC
K6	VCCMSSIOB4	VCCMSSIOB4
K7	GND	GND
K8	VCC	VCC
K9	GND	GND
K10	VCC	VCC
K11	GND	GND
K12	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
K13	GND	GND
K14	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
K15	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
K16	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
L1	GND	GND
L2	GPIO_2/IO31RSB4V0	MAC_TXEN/IO61RSB4V0
L3	GPIO_3/IO30RSB4V0	MAC_CRSDV/IO60RSB4V0
L4	GPIO_4/IO29RSB4V0	MAC_RXER/IO59RSB4V0
L5	GPIO_9/IO24RSB4V0	MAC_CLK

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

FG484	
Pin Number	**A2F500 Function**
B9	EMC_BYTEN[0]/GAC0/IO07NDB0V0
B10	EMC_AB[2]/IO09NDB0V0
B11	EMC_AB[3]/IO09PDB0V0
B12	EMC_AB[6]/IO12NDB0V0
B13	EMC_AB[14]/IO15NDB0V0
B14	EMC_AB[15]/IO15PDB0V0
B15	VCCFPGAIOB0
B16	EMC_AB[18]/IO18NDB0V0
B17	EMC_AB[19]/IO18PDB0V0
B18	VCCFPGAIOB0
B19	GBB0/IO24NDB0V0
B20	GBB1/IO24PDB0V0
B21	GND
B22	GBA2/IO27PDB1V0
C1	EMC_DB[14]/GAB2/IO88NDB5V0
C2	NC
C3	NC
C4	IO01NDB0V0
C5	IO01PDB0V0
C6	EMC_CLK/GAA0/IO02NDB0V0
C7	IO03PPB0V0
C8	IO04NPB0V0
C9	EMC_BYTEN[1]/GAC1/IO07PDB0V0
C10	EMC_OEN1_N/IO08PDB0V0
C11	GND
C12	VCCFPGAIOB0
C13	EMC_AB[8]/IO13NDB0V0
C14	EMC_AB[16]/IO17NDB0V0
C15	EMC_AB[17]/IO17PDB0V0
C16	EMC_AB[24]/IO20NDB0V0
C17	EMC_AB[22]/IO19NDB0V0
C18	EMC_AB[23]/IO19PDB0V0
C19	GBA0/IO23NPB0V0
C20	NC
C21	GBC2/IO30PDB1V0
C22	GBB2/IO27NDB1V0
D1	GND

FG484	
Pin Number	**A2F500 Function**
D2	EMC_DB[12]/IO87NDB5V0
D3	EMC_DB[13]/GAC2/IO87PDB5V0
D4	NC
D5	NC
D6	GND
D7	IO00NPB0V0
D8	IO03NPB0V0
D9	GND
D10	EMC_OEN0_N/IO08NDB0V0
D11	EMC_AB[10]/IO11NDB0V0
D12	EMC_AB[11]/IO11PDB0V0
D13	EMC_AB[9]/IO13PDB0V0
D14	GND
D15	GBC1/IO22PPB0V0
D16	EMC_AB[25]/IO20PDB0V0
D17	GND
D18	GBA1/IO23PPB0V0
D19	NC
D20	NC
D21	IO30NDB1V0
D22	GND
E1	GFC2/IO84PPB5V0
E2	VCCFPGAIOB5
E3	GFA2/IO85PDB5V0
E4	GND
E5	NC
E6	GNDQ
E7	VCCFPGAIOB0
E8	IO00PPB0V0
E9	NC
E10	VCCFPGAIOB0
E11	EMC_AB[4]/IO10NDB0V0
E12	EMC_AB[5]/IO10PDB0V0
E13	VCCFPGAIOB0
E14	GBC0/IO22NPB0V0
E15	NC
E16	VCCFPGAIOB0

FG484	
Pin Number	A2F500 Function
J3	EMC_DB[4]/GEA0/IO78NDB5V0
J4	EMC_DB[3]/GEC2/IO77PPB5V0
J5	VCCFPGAIOB5
J6	GFA0/IO81NDB5V0
J7	VCCFPGAIOB5
J8	GND
J9	VCC
J10	GND
J11	VCC
J12	GND
J13	VCC
J14	GND
J15	VCC
J16	GND
J17	IO37PDB1V0
J18	VCCFPGAIOB1
J19	GCA0/IO36NDB1V0
J20	GCA1/IO36PDB1V0
J21	GCC1/IO35PPB1V0
J22	GCB1/IO34PDB1V0
K1	GND
K2	EMC_DB[0]/GEA2/IO76NDB5V0
K3	EMC_DB[1]/GEB2/IO76PDB5V0
K4	IO74PPB5V0
K5	EMC_DB[2]/IO77NPB5V0
K6	IO75PDB5V0
K7	GND
K8	VCC
K9	GND
K10	VCC
K11	GND
K12	VCC
K13	GND
K14	VCC
K15	GND
K16	VCCFPGAIOB1
K17	IO37NDB1V0

FG484	
Pin Number	A2F500 Function
K18	GDA1/IO40PDB1V0
K19	GDA0/IO40NDB1V0
K20	GDC1/IO38PDB1V0
K21	GDC0/IO38NDB1V0
K22	GND
L1	IO73PDB5V0
L2	IO73NDB5V0
L3	IO72PPB5V0
L4	GND
L5	IO74NPB5V0
L6	IO75NDB5V0
L7	VCCFPGAIOB5
L8	GND
L9	VCC
L10	GND
L11	VCC
L12	GND
L13	VCC
L14	GND
L15	VCC
L16	GND
L17	GNDQ
L18	GDA2/IO42NDB1V0
L19	VCCFPGAIOB1
L20	GDB1/IO39PDB1V0
L21	GDB0/IO39NDB1V0
L22	GDC2/IO41PDB1V0
M1	IO71PDB5V0
M2	IO71NDB5V0
M3	VCCFPGAIOB5
M4	IO72NPB5V0
M5	GNDQ
M6	IO68PDB5V0
M7	GND
M8	VCC
M9	GND
M10	VCC

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,400 employees globally. Learn more at **www.microsemi.com**.

51700120-2/03.15