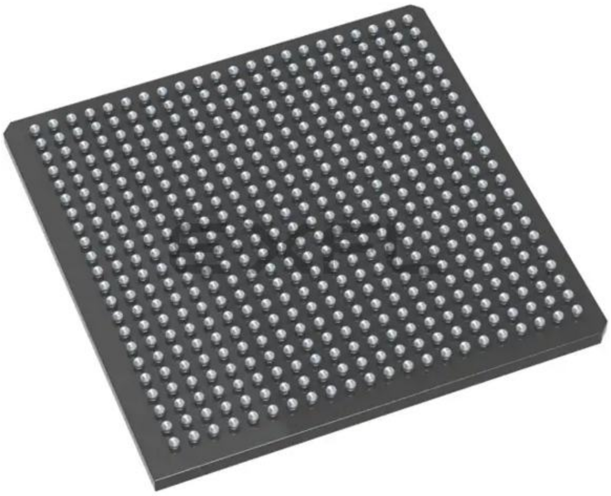
Microchip Technology - A2F500M3G-FGG484M Datasheet



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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Speed	80MHz
Primary Attributes	ProASIC®3 FPGA, 500K Gates, 11520 D-Flip-Flops
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a2f500m3g-fgg484m

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100°C - 70°C}{16.4\ W} = 1.82\ W$$

EQ 6

The 1.82 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 7:

$$\theta_{JA(total)} = \frac{T_J - T_A}{P} = \frac{100°C - 70°C}{3.00\ W} = 10.00°C/W$$

EQ 7

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 8

where

θ_{JA} = 0.37°C/W

= Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

θ_{SA} = Thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 9

$$\theta_{SA} = 10°C/W - 7.5°C/W - 0.37°C/W = 2.5°C/W$$

A heat sink with a thermal resistance of 2.5°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

Temperature and Voltage Derating Factors

Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 125°C, worst-case VCC = 1.425 V)

Array Voltage VCC (V)		Junction Temperature (°C)						
	–55°C	–40°C	0°C	25°C	70°C	85°C	100°C	125°C
1.425	0.81	0.82	0.87	0.89	0.94	0.96	0.97	1.00
1.500	0.76	0.78	0.82	0.84	0.89	0.91	0.92	0.95
1.575	0.73	0.75	0.79	0.81	0.86	0.87	0.89	0.91

Standby Mode and Time Keeping Mode

$P_{NET} = 0\ W$

I/O Input Buffer Dynamic Contribution—P_{INPUTS}

SoC Mode

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * P_{AC9} * F_{CLK}$

Where:

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-17 on page 2-19.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$P_{INPUTS} = 0\ W$

I/O Output Buffer Dynamic Contribution—$P_{OUTPUTS}$

SoC Mode

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * P_{AC10} * F_{CLK}$

Where:

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-17 on page 2-19.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-18 on page 2-19.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$P_{OUTPUTS} = 0\ W$

FPGA Fabric SRAM Dynamic Contribution—P_{MEMORY}

SoC Mode

$P_{MEMORY} = (N_{BLOCKS} * P_{AC11} * \beta_2 * F_{READ-CLOCK}) + (N_{BLOCKS} * P_{AC12} * \beta_3 * F_{WRITE-CLOCK})$

Where:

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 2-18 on page 2-19.

β_3 the RAM enable rate for write operations—guidelines are provided in Table 2-18 on page 2-19.

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

Standby Mode and Time Keeping Mode

$P_{MEMORY} = 0\ W$

PLL/CCC Dynamic Contribution—P_{PLL}

SoC Mode

$P_{PLL} = P_{AC13} * F_{CLKOUT}$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.[1]

Standby Mode and Time Keeping Mode

---

[1] *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-35 • **Minimum and Maximum DC Output Levels, 3.3 V LVTTL/ 3.3 V LVCMOS Applicable to FPGA I/O Banks**

	VOL	VOL	VOH	VOH	IOL	IOH	IOSL	IOSH
Drive Strgth.	Max. V	Max. V	Min. V		mA	mA	Max. mA[1]	Max. mA[1]
	$-55 \leq T_J \leq 100$ (°C)	$100 < T_J \leq 125$(°C)	$-55 \leq T_J \leq 100$ (°C)	$100 < T_J \leq 125$(°C)	$-55 \leq T_J \leq 125$(°C)		$-55 \leq T_J \leq 100$(°C)	
2 mA	0.4	0.4	2.4	2.4	2	2	27	25
4 mA	0.4	0.4	2.4	2.4	4	4	27	25
6 mA	0.4	0.4	2.4	2.4	6	6	54	51
8 mA	0.4	0.4	2.4	2.4	8	8	54	51
12 mA	0.4	0.4	2.4	2.4	12	12	109	103
16 mA	0.4	0.4	2.4	2.4	16	16	127	132
24 mA	0.4	0.44	2.4	2.16	24	24	181	268

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Software default selection highlighted in gray.*

Table 2-36 • **Minimum and Maximum DC Input Levels, 3.3 V LVTTL/ 3.3 V LVCMOS Applicable to FPGA I/O Banks**

VIL		VIH		IIL	IIH
Min. V	Max. V	Min. V	Max. V	µA*	µA*
$-55 \leq T_J \leq 125$(°C)		$-55 \leq T_J \leq 125$(°C)		$-55 \leq T_J \leq 125$(°C)	
–0.3	0.8	2	3.6	15	15

*Note: *Currents are measured at 125°C junction temperature and maximum voltage.*

Table 2-37 • **Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks**

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-42 • **Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks**

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[1]**	**Max. mA[1]**	**µA[2]**	**µA[2]**
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	15	15
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	15	15
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	15	15
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	15	15
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	15	15
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	15	15
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-43 • **Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks**

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

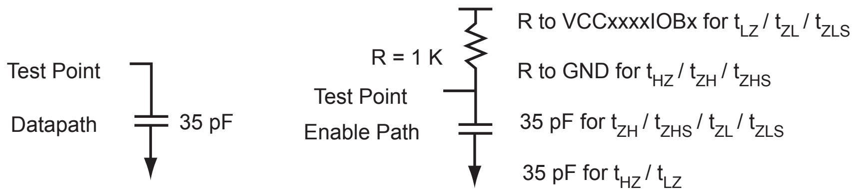

Figure 2-8 • **AC Loading**

Table 2-44 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

Note: *Measuring point = Vtrip. See Table 2-22 on page 2-25 for a complete table of trip points.

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-48 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	μA[2]	μA[2]
2 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	2	2	11	9	15	15
4 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	4	4	22	17	15	15
6 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	6	6	44	35	15	15
8 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	8	8	51	45	15	15
12 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	12	12	74	91	15	15
16 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	16	16	74	91	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-49 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	μA[2]	μA[2]
4 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	4	4	22	17	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

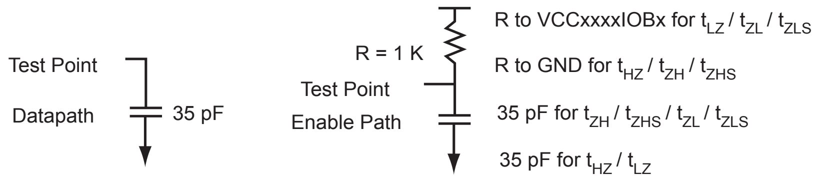

Figure 2-9 • AC Loading

Table 2-50 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	35

Note: *Measuring point = Vtrip. See Table 2-22 on page 2-25 for a complete table of trip points.

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-60 • **Minimum and Maximum DC Input and Output Levels**

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[1]**	**Max. mA[1]**	**µA[2]**	**µA[2]**
Per PCI specification	Per PCI curves										15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; SoC Products Group loadings for enable path characterization are described in Figure 2-11.

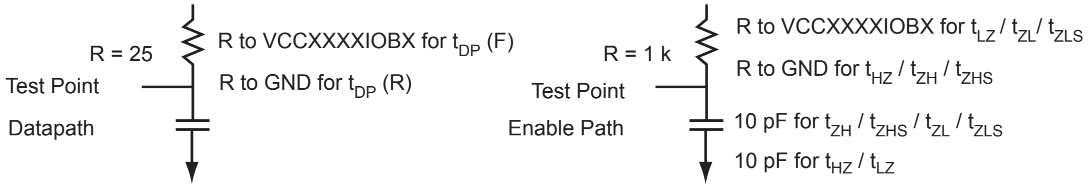

Figure 2-11 • **AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; SoC Products Group loading for tristate is described in Table 2-61.

Table 2-61 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCCxxxxIOBx for $t_{DP(R)}$ 0.615 * VCCxxxxIOBx for $t_{DP(F)}$	–	10

Note: *Measuring point = Vtrip. See Table 2-22 on page 2-25 for a complete table of trip points.

Timing Characteristics

Table 2-62 • **3.3 V PCI**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.62	2.72	0.04	0.88	0.41	2.77	2.02	3.28	3.62	4.97	4.22	ns
–1	0.52	2.26	0.03	0.73	0.34	2.30	1.68	2.73	3.02	4.14	3.52	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-63 • **3.3 V PCI-X**
Worst Military-Case Conditions: T_J =125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.62	2.72	0.04	0.83	0.41	2.77	2.02	3.28	3.62	4.97	4.22	ns
–1	0.52	2.26	0.03	0.69	0.34	2.30	1.68	2.73	3.02	4.14	3.52	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by SoC Products Group Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-12. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, SmartFusion cSoCs also support bus LVDS structure and multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

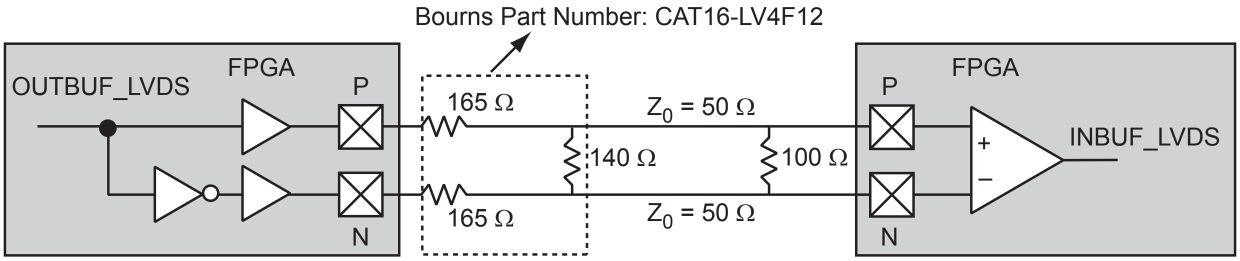

Figure 2-12 • **LVDS Circuit Diagram and Board-Level Implementation**

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

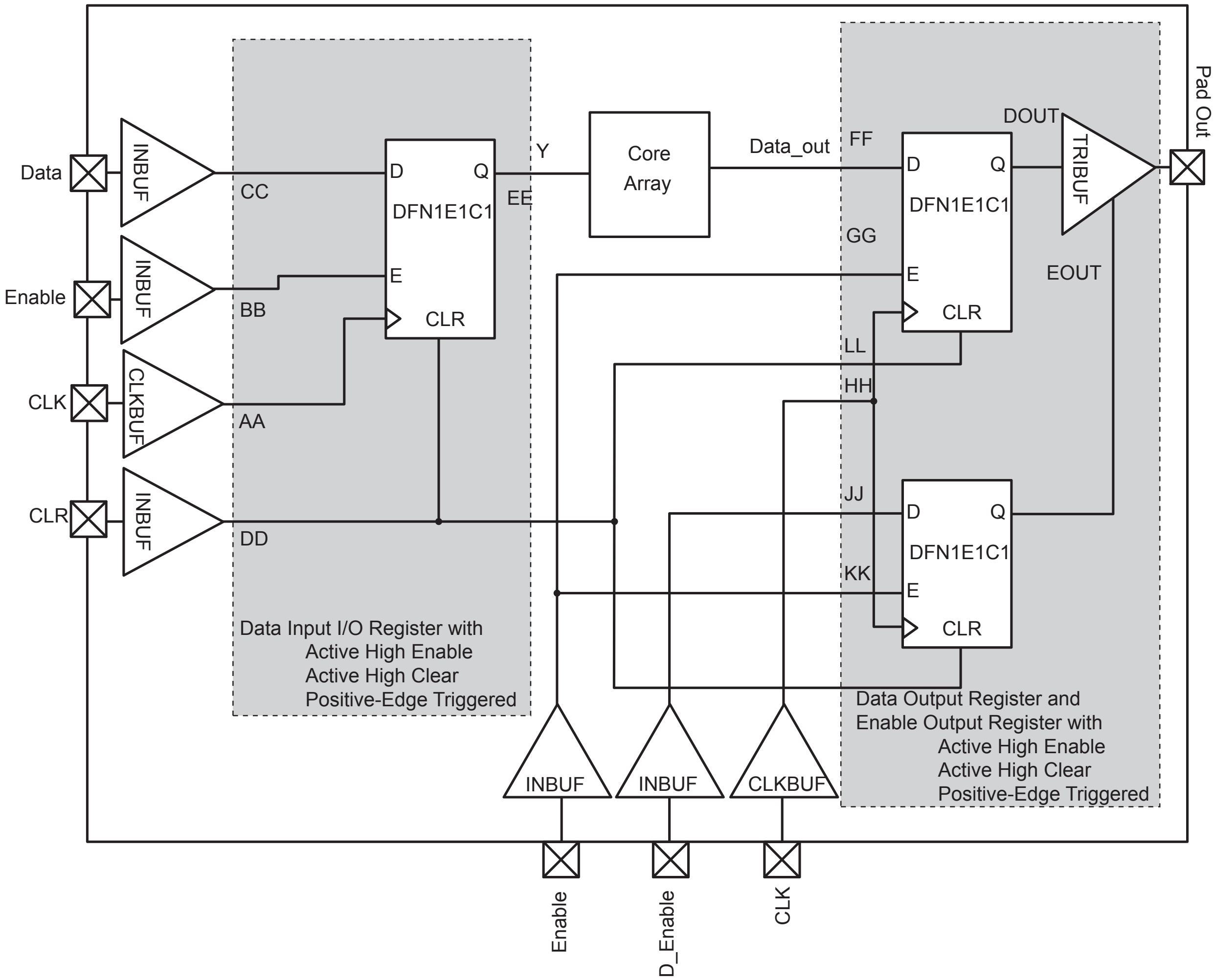

Figure 2-16 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

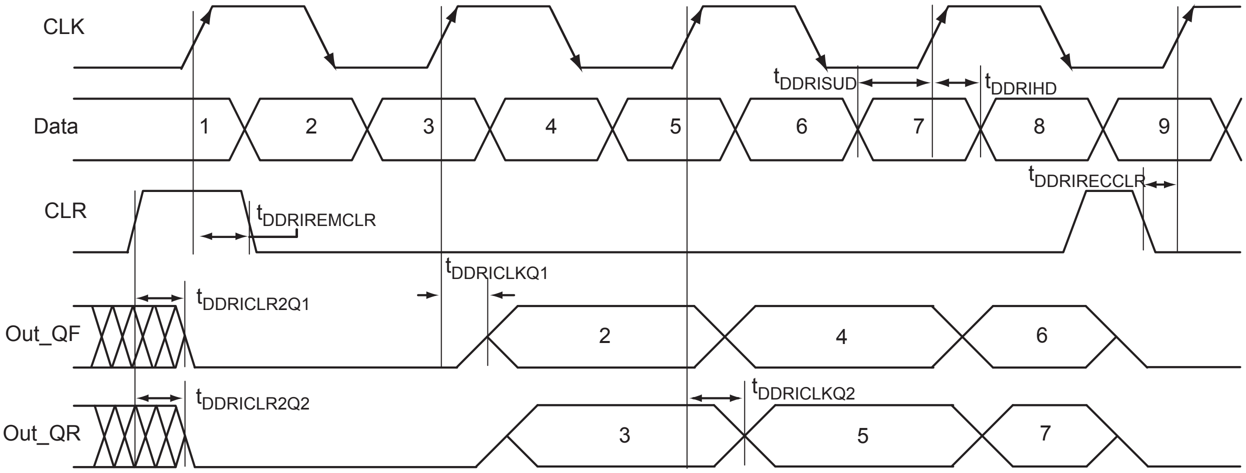

***Figure 2-21* • Input DDR Timing Diagram**

Timing Characteristics

***Table 2-76* • Input DDR Propagation Delays**
Worst Military-Case Conditions: T_J = 85°C, Worst Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.41	0.49	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.29	0.35	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.30	0.36	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.60	0.72	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.49	0.59	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal time for Input DDR	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery time for Input DDR	0.24	0.28	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	0.26	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.36	0.42	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.32	0.38	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	350	350	MHz

Note: *For derating values at specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.*

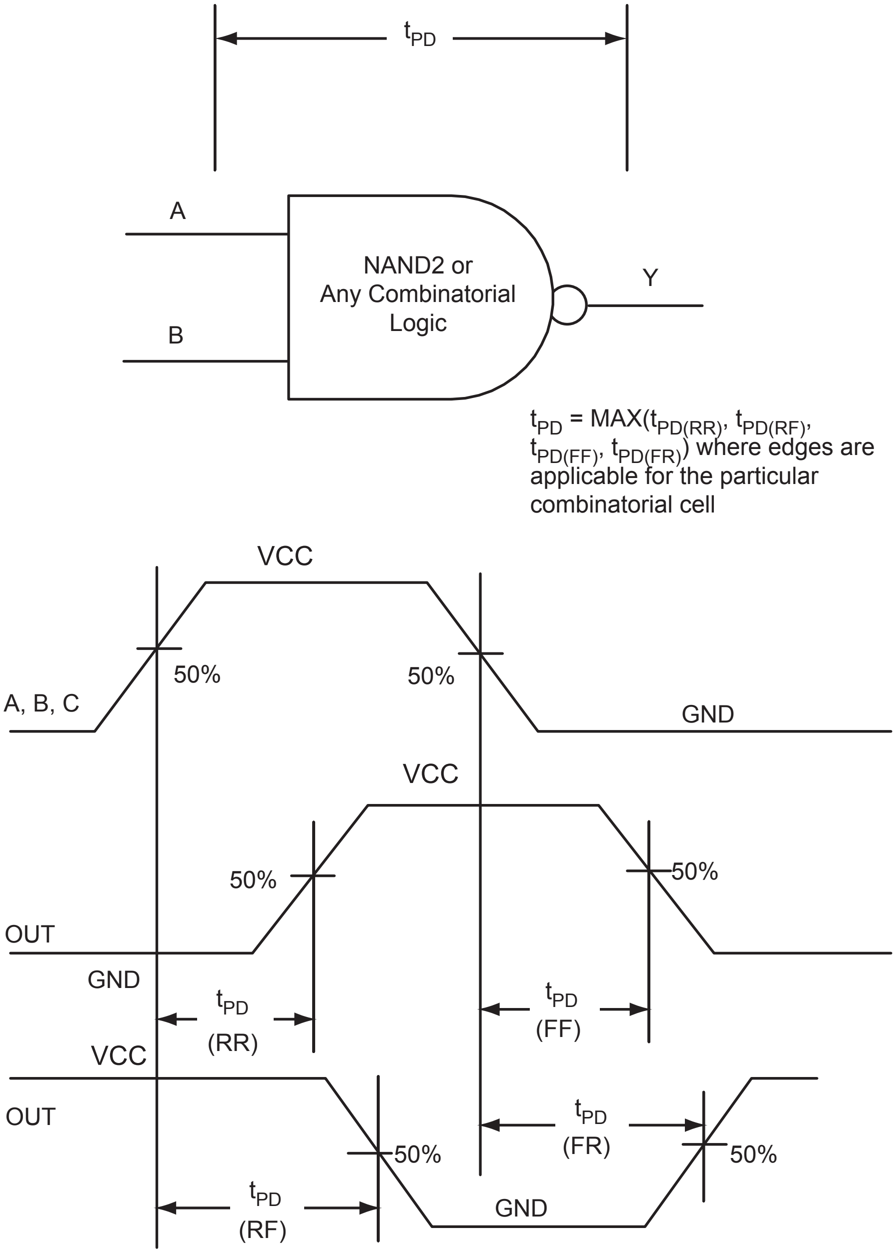

***Figure 2-25* • Timing Model and Waveforms**

Global Resource Characteristics

A2F500 Clock Tree Topology

Clock delays are device-specific. Figure 2-28 is an example of a global tree used for clock routing. The global tree presented in Figure 2-28 is driven by a CCC located on the west side of the A2F500 device. It is used to drive all D-flip-flops in the device.

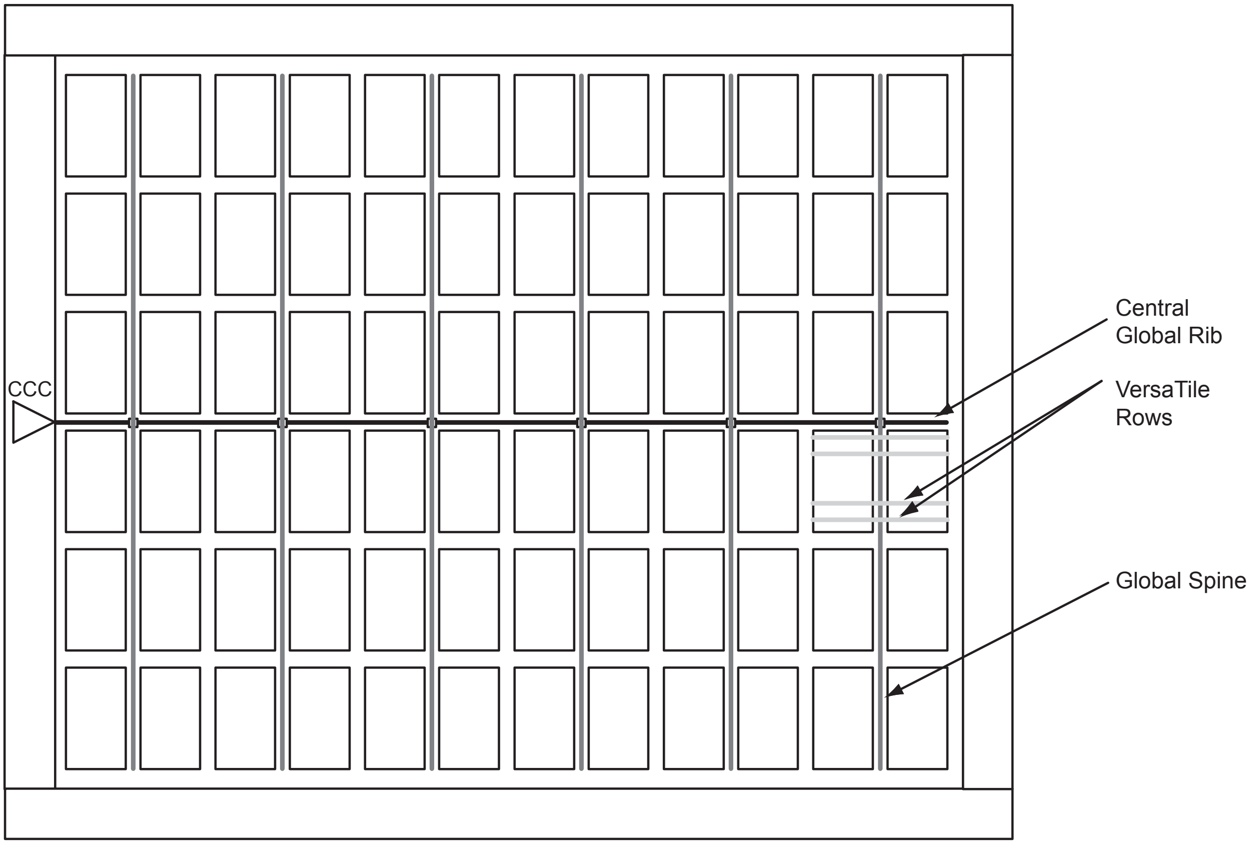

Figure 2-28 • **Example of Global Tree Use in an A2F500 Device for Clock Routing**

Timing Waveforms

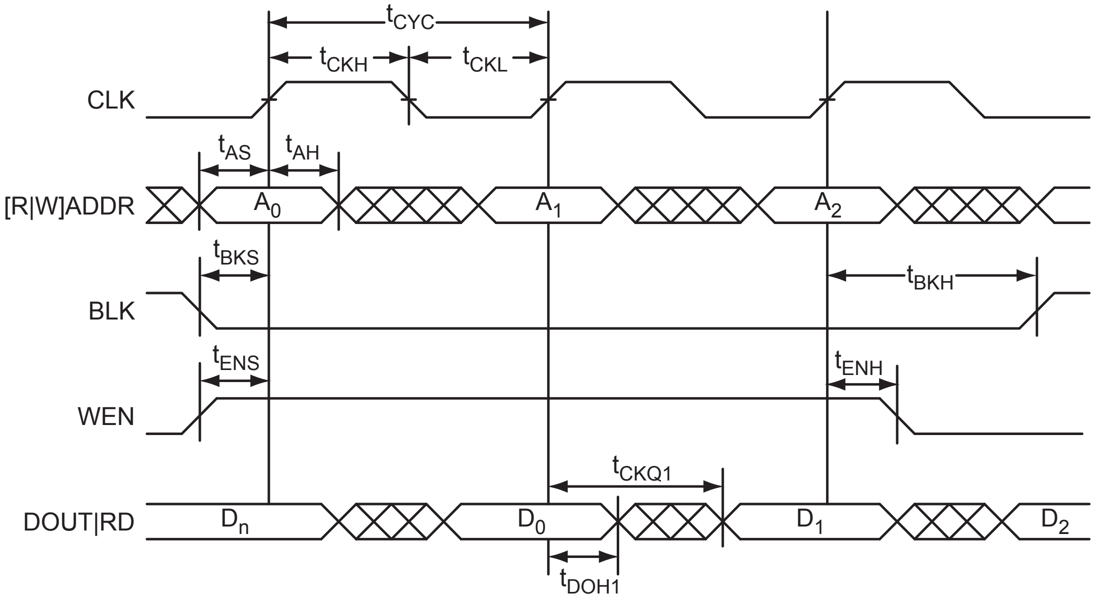

Figure 2-31 **• RAM Read for Pass-Through Output. Applicable to both RAM4K9 and RAM512x18.**

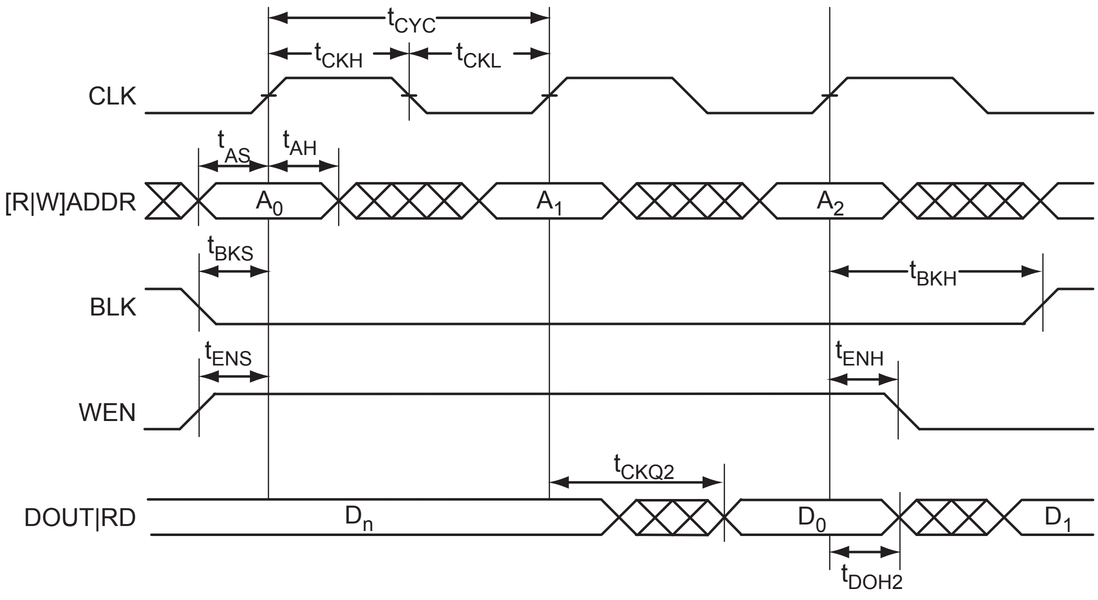

Figure 2-32 **• RAM Read for Pipelined Output Applicable to both RAM4K9 and RAM512x18.**

Programmable Analog Specifications

Current Monitor

Unless otherwise noted, current monitor performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 91 Ksps, after digital compensation. All results are based on averaging over 16 samples.

Table 2-93 • **Current Monitor Performance Specification**

Specification	Test Conditions	Min.	Typical	Max.	Units
Input voltage range (for driving ADC over full range)		0 – 48	0 – 50	1 – 51	mV
Analog gain	From the differential voltage across the input pads to the ADC input		50		V/V
Input referred offset voltage	Input referred offset voltage	0	0.1	0.5	mV
	–55ºC to +125ºC	0	0.1	0.5	mV
Gain error	Slope of BFSL vs. 50 V/V		±0.1	±0.7	% nom.
	–55ºC to +125ºC			±0.7	% nom.
Overall Accuracy	Peak error from ideal transfer function, 25°C		±(0.1 + 0.25%)	±(0.4 + 1.5%)	mV plus % reading
	–55ºC to +125ºC		±(0.1 + 0.25%)	±(1.5 + 1.5%)	mV plus % reading
Input referred noise	0 VDC input (no output averaging)	0.3	0.4	0.5	mVrms
Common-mode rejection ratio	0 V to 12 VDC common-mode voltage	–86	–87		dB
Analog settling time	To 0.1% of final value (with ADC load)				
	From CM_STB (High)	5			µs
	From ADC_START (High)	5		200	µs
Input capacitance			8		pF
Input biased current	CM[n] or TM[n] pad, –40°C to +100°C over maximum input voltage range (plus is into pad)				
	Strobe = 0; IBIAS on CM[n]		0		µA
	Strobe = 1; IBIAS on CM[n]		1		µA
	Strobe = 0; IBIAS on TM[n]		2		µA
	Strobe = 1; IBIAS on TM[n]		1		µA
Power supply rejection ratio	DC (0 – 10 KHz)	41	42		dB
Incremental operational current monitor power supply current requirements (per current monitor instance, not including ADC or VAREFx)	VCC33A		150		µA
	VCC33AP		140		µA
	VCC15A		50		µA

Note: *Under no condition should the TM pad ever be greater than 10 mV above the CM pad. This restriction is applicable only if current monitor is used.*

Analog Sigma-Delta Digital to Analog Converter (DAC)

Unless otherwise noted, sigma-delta DAC performance is specified at 25°C with nominal power supply voltages, using the internal sigma-delta modulators with 16-bit inputs, HCLK = 100 MHz, modulator inputs updated at a 100 KHz rate, in voltage output mode with an external 160 pF capacitor to ground, after trimming and digital [pre-]compensation.

Table 2-99 • **Analog Sigma-Delta DAC**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Resolution		8		24	Bits
Output range			0 to 2.56		V
	Current output mode		0 to 256		µA
Output Impedance		6	10	12	KΩ
	Current output mode	10			MΩ
Output voltage compliance	Current output mode		0–3.0		V
	–40ºC to +100ºC	0–2.7		0–3.4	V
Gain error	Voltage output mode		0.3	±2	%
	–40ºC to +100ºC		0.3	±2	%
	–55ºC to +125ºC		0.3	±6	%
	Current output mode		0.3	±2	%
	–40ºC to +100ºC		0.3	±2	%
	–55ºC to +125ºC		0.3	±6	%
Output referred offset	DACBYTE0 = h’00 (8-bit)		0.25	±1	mV
	–40ºC to +100ºC		1	±2.5	mV
	Current output mode		0.3	±1	µA
	–40ºC to +100ºC		1	±2.5	µA
Integral non-linearity	RMS deviation from BFSL		0.1	0.4	% FS*
Differential non-linearity			0.05	0.4	% FS*
Analog settling time			Refer to Figure 2-44 on page 2-87		µs
Power supply rejection ratio	DC, full scale output	33	34		dB

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User’s Guide for more information.*

Re-Programming the eNVM Blocks Using the Cortex-M3

In this mode the Cortex-M3 is executing the eNVM programming algorithm from eSRAM. Since individual pages (132 bytes) of the eNVM can be write-protected, the programming algorithm software can be protected from inadvertent erasure. When reprogramming the eNVM, both MSS I/Os and FPGA I/Os are available as interfaces for sourcing the new eNVM image. The SoC Products Group provides working example projects for SoftConsole, IAR, and Keil development environments. These can be downloaded via the SoC Products Group Firmware Catalog.

Alternately, the eNVM can be reprogrammed by the Cortex-M3 via the IAP driver. This is necessary when using an encrypted image.

Secure Programming

For background, refer to the "Security in Low Power Flash Devices" chapter of the *Fusion FPGA Fabric User's Guide* on the SoC Products Group website. SmartFusion ISP behaves identically to Fusion ISP. IAP of SmartFusion cSoCs is accomplished by using the IAP driver. Only the FPGA fabric and the eNVM can be reprogrammed with the protection of security measures by using the IAP driver.

Typical Programming and Erase Times

Table 4-3 documents the typical programming and erase times for two components of SmartFusion cSoCs, FPGA fabric and eNVM, using the SoC Products Group's FlashPro hardware and software. These times will be different for other ISP and IAP methods. The **Program** action in FlashPro software includes erase, program, and verify to complete.

The typical programming (including erase) time per page of the eNVM is 8 ms.

***Table 4-3* • Typical Programming and Erase Times**

	FPGA Fabric (seconds)	eNVM (seconds)
Device	**A2F500**	**A2F500**
Erase	21	N/A
Program	15	26
Verify	16	42

References

User's Guides

DirectC User's Guide

http://www.microsemi.com/soc/documents/DirectC_UG.pdf

Fusion FPGA Fabric User's Guide

http://www.microsei.com/soc/documents/Fusion_UG.pdf

Chapters:

"In-System Programming (ISP) of Actel's Low-Power Flash Devices Using FlashPro4/3/3X"

"Security in Low Power Flash Devices"

"Programming Flash Devices"

"Microprocessor Programming of Actel's Low-Power Flash Devices"

5 – Pin Descriptions

Supply Pins

Name	Type	Description
GND	Ground	Digital ground to the FPGA fabric, microcontroller subsystem and GPIOs
GND15ADC0	Ground	Quiet analog ground to the 1.5 V circuitry of the first analog-to-digital converter (ADC)
GND15ADC1	Ground	Quiet analog ground to the 1.5 V circuitry of the second ADC
GND15ADC2	Ground	Quite analog ground to the 1.5 V circuitry of the third ADC
GND33ADC0	Ground	Quiet analog ground to the 3.3 V circuitry of the first ADC
GND33ADC1	Ground	Quiet analog ground to the 3.3 V circuitry of the second ADC
GND33ADC2	Ground	Quiet analog ground to the 3.3 V circuitry of the third ADC
GNDA	Ground	Quiet analog ground to the analog front-end
GNDAQ	Ground	Quiet analog ground to the analog I/O of SmartFusion cSoCs
GNDENVM	Ground	Digital ground to the embedded nonvolatile memory (eNVM)
GNDLPXTAL	Ground	Analog ground to the low power 32 KHz crystal oscillator circuitry
GNDMAINXTAL	Ground	Analog ground to the main crystal oscillator circuitry
GNDQ	Ground	Quiet digital ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND.
GNDRCOSC	Ground	Analog ground to the integrated RC oscillator circuit
GNDSDD0	Ground	Analog ground to the first sigma-delta DAC
GNDSDD1	Ground	Common analog ground to the second and third sigma-delta DACs
GNDTM0	Ground	Analog temperature monitor common ground for signal conditioning blocks SCB 0 and SCB 1 (see information for pins "TM0" and "TM1" in the "Analog Front-End (AFE)" section on page 5-13).
GNDTM1	Ground	Analog temperature monitor common ground for signal conditioning block SCB 2 and SBCB 3 (see information for pins "TM2" and "TM3" in the "Analog Front-End (AFE)" section on page 5-13).
GNDTM2	Ground	Analog temperature monitor common ground for signal conditioning block SCB4
GNDVAREF	Ground	Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.
VCC	Supply	Digital supply to the FPGA fabric and MSS, nominally 1.5 V. VCC is also required for powering the JTAG state machine, in addition to VJTAG. Even when a SmartFusion cSoC is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the SmartFusion cSoC.
VCC15A	Supply	Clean analog 1.5 V supply to the analog circuitry. Always power this pin.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*

Name	Type	Description
VCC15ADC0	Supply	Analog 1.5 V supply to the first ADC. Always power this pin.
VCC15ADC1	Supply	Analog 1.5 V supply to the second ADC. Always power this pin.
VCC15ADC2	Supply	Analog 1.5 V supply to the third ADC. Always power this pin.
VCC33A	Supply	Clean 3.3 V analog supply to the analog circuitry. VCC33A is also used to feed the 1.5 V voltage regulator for designs that do not provide an external supply to VCC. Refer to the Voltage Regulator (VR), Power Supply Monitor (PSM), and Power Modes section in the *SmartFusion Microcontroller Subsystem User's Guide* for more information.
VCC33ADC0	Supply	Analog 3.3 V supply to the first ADC. Never ground this pin. Can be left floating if unused.[1]
VCC33ADC1	Supply	Analog 3.3 V supply to the second ADC. Never ground this pin. Can be left floating if unused.[1]
VCC33ADC2	Supply	Analog 3.3 V supply to the third ADC. Never ground this pin. Can be left floating if unused.[1]
VCC33AP	Supply	Analog clean 3.3 V supply to the charge pump. To avoid high current draw, VCC33AP should be powered up simultaneously with or after VCC33A. Can be pulled down if unused.[1]
VCC33N	Supply	–3.3 V output from the voltage converter. A 2.2 µF capacitor must be connected from this pin to GND. Analog charge pump capacitors are not needed if none of the analog SCB features are used and none of the SDDs are used. In that case it should be left unconnected.
VCC33SDD0	Supply	Analog 3.3 V supply to the first sigma-delta DAC
VCC33SDD1	Supply	Common analog 3.3 V supply to the second and third sigma-delta DACs
VCCENVM	Supply	Digital 1.5 V power supply to the embedded nonvolatile memory blocks. To avoid high current draw, VCC should be powered up before or simultaneously with VCCENVM.
VCCESRAM	Supply	Digital 1.5 V power supply to the embedded SRAM blocks. Available only on the 208PQFP package. It should be connected to VCC (in other packages, it is internally connected to VCC).
VCCFPGAIOB0	Supply	Digital supply to the FPGA fabric I/O bank 0 (north FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.
VCCFPGAIOB1	Supply	Digital supply to the FPGA fabric I/O bank 1 (east FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.
VCCFPGAIOB5	Supply	Digital supply to the FPGA fabric I/O bank 5 (west FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*

Global I/O Naming Conventions

Gmn (Gxxx) refers to Global I/Os. These Global I/Os are used to connect the input to global networks. Global networks have high fanout and low skew. The naming convention for Global I/Os is as follows:

G = Global

m = Global pin location associated with each CCC on the device:

- A (northwest corner)
- B (northeast corner)
- C (east middle)
- D (southeast corner)
- E (southwest corner)
- F (west middle)

n = Global input MUX and pin number of the associated Global location m—A0, A1, A2, B0, B1, B2, C0, C1, or C2.

Global (GL) I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities.

Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the clocking resources chapter of the *SmartFusion FPGA Fabric User's Guide* and the clock conditioning circuitry chapter of the *SmartFusion Microcontroller Subsystem User's Guide*.

All inputs labeled GC/GF are direct inputs into the quadrant clocks. The inputs to the global network are multiplexed, and only one input can be used as a global input. For example, if GAA0 is used as a quadrant global input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals.

User Pins

Name	Type	Polarity/Bus Size	Description
GPIO_x	In/out	32	Microcontroller Subsystem (MSS) General Purpose I/O (GPIO). The MSS GPIO pin functions as an input, output, tristate, or bidirectional buffer with configurable interrupt generation and Schmitt trigger support. Input and output signal levels are compatible with the I/O standard selected. Unused GPIO pins are tristated and do not include pull-up or pull-down resistors. During power-up, the used GPIO pins are tristated with no pull-up or pull-down resistors until Sys boot configures them. Some of these pins are also multiplexed with integrated peripherals in the MSS (SPI, I^2C, and UART). GPIOs can be routed to dedicated I/O buffers (MSSIOBUF) or in some cases to the FPGA fabric interface through an IOMUX. This allows GPIO pins to be multiplexed as either I/Os for the FPGA fabric, the ARM® Cortex-M3 or for given integrated MSS peripherals. The MSS peripherals are not multiplexed with each other; they are multiplexed only with the GPIO block. For more information, see the General Purpose I/O Block (GPIO) section in the *SmartFusion Microcontroller Subsystem User's Guide*.
IO	In/out		FPGA user I/O