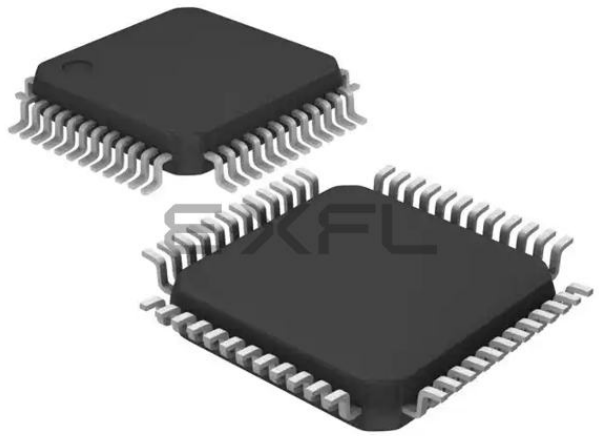

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	15
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmba4f0vlf

  - 10.4 kBit/s
  - 20 kBit/s
  - Fast Mode (up to 250 kBit/s)
- Selectable pull-up of 34 k or 330 k (in Shutdown Mode, 330 k only)
- Current limitation for LIN Bus pin falling edge.
- Over-current protection.
- LIN TxD-dominant timeout feature monitoring the LPTxD signal.
- Automatic transmitter shutdown in case of an over-current or TxD-dominant timeout.
- Fulfills the OEM “Hardware Requirements for LIN (CAN and FlexRay) Interfaces in Automotive Applications” v1.3.

1.4.9 Serial communication interface module (SCI)

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 16-bit baud rate selection
- Programmable character length
- Programmable polarity for transmitter and receiver
- Active edge receive wakeup
- Break detect and transmit collision detect supporting LIN

1.4.10 Serial peripheral interface module (SPI)

- Configurable 8- or 16-bit data size
- Full-duplex or single-wire bidirectional
- Double-buffered transmit and receive
- Master or slave mode
- MSB-first or LSB-first shifting
- Serial clock phase and polarity options

1.4.11 Analog-to-digital converter module (ADC)

- Selectable 10-bit or 8-bit resolution
- Up to 12 external channels & 8 internal channels
- 2.2us for single 10-bit resolution conversion
- Left or right aligned result data
- Continuous conversion mode
- Programmers model with list based command and result storage architecture

1.7.4 Package and pinouts

The following package options are offered.

- 48LQFP
- 64LQFP

The pin outs are shown in the following diagrams. The signal to pin mapping is specified in Table 1-7

Pins specified as N.C. have no physical connection to silicon.

Figure 1-3. MC9S12ZVMB-Family 48-pin LQFP pin out

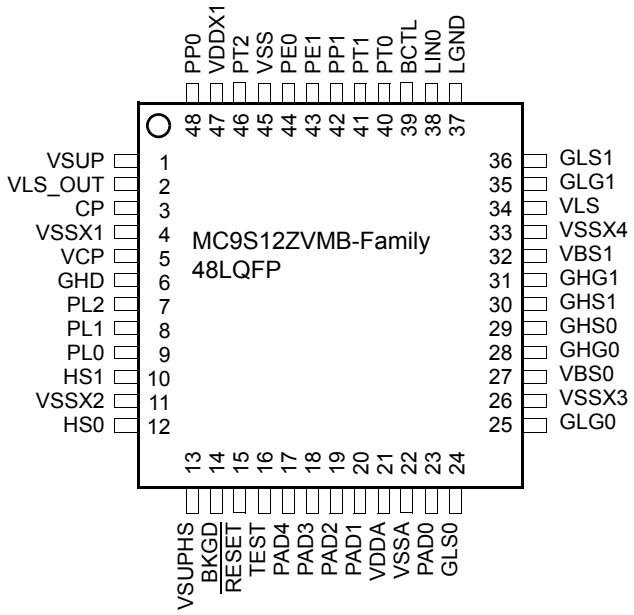

Table 1-14. Interrupt vector locations (Sheet 1 of 4)

Vector Address[1]	Interrupt Source	CCR Mask	Local Enable	Wake up from STOP	Wake up from WAIT
Vector base + 0x130 to Vector base + 0x114	Reserved				
Vector base + 0x110	NGPIO over-current (Port T)	I bit	OCIET[2]	No	Yes
Vector base + 0x10C	Port P interrupt	I bit	PIEP[1:0]	Yes	Yes
Vector base + 0x108	EVDD over-current	I bit	OCIEP[0]	No	Yes
Vector base + 0x104	Low-voltage interrupt (LVI)	I bit	CPMUCTRL (LVIE)	No	Yes
Vector base + 0x100	Autonomous periodical interrupt (API)	I bit	CPMUAPICTRL (APIE)	Yes	Yes
Vector base + 0x0FC	High temperature interrupt	I bit	CPMUHTCTL(HTIE)	No	Yes
Vector base + 0x0F8	Reserved				
Vector base + 0x0F4	Port AD interrupt	I bit	PIEADH(PIEADH0) PIEADL(PIEADL[7:0])	Yes	Yes
Vector base + 0x0F0	PTU Reload Overrun	I bit	PTUIEH(PTUROIE)	No	Yes
Vector base + 0x0EC	PTU Trigger0 Error	I bit	PTUIEL(TG0AEIE,TG0REIE, TG0TEIE)	No	Yes
Vector base + 0x0E8	Reserved				
Vector base + 0x0E4	PTU Trigger0 Done	I bit	PTUIEL[TG0DIE]	No	Yes
Vector base + 0x0E0 to Vector base + 0x0D4	Reserved				
Vector base + 0x0D0	PMF Reload A	I bit	PMFENCA(PWMRIEA)	No	Yes
Vector base + 0x0CC	PMF Reload B	I bit	PMFENCB(PWMRIEB)	No	Yes
Vector base + 0x0C8	PMF Reload C	I bit	PMFENCC(PWMRIEC)	No	Yes
Vector base + 0x0C4	PMF Fault	I bit	PMFFIE(FIE[5:0])	No	Yes
Vector base + 0x0C0	PMF Reload Overrun	I bit	PMFROIE(PMFROIEA,PMF ROIEB,PMFROIEC)	No	Yes
Vector base + 0x0BC	Port L interrupt	I bit	PIEL[2:0]	Yes	Yes
Vector base + 0x0B8 to Vector base + 0x0B0	Reserved				
Vector base + 0x0AC	TIM1 timer channel 0	I bit	TIM1TIE (C0I)	No	Yes
Vector base + 0x0A8	TIM1 timer channel 1	I bit	TIM1TIE (C1I)	No	Yes
Vector base + 0x0A4	TIM1 timer channel 2	I bit	TIM1TIE (C2I)	No	Yes
Vector base + 0x0A0	TIM1 timer channel 3	I bit	TIM1TIE (C3I)	No	Yes
Vector base + 0x09C to Vector base + 0x090	Reserved				

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x02F7	PIFP	R	0	0	0	0	0	0	PIFP1	PIFP0
		W								
0x02F8	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02F9	OCPEP	R	0	0	0	0	0	0	0	OCPEP0
		W								
0x02FA	OCIEP	R	0	0	0	0	0	0	0	OCIEP0
		W								
0x02FB	OCIFP	R	0	0	0	0	0	0	0	OCIFP0
		W								
0x02FC	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02FD	RDRP	R	0	0	0	0	0	0	0	RDRP0
		W								
0x02FE–0x02FF	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0300–0x032F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0330	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0331	PTIL	R	0	0	0	0	0	PTIL2	PTIL1	PTIL0
		W								
0x0332	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0333	PTPSL	R	0	0	0	0	0	PTPSL2	PTPSL1	PTPSL0
		W								
0x0334	PPSL	R	0	0	0	0	0	PPSL2	PPSL1	PPSL0
		W								
0x0335	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0336	PIEL	R	0	0	0	0	0	PIEL2	PIEL1	PIEL0
		W								

Table 2-21. Pull Device Enable Register Field Descriptions

Field	Description
7-0 PERx7-0	**Pull Enable** — Activate pull device on input pin This bit controls whether a pull device on the associated port input or open-drain output pin is active. If a pin is used as push-pull output this bit has no effect. The polarity is selected by the related polarity select register bit. On open-drain output pins only a pullup device can be enabled. 1 Pull device enabled 0 Pull device disabled

2.3.3.5 Polarity Select Register

Address 0x0268 PPSE
0x0288 PPSADH
0x0289 PPSADL

Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PPSx7	PPSx6	PPSx5	PPSx4	PPSx3	PPSx2	PPSx1	PPSx0
Reset								
Ports E:	0	0	0	0	0	0	1	1
Others:	0	0	0	0	0	0	0	0

Figure 2-17. Polarity Select Register

1. Read: Anytime
Write: Anytime

Table 2-22. Polarity Select Register Field Descriptions

Field	Description
7-0 PPSx7-0	**Pull Polarity Select** — Configure pull device and pin interrupt edge polarity on input pin This bit selects a pullup or a pulldown device if enabled on the associated port input pin. If a port has interrupt functionality this bit also selects the polarity of the active edge. 1 Pulldown device selected; rising edge selected 0 Pullup device selected; falling edge selected

2.3.3.6 Port Interrupt Enable Register

Address 0x028C PIEADH
0x028D PIEADL
0x02F6 PIEP
0x0336 PIEL

Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PIEx7	PIEx6	PIEx5	PIEx4	PIEx3	PIEx2	PIEx1	PIEx0
Reset	0	0	0	0	0	0	0	0

Figure 2-18. Port Interrupt Enable Register

1. Please refer to the notes following the PRIOLVL[2:0] description below.

Address: 0x00001B

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PRIOLVL[2:0]		
W								
Reset	0	0	0	0	0	0	0	1(1)

= Unimplemented or Reserved

Figure 4-8. Interrupt Request Configuration Data Register 3 (INT_CFDATA3)

1. Please refer to the notes following the PRIOLVL[2:0] description below.

Address: 0x00001C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PRIOLVL[2:0]		
W								
Reset	0	0	0	0	0	0	0	1(1)

= Unimplemented or Reserved

Figure 4-9. Interrupt Request Configuration Data Register 4 (INT_CFDATA4)

1. Please refer to the notes following the PRIOLVL[2:0] description below.

Address: 0x00001D

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PRIOLVL[2:0]		
W								
Reset	0	0	0	0	0	0	0	1(1)

= Unimplemented or Reserved

Figure 4-10. Interrupt Request Configuration Data Register 5 (INT_CFDATA5)

1. Please refer to the notes following the PRIOLVL[2:0] description below.

Address: 0x00001E

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PRIOLVL[2:0]		
W								
Reset	0	0	0	0	0	0	0	1(1)

= Unimplemented or Reserved

Figure 4-11. Interrupt Request Configuration Data Register 6 (INT_CFDATA6)

1. Please refer to the notes following the PRIOLVL[2:0] description below.

6.1.4 Modes of Operation

The DBG module can be used in all MCU functional modes.

The DBG module can issue breakpoint requests to force the device to enter active BDM or an SWI ISR. The BDC BACKGROUND command is also handled by the DBG to force the device to enter active BDM. When the device enters active BDM through a BACKGROUND command with the DBG module armed, the DBG remains armed.

6.1.5 Block Diagram

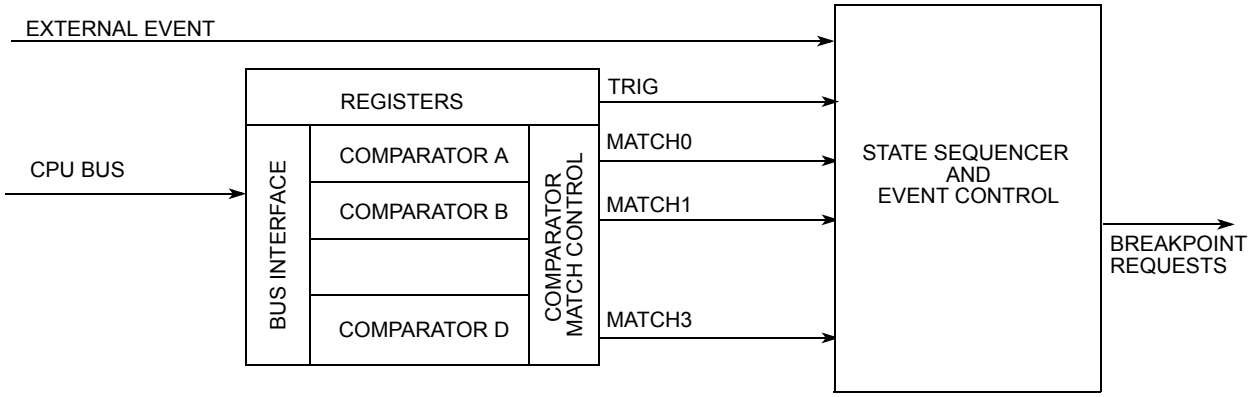

Figure 6-1. Debug Module Block Diagram

6.2 External Signal Description

6.2.1 External Event Input

The DBG module features an external event input signal, DBGEEV. The mapping of this signal to a device pin is specified in the device specific documentation. This function can be enabled and configured by the EEVE field in the DBGC1 control register. This signal is input only and allows an external event to force a state sequencer transition. With the external event function enabled, a falling edge at the external event pin constitutes an event. Rising edges have no effect. The maximum frequency of events is half the internal core bus frequency. The function is explained in the EEVE field description.

NOTE

Due to input pin synchronization circuitry, the DBG module sees external events 2 bus cycles after they occur at the pin. Thus an external event occurring less than 2 bus cycles before arming the DBG module is perceived to occur whilst the DBG is armed.

9.5.2.8 ADC Interrupt Enable Register (ADCIE)

Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	SEQAD_IE	CONIF_OIE	Reserved	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-11. ADC Interrupt Enable Register (ADCIE)

Read: Anytime

Write: Anytime

Table 9-13. ADCIE Field Descriptions

Field	Description
7 SEQAD_IE	**Conversion Sequence Abort Done Interrupt Enable Bit** — This bit enables the conversion sequence abort event done interrupt. 0 Conversion sequence abort event done interrupt disabled. 1 Conversion sequence abort event done interrupt enabled.
6 CONIF_OIE	**ADCCONIF Register Flags Overrun Interrupt Enable** — This bit enables the flag which indicates if an overrun situation occurred for one of the CON_IF[15:1] flags or for the EOL_IF flag. 0 No ADCCONIF Register Flag overrun occurred. 1 ADCCONIF Register Flag overrun occurred.

9.5.2.16 ADC Command Register 1 (ADCCMD_1)

A command which contains reserved bit settings causes the error flag CMD_EIF being set and ADC cease operation. The CMD_EIF is never set for Internal_x channels, even if the channels are specified as reserved in the Device Overview section of the Reference Manual.

Module Base + 0x0015

	23	22	21	20	19	18	17	16
R W	VRH_SEL(1)	VRL_SEL1	CH_SEL[5:0]					
R W	VRH_SEL[1:0](2)		CH_SEL[5:0]					
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-19. ADC Command Register 1 (ADCCMD_1)

1. Only available on ADC12B_LBA V1 and V2 (see Table 9-2 for details)
2. Only available on ADC12B_LBA V3 (see Table 9-2 for details)

Read: Anytime

Write: Only writable if bit SMOD_ACC is set
(see also Section 9.5.2.2, “ADC Control Register 1 (ADCCTL_1) bit SMOD_ACC description for more details)

Table 9-23. ADCCMD_1 Field Descriptions

Field	Description
	ADC12B_LBA V1 and V2 (includes VRH_SEL/VRL_SEL)
23 VRH_SEL	**Reference High Voltage Select Bit** — This bit selects the high voltage reference for current conversion. 0 VRH_0 input selected as high voltage reference. 1 VRH_1 input selected as high voltage reference.
22 VRL_SEL	**Reference Low Voltage Select Bit** — This bit selects the low voltage reference for current conversion. 0 VRL_0 input selected as low voltage reference. 1 VRL_1 input selected as low voltage reference.
	ADC12B_LBA V3 (includes VRH_SEL[1:0])
23-22 VRH_SEL	**Reference High Voltage Select Bit** — These bits select the high voltage reference for current conversion. 00 VRH_0 input selected as high voltage reference 01 VRH_1 input selected as high voltage reference 10 VRH_2 input selected as high voltage reference 11 Reserved
21-16 CH_SEL[5:0]	**ADC Input Channel Select Bits** — These bits select the input channel for the current conversion. See Table 9-24 for channel coding information.

NOTE

If bit SMOD_ACC is set modifying this register must be done carefully - only when no conversion and conversion sequence is ongoing.

11.3.2.11 Main Timer Interrupt Flag 2 (TFLG2)

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	TOF	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 11-17. Main Timer Interrupt Flag 2 (TFLG2)

TFLG2 indicates when interrupt conditions have occurred. To clear a bit in the flag register, write the bit to one while TEN bit of TSCR1 .

Read: Anytime

Write: Used in clearing mechanism (set bits cause corresponding bits to be cleared).

Any access to TCNT will clear TFLG2 register if the TFFCA bit in TSCR register is set.

Table 11-14. TRLG2 Field Descriptions

Field	Description
7 TOF	**Timer Overflow Flag** — Set when 16-bit free-running timer overflows from 0xFFFF to 0x0000. Clearing this bit requires writing a one to bit 7 of TFLG2 register while the TEN bit of TSCR1 is set to one .

buffered mode. In addition, if restart is enabled (RSTRTx=1), the commutation event generates both “PWM reload event” and “PWM reload-is-asynchronous event” simultaneously.

12.2.6 Commutation Event Edge Select Signal — async_event_edge_sel[1:0]

These device-internal PMF input signals select the active edge for the async_event input. Refer to the device overview section to determine if the selection is user configurable or tied constant at integration level.

Table 12-5. Commutation Event Edge Selection

async_event_edge-sel[1:0]	async_event active edge
00	direct input
01	rising edge
10	falling edge
11	both edges

12.2.7 PWM Reload Event Signals — pmf_reloada,b,c

These device-internal PMF output signals assert once per control cycle and can serve as triggers for other implemented IP modules. Signal pmf_reloadb and pmf_reloadc are related to time base B and C, respectively, while signal pmf_reloada is off out of reset and can be programmed for time base A, B, or C. Refer to the device overview section to determine the signal connections.

12.2.8 PWM Reload-Is-Asynchronous Signal — pmf_reload_is_async

This device-internal PMF output signal serves as a qualifier to the PMF reload event signal pmf_reloada. Whenever the async_event signal causes pmf_reloada output to assert also the pmf_reload_is_async output asserts for the same duration, except if asynchronous event and generated PWM reload event occur in the same cycle.

12.3.2.22 PMF Counter Modulo A Register (PMFMODA)

Address: Module Base + 0x0024 Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	PMFMODA														
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 12-27. PMF Counter Modulo A Register (PMFMODA)

1. Read: Anytime
   Write: Anytime. Do not write a modulus value of zero for center-aligned operation. Do not write a modulus of zero or one in edge-aligned mode.

The 15-bit unsigned value written to this register is the PWM period in PWM clock periods.

NOTE

The PWM counter modulo register is buffered. The value written does not take effect until the LDOKA bit or global load OK is set and the next PWM load cycle begins. Reading PMFMODA returns the value in the buffer. It is not necessarily the value the PWM generator A is currently using.

12.3.2.23 PMF Deadtime A Register (PMFDTMA)

Address: Module Base + 0x0026 Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	PMFDTMA											
W																
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Figure 12-28. PMF Deadtime A Register (PMFDTMA)

1. Read: Anytime
   Write: This register cannot be modified after the WP bit is set.

The 12-bit value written to this register is the number of PWM clock cycles in complementary channel operation. A reset sets the PWM deadtime register to the maximum value of 0x0FFF, selecting a deadtime of 4095 PWM clock cycles. Deadtime is affected by changes to the prescaler value. The deadtime duration is determined as follows:

$$T_{DEAD\_A} = PMFDTMA / f_{PWM\_A} = PMFDTMA \times P_A \times T_{core} \qquad \textit{Eqn. 12-1}$$

12.3.2.24 PMF Enable Control B Register (PMFENCB)

Address: Module Base + 0x0028 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	PWMENB	GLDOKB	0	0	0	RSTRTB	LDOKB	PWMRIEB
W								
Reset	0	0	0	0	0	0	0	0

Figure 12-29. PMF Enable Control B Register (PMFENCB)

Chapter 13
Programmable Trigger Unit (PTUV3)

Table 13-1. Revision History Table

Rev. No. (Item No.)	Data	Sections Affected	Substantial Change(s)
3.0	16. Jul. 2013		- removed second TG

Table 13-2. Terminology

Term	Meaning
TG	Trigger Generator
EOL	End of trigger list

13.1 Introduction

In PWM driven systems it is important to schedule the acquisition of the state variables with respect to PWM cycle.

The Programmable Trigger Unit (PTU) is intended to completely avoid CPU involvement in the time acquisitions of state variables during the control cycle that can be half, full, multiple PWM cycles.

All acquisition time values are stored inside the global memory map, basically inside the system memory; see the MMC section for the supported memory area. In such cases the pre-setting of the acquisition times needs to be completed during the previous control cycle to where the actual acquisitions are to be made.

13.1.1 Features

The PTU module includes these distinctive features:

- One 16 bit counter as time base for all trigger events
- One trigger generator(TG0)
- Up to 32 trigger events per trigger generator
- Global Load OK support, to guarantee coherent update of all control loop modules
- Trigger values stored inside the global memory map, basically inside system memory
- Software generated reload event and Trigger event generation for debugging

13.1.2 Modes of Operation

The PTU module behaves as follows in the system power modes:

1. Run mode
   All PTU features are available.

13.2.2 PTURE — PTUE Reload Event

If enabled (PTUREPE is set) this pin shows the internal reload event.

13.3 Memory Map and Register Definition

This section provides the detailed information of all registers for the PTU module.

13.3.1 Register Summary

Figure 13-2 shows the summary of all implemented registers inside the PTU module.

NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address Offset / Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 PTUE	R	0	PTUFRZ	0	0	0	0	0	TG0EN
	W								
0x0001 PTUC	R	0	0	0	0	0	0	0	PTULDOK
	W								
0x0002 PTUIEH	R	0	0	0	0	0	0	0	PTUROIE
	W								
0x0003 PTUIEL	R	0	0	0	0	TG0AEIE	TG0REIE	TG0TEIE	TG0DIE
	W								
0x0004 PTUIFH	R	0	0	0	0	0	0	PTUDEEF	PTUROIF
	W								
0x0005 PTUIFL	R	0	0	0	0	TG0AEIF	TG0REIF	TG0TEIF	TG0DIF
	W								
0x0006 TG0LIST	R	0	0	0	0	0	0	0	TG0LIST
	W								
0x0007 TG0TNUM	R	0	0	0	TG0TNUM[4:0]				
	W								
0x0008 TG0TVH	R	TG0TV[15:8]							
	W								

= Unimplemented

Figure 13-2. PTU Register Summary

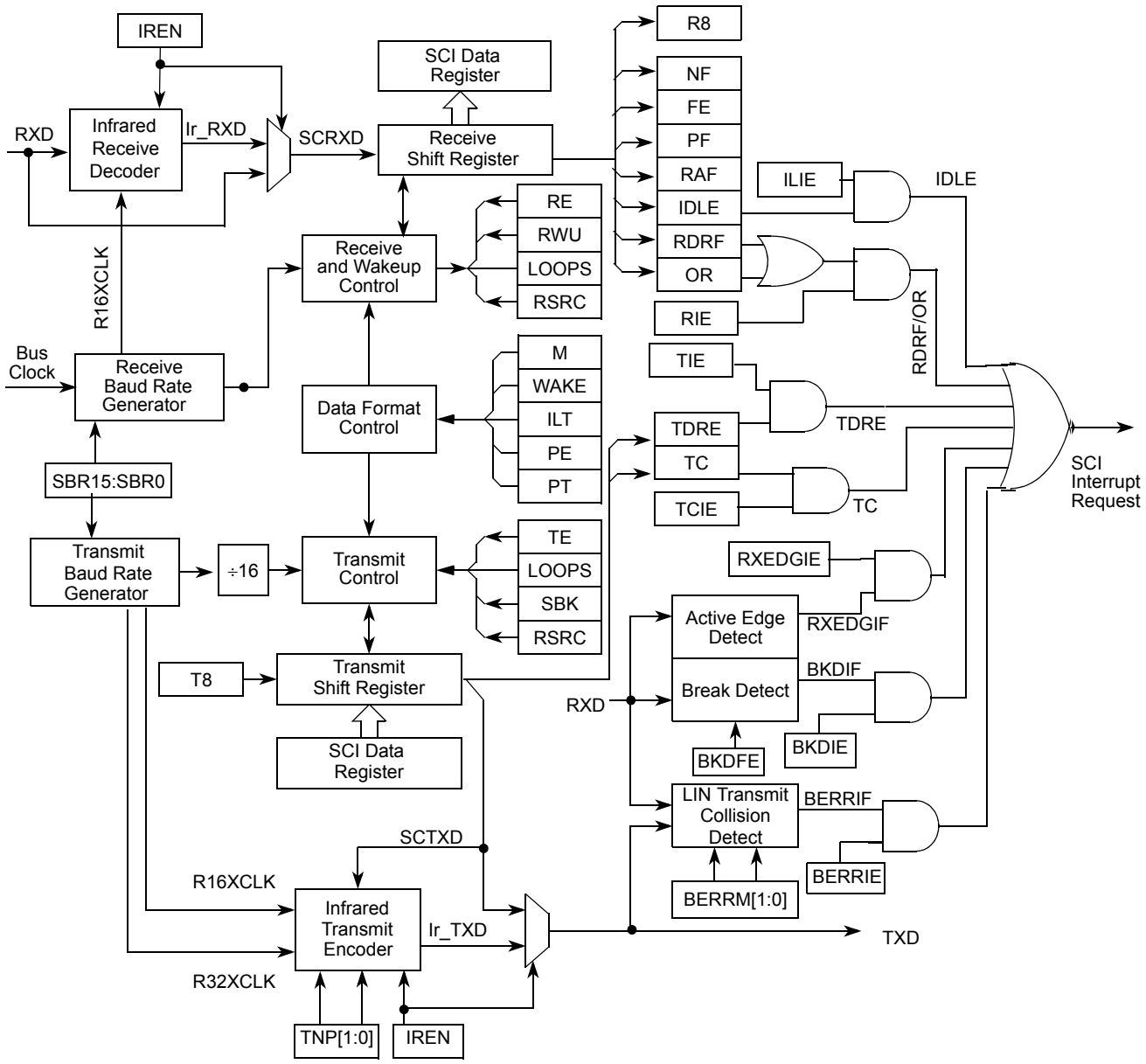

Figure 14-14. Detailed SCI Block Diagram

14.4.1 Infrared Interface Submodule

This module provides the capability of transmitting narrow pulses to an IR LED and receiving narrow pulses and transforming them to serial bits, which are sent to the SCI. The IrDA physical layer specification defines a half-duplex infrared communication link for exchange data. The full standard includes data rates up to 16 Mbits/s. This design covers only data rates between 2.4 Kbits/s and 115.2 Kbits/s.

The infrared submodule consists of two major blocks: the transmit encoder and the receive decoder. The SCI transmits serial bits of data which are encoded by the infrared submodule to transmit a narrow pulse

18.3.2.7 GDU Flag Register (GDUF)

Module Base + 0x0006 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	GSUF	GHHDF	GLVLSF	0	GOCIF0	0	GHHDIF	GLVLSIF
W								
Reset	0	0	X(2)	0	0	0	0	X(2)

= Unimplemented

Figure 18-9. GDU Flag Register (GDUF)

1. Read: Anytime
   Write: Anytime, write 1 to clear flag
2. Out of power on reset the flags may be set.

Table 18-8. GDUF Register Field Descriptions

Field	Description
7 GSUF	**GDU Start-up Flag** — The start-up flag is loaded from the flash option field after system reset deasserts. Writing a logic “1” to the bit field clears the flag. If the flag is set all high-side FET pre-drivers are turned off and all low-side FET pre-drivers are turned on. If the flag is cleared and there is no error condition present all high-side and low-side FET pre-drivers are driven by the pwm channels. 0 High-side and low-side FET pre-drivers are driven by pwm channels 1 High-side FET pre-drivers turned off and low-side FET pre-drivers are turned on
6 GHHDF	**GDU High V_{HD} Supply Flag** — The flag controls the state of the FET pre-drivers. If the flag is set and GOVA=0 the high-side pre-drivers are turned off and the low-side pre-drivers are turned on. If GOVA=1 all high-side and low-side FET pre-drivers are turned off. If the flag is cleared and no other error condition is present the high-side and low-side pre-drivers are driven by the PWM channels. The flag is set by hardware if a high voltage condition on GHD pin occurs. The flag is set if the voltage on pin GHD is greater than the threshold voltage V_{HVHDLA} or V_{HVHDHA} . Writing a logic “1” to the bit field clears the flag. 0 Voltage on pin GHD is less than V_{HVHDLD} or V_{HVHDHD} 1 Voltage on pin GHD is greater than V_{HVHDLA} or V_{HVHDHA}
5 GLVLSF	**GDU Low VLS Supply Flag** — The flag controls the state of the FET pre-drivers. If the flag is set all high-side and low-side pre-drivers are turned off. If the flag is cleared and no other error condition is present the high-side and low-side pre-drivers are driven by the PWM channels. The flag is set by hardware if a low voltage condition on VLS_OUT pin occurs. The flag is set if the voltage on pin VLS drops below the threshold voltage V_{LVLSA}. Writing a logic “1” to the bit field clears the flag. 0 VLS Supply is above V_{LVLSD} 1 VLS Supply is below $V_{LVLSA,}$ all high-side and low-side FET pre-drivers are turned off
3 GOCIF0	**GDU Overcurrent Interrupt Flag** — The interrupt flags are set by hardware if an overcurrent condition occurs. The flags are set if the voltage on the overcurrent comparator input is greater than the threshold voltage V_{OCT}. If the GOCIE bit is set an interrupt is requested. Writing a logic “1” to the bit field clears the flag. If the GOCA bit is cleared all high-side FET pre-drivers are turned off and fault[3] is asserted. If GOCA is set all high-side and low-side FET pre-drivers are turned off and fault[1:0] are asserted. 0 Voltage on overcurrent comparator input is less than V_{OCT} 1 Voltage on overcurrent comparator is greater than V_{OCT}
1 GHHDIF	**GDU High V_{HD} Supply Interrupt Flag**— The interrupt flag is set by hardware if GHHDF is set or if GHHDS is cleared. If the GHHDIE bit is set an interrupt is requested. Writing a logic “1” to the bit field clears the flag.
0 GLVLSIF	**GDU Low VLS Supply Interrupt Flag**— The interrupt flag is set by hardware if GLVLSF is set or GLVLSS is cleared. If the GLVLSIE bit is set an interrupt is requested.Writing a logic “1” to the bit field clears the flag.

To guarantee the proper read timing from the Flash array, the Flash will control (i.e. pause) the S12Z core accesses, considering that the MCU can be configured to fetch data at a faster frequency than the Flash block can support. Right after reset the Flash will be configured to run with the maximum amount of wait-states enabled; if the user application is setup to run at a slower frequency the control bits FCNFG[WSTAT] (see Section 19.3.2.5) can be configured by the user to disable the generation of wait-states, so it does not impose a performance penalty to the system if the read timing of the S12Z core is setup to be within the margins of the Flash block. For a definition of the frequency values where wait-states can be disabled please refer to the device electrical parameters.

The following sequence must be followed when the transition from a higher frequency to a lower frequency is going to happen:

- Flash resets with wait-states enabled;
- system frequency must be configured to the lower target;
- user writes to FNCNF[WSTAT] to disable wait-states;
- user reads the value of FPSTAT[WSTATACK], the new wait-state configuration will be effective when it reads as 1;
- user must re-write FCLKDIV to set a new value based on the lower frequency.

The following sequence must be followed on the contrary direction, going from a lower frequency to a higher frequency:

- user writes to FCNFG[WSTAT] to enable wait-states;
- user reads the value of FPSTAT[WSTATACK], the new wait-state configuration will be effective when it reads as 1;
- user must re-write FCLKDIV to set a new value based on the higher frequency;
- system frequency must be set to the upper target.

CAUTION

If the application is going to require the frequency setup to change, the value to be loaded on register FCLKDIV will have to be updated according to the new frequency value. In this scenario the application must take care to avoid locking the value of the FCLKDIV register: bit FDIVLCK must not be set if the value to be loaded on FDIV is going to be re-written, otherwise a reset is going to be required. Please refer to Section 19.3.2.1, “Flash Clock Divider Register (FCLKDIV) and Section 19.4.5.1, “Writing the FCLKDIV Register.

19.4.4 Internal NVM resource

IFR is an internal NVM resource readable by CPU. The IFR fields are shown in Table 19-5..

The NVM Resource Area global address map is shown in Table 19-6..

19.4.5.3 Valid Flash Module Commands

Table 19-29. present the valid Flash commands, as enabled by the combination of the functional MCU mode (Normal SingleChip NS, Special Singlechip SS) with the MCU security state (Unsecured, Secured).

Table 19-29. Flash Commands by Mode and Security State

FCMD	Command	Unsecured		Secured	
		NS (1)	SS(2)	NS (3)	SS(4)
0x01	Erase Verify All Blocks	*	*	*	*
0x02	Erase Verify Block	*	*	*	*
0x03	Erase Verify P-Flash Section	*	*	*	
0x04	Read Once	*	*	*	
0x06	Program P-Flash	*	*	*	
0x07	Program Once	*	*	*	
0x08	Erase All Blocks		*		*
0x09	Erase Flash Block	*	*	*	
0x0A	Erase P-Flash Sector	*	*	*	
0x0B	Unsecure Flash		*		*
0x0C	Verify Backdoor Access Key	*		*	
0x0D	Set User Margin Level	*	*	*	
0x0E	Set Field Margin Level		*		
0x10	Erase Verify EEPROM Section	*	*	*	
0x11	Program EEPROM	*	*	*	
0x12	Erase EEPROM Sector	*	*	*	
0x13	Protection Override	*	*	*	*

1. Unsecured Normal Single Chip mode
2. Unsecured Special Single Chip mode.
3. Secured Normal Single Chip mode.
4. Secured Special Single Chip mode.

4.). The Verify Backdoor Access Key command must not be executed from the Flash block containing the backdoor comparison key to avoid code runaway.

Table 19-54. Verify Backdoor Access Key Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0C	Not required
FCCOB1	Key 0	
FCCOB2	Key 1	
FCCOB3	Key 2	
FCCOB4	Key 3	

Upon clearing CCIF to launch the Verify Backdoor Access Key command, the Memory Controller will check the FSEC KEYEN bits to verify that this command is enabled. If not enabled, the Memory Controller sets the ACCERR bit in the FSTAT register and terminates. If the command is enabled, the Memory Controller compares the key provided in FCCOB to the backdoor comparison key in the Flash configuration field with Key 0 compared to 0xFF_FE00, etc. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the Verify Backdoor Access Key command are aborted (set ACCERR) until a reset occurs. The CCIF flag is set after the Verify Backdoor Access Key operation has completed.

Table 19-55. Verify Backdoor Access Key Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 100 at command launch
		Set if an incorrect backdoor key is supplied
		Set if backdoor key access has not been enabled (KEYEN[1:0] != 10, see Section 19.3.2.2)
		Set if the backdoor key has mismatched since the last reset
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

19.4.7.12 Set User Margin Level Command

The Set User Margin Level command causes the Memory Controller to set the margin level for future read operations of the P-Flash or EEPROM block.

Table 19-56. Set User Margin Level Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0D	Global address [23:16] to identify Flash block
FCCOB1	Global address [15:0] to identify Flash block	
FCCOB2	Margin level setting.	

Table 19-59. Set Field Margin Level Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0E	Global address [23:16] to identify Flash block
FCCOB1	Global address [15:0] to identify Flash block	
FCCOB2	Margin level setting.	

Upon clearing CCIF to launch the Set Field Margin Level command, the Memory Controller will set the field margin level for the targeted block and then set the CCIF flag.

NOTE

When the EEPROM block is targeted, the EEPROM field margin levels are applied only to the EEPROM reads. However, when the P-Flash block is targeted, the P-Flash field margin levels are applied to both P-Flash and EEPROM reads. It is not possible to apply field margin levels to the P-Flash block only.

Valid margin level settings for the Set Field Margin Level command are defined in Table 19-60.

Table 19-60. Valid Set Field Margin Level Settings

FCCOB2	Level Description
0x0000	Return to Normal Level
0x0001	User Margin-1 Level(1)
0x0002	User Margin-0 Level(2)
0x0003	Field Margin-1 Level[1]
0x0004	Field Margin-0 Level[2]

1. Read margin to the erased state
2. Read margin to the programmed state

Table 19-61. Set Field Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 19-29)
		Set if an invalid global address [23:0] is supplied see Table 19-3)
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None