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Applications of "Embedded - Microcontrollers"

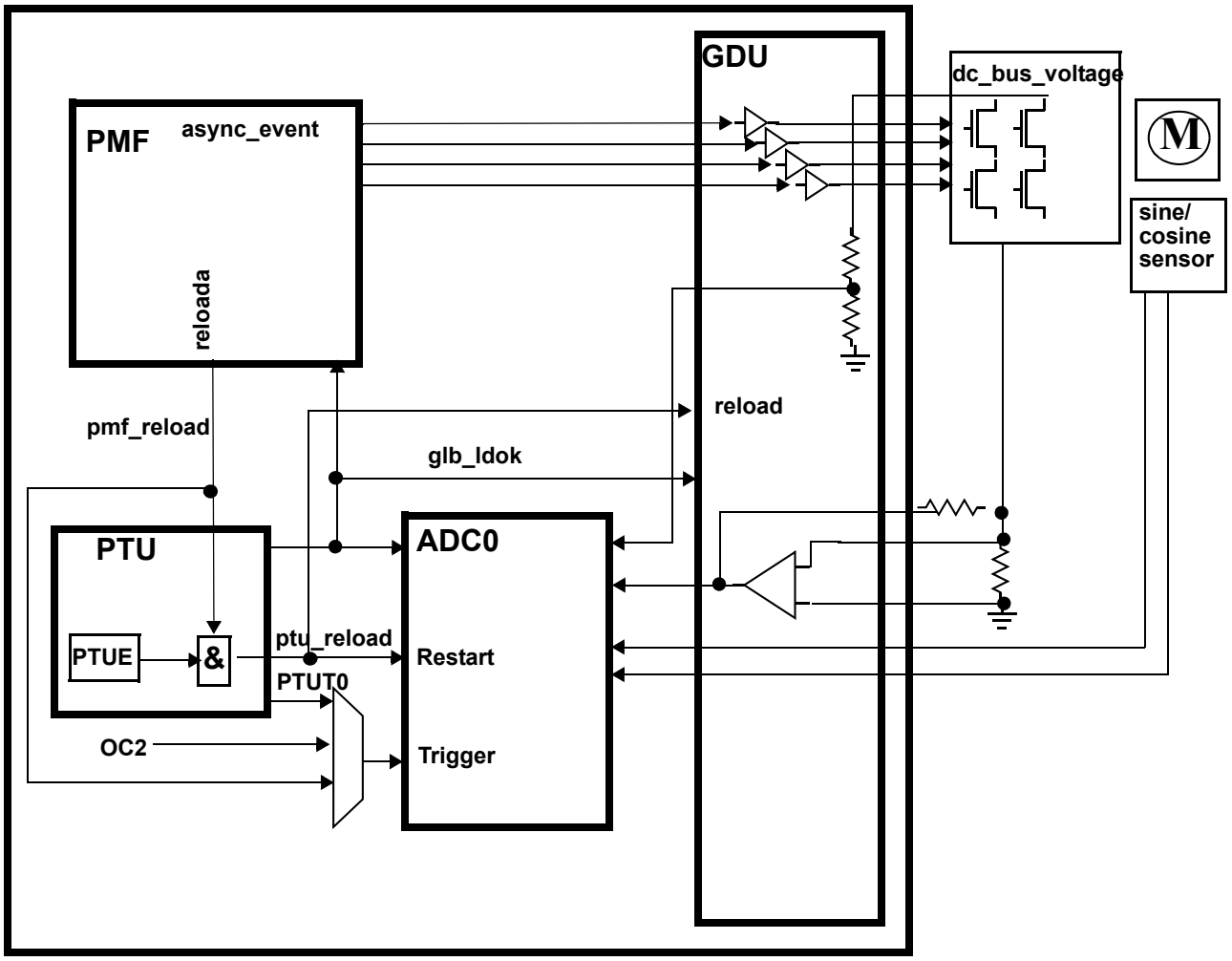
Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmba4f0vlh

Table 1-10. Control loop interface connectivity

Device Level Event	PMF	PTU	ADC0	GDU
trigger_0		PTUT0	Trigger (MUX Option)	

1. PMF events reloadb and reloadc are not connected at device level

Figure 1-5. Motor control module interfaces



1.8.6 BDC clock source connectivity

The BDC clock, BDCCLK, is mapped to the IRCCLK generated in the CPMU module.

The BDC clock, BDCFCLK is mapped to the device bus clock, generated in the CPMU module.

Chapter 2
Port Integration Module (S12ZVMBPIMV3)

Table 2-1. Revision History

Rev. No. (Item No.)	Date (Submitted By)	Sections Affected	Substantial Change(s)
V03.00	19 Jun 2015		• Initial release for S12ZVMB-family
V03.01	7 Jul 2015		• Incorporated feedback from review
V03.02	14 Jul 2015	2.3.2.6/2-87	• Added TIM1 IC0 routing option
V03.03	22 Jul 2015		• Typos and formatting
V03.04	24 Jul 2015	2.3.2.5/2-86	• Changed write restrictions of MODRR4 register • Typos and formatting
V03.05	30 Jul 2015		• Typos and formatting
V03.06	5 Aug 2015	2.1.1/2-68 2.2/2-71 2.3.1/2-77 2.3.2.6/2-87	• Added PT7 • Typos and formatting
V03.06	5 Aug 2015	2.1.1/2-68 2.2/2-71 2.3.1/2-77 2.3.2.6/2-87	• Added PT7 • Typos and formatting
V03.07	13 Aug 2015	Table 2-4 Table 2-44	• Typos and formatting
V03.08	28 Aug 2015	2.1.1/2-68 2.3.1/2-77 2.3.2.1/2-83Table 2-5 Table 2-6	• Changed SPI0 (SCLK) routing
V03.09	1 Sep 2015	2.3.4.5/2-99 Table 2-45	• Corrections

2.3.4.11 Port L Polarity Select Register (PPSL)

Address 0x0334 PPSL — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PPSL2	PPSL1	PPSL0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-33. Port L Polarity Select Register (PPSL)

1. Read: Anytime
   Write: Anytime

Table 2-37. PPSL Register Field Descriptions

Field	Description
2-0 PPSL2-0	**Polarity Select** — This bit selects the polarity of the active interrupt edge on the associated HVI pin. 1 Rising edge selected 0 Falling edge selected

2.3.4.12 Port L ADC Bypass Register (PTABYPL)

Address 0x033A — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PTABYPL2	PTABYPL1	PTABYPL0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-34. Port L ADC Bypass Register (PTBYPL)

1. Read: Anytime
   Write: Anytime

Table 2-38. PTABYPL Register Field Descriptions

Field	Description
2-0 PTABYPL 2-0	**Port L ADC Connection Bypass** — This bit bypasses and powers down the impedance converter stage in the signal path from the analog input pin to the ADC channel input. This bit takes effect only if using direct input connection to the ADC channel (PTADIRL=1). 1 Impedance converter bypassed 0 Impedance converter used

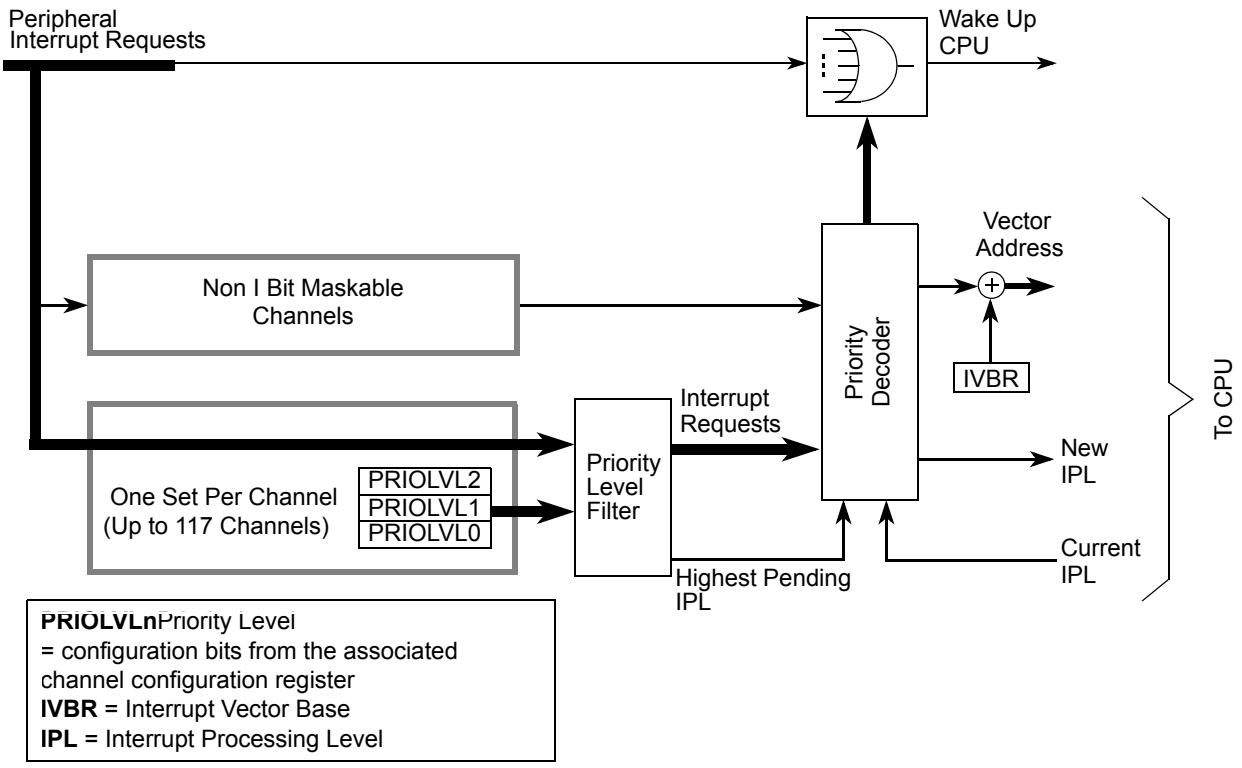


Figure 4-1. INT Block Diagram

4.2 External Signal Description

The INT module has no external signals.

4.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the INT module.

4.3.1 Module Memory Map

Table 4-3 gives an overview over all INT module registers.

Table 4-3. INT Memory Map

Address	Use	Access
0x000010–0x000011	Interrupt Vector Base Register (IVBR)	R/W
0x000012–0x000016	RESERVED	—
0x000017	Interrupt Request Configuration Address Register (INT_CFADDR)	R/W
0x000018	Interrupt Request Configuration Data Register 0 (INT_CFDATA0)	R/W

the BDCCSRL status byte is returned before the read data. This status byte reflects the state after the memory read was performed. If enabled, an ACK pulse is driven before the data bytes are transmitted. The effect of the access size and alignment on the next address to be accessed is explained in more detail in Section 5.4.5.2, “BDC Access Of Device Memory Mapped Resources”.

NOTE

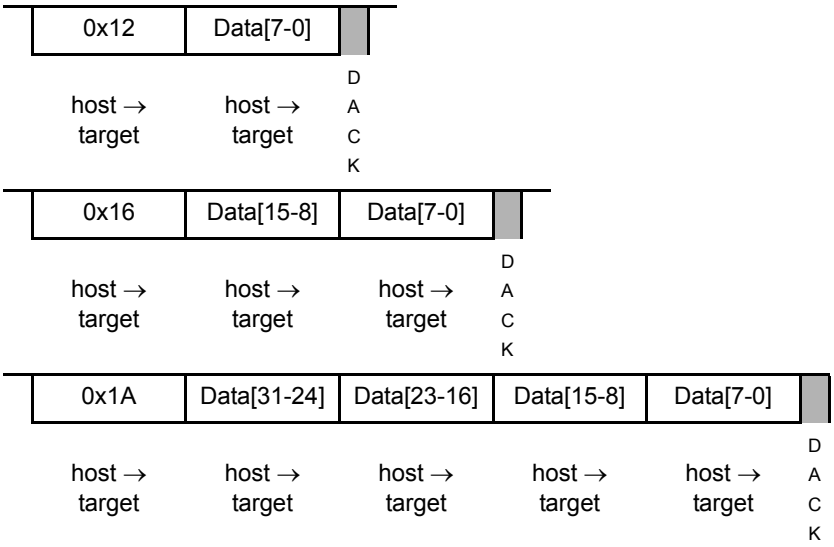
DUMP_MEM{_WS} is a valid command only when preceded by SYNC, NOP, READ_MEM{_WS}, or another DUMP_MEM{_WS} command. Otherwise, an illegal command response is returned, setting the ILLCMD bit. NOP can be used for inter-command padding without corrupting the address pointer.

The size field (sz) is examined each time a DUMP_MEM{_WS} command is processed, allowing the operand size to be dynamically altered. The examples show the DUMP_MEM.B{_WS}, DUMP_MEM.W{_WS} and DUMP_MEM.L{_WS} commands.

5.4.4.6 FILL_MEM.sz, FILL_MEM.sz_WS

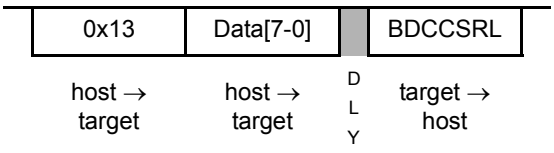
FILL_MEM.sz

Write memory specified by debug address register, then increment address **Non-intrusive**



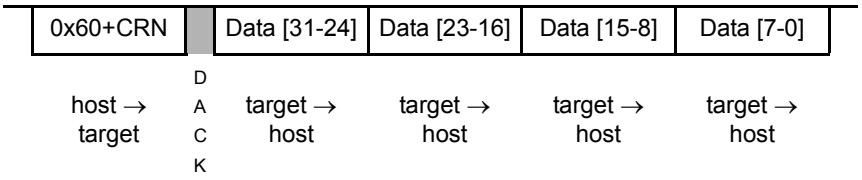
FILL_MEM.sz_WS

Write memory specified by debug address register with status, then increment address **Non-intrusive**



5.4.4.10 READ_Rn

Read CPU register **Active Background**



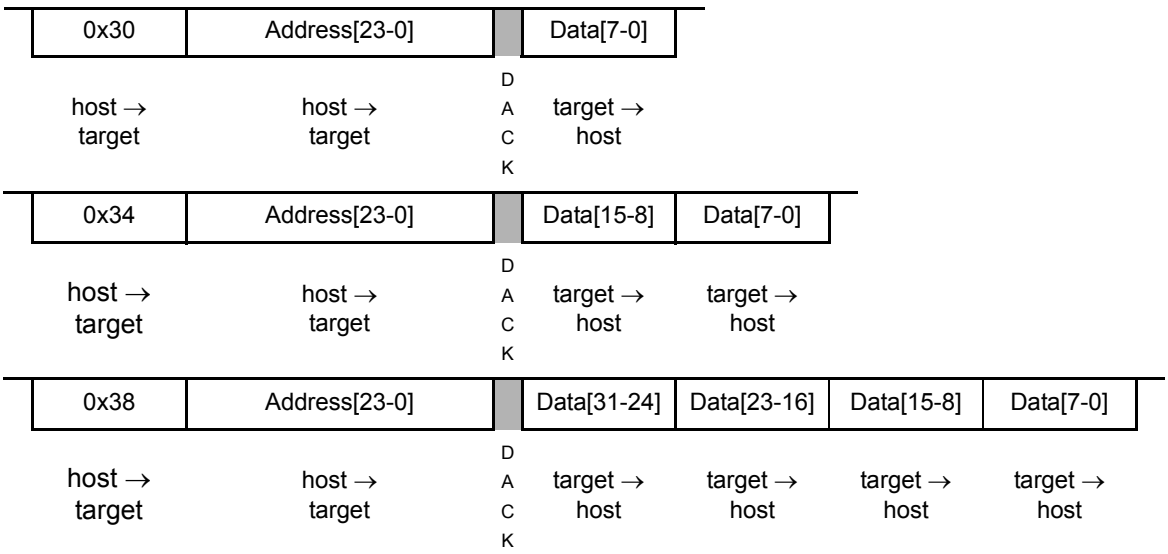
This command reads the selected CPU registers and returns the 32-bit result. Accesses to CPU registers are always 32-bits wide, regardless of implemented register width. Bytes that are not implemented return zero. The register is addressed through the CPU register number (CRN). See Section 5.4.5.1, “BDC Access Of CPU Registers for the CRN address decoding. If enabled, an ACK pulse is driven before the data bytes are transmitted.

If the device is not in active BDM, this command is illegal, the ILLCMD bit is set and no access is performed.

5.4.4.11 READ_MEM.sz, READ_MEM.sz_WS

READ_MEM.sz

Read memory at the specified address **Non-intrusive**



Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0140	DBGDCTL	R	0	0	INST	0	RW	RWE	reserved	COMPE
		W								
0x0141-0x0144	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0145	DBGDAH	R	DBGDA[23:16]							
		W								
0x0146	DBGDAM	R	DBGDA[15:8]							
		W								
0x0147	DBGDAL	R	DBGDA[7:0]							
		W								
0x0148-0x017F	Reserved	R	0	0	0	0	0	0	0	0
		W								

Figure 6-2. Quick Reference to DBG Registers

6.3.2 Register Descriptions

This section consists of the DBG register descriptions in address order. When ARM is set in DBGC1, the only bits in the DBG module registers that can be written are ARM, and TRIG

6.3.2.1 Debug Control Register 1 (DBGC1)

Address: 0x0100

	7	6	5	4	3	2	1	0
0x0100	ARM	0 TRIG	reserved	BDMBP	BRKCPU	reserved	EEVE1	0
Reset	0	0	0	0	0	0	0	0

Figure 6-3. Debug Control Register (DBGC1)

Read: Anytime

Write: Bit 7 Anytime . An ongoing profiling session must be finished before DBG can be armed again.
Bit 6 can be written anytime but always reads back as 0.
Bits 5:0 anytime DBG is not armed.

NOTE

On a write access to DBGC1 and simultaneous hardware disarm from an internal event, the hardware disarm has highest priority, clearing the ARM bit and generating a breakpoint, if enabled.

9.5 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the ADC12B_LBA.

9.5.1 Module Memory Map

Figure 9-3 gives an overview of all ADC12B_LBA registers.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	ADCCTL_0	R	ADC_EN	ADC_SR	FRZ_MOD	SWAI	ACC_CFG[1:0]		STR_SEQA	MOD_CFG
		W								
0x0001	ADCCTL_1	R	CSL_BMOD	RVL_BMOD	SMOD_ACC	AUT_RSTA	0	0	0	0
		W								
0x0002	ADCSTS	R	CSL_SEL	RVL_SEL	DBECC_ERR	Reserved	READY	0	0	0
		W								
0x0003	ADCTIM	R	0	PRS[6:0]						
		W								
0x0004	ADCFMT	R	DJM	0	0	0	0	SRES[2:0]		
		W								
0x0005	ADCFLWCTL	R	SEQA	TRIG	RSTA	LDOK	0	0	0	0
		W								
0x0006	ADCEIE	R	IA_EIE	CMD_EIE	EOL_EIE	Reserved	TRIG_EIE	RSTAR_EIE	LDOK_EIE	0
		W								
0x0007	ADCIE	R	SEQAD_IE	CONIF_OIE	Reserved	0	0	0	0	0
		W								
0x0008	ADCEiF	R	IA_EIF	CMD_EIF	EOL_EIF	Reserved	TRIG_EIF	RSTAR_EIF	LDOK_EIF	0
		W								
0x0009	ADCIF	R	SEQAD_IF	CONIF_OIF	Reserved	0	0	0	0	0
		W								
0x000A	ADCCONIE_0	R	CON_IE[15:8]							
		W								
0x000B	ADCCONIE_1	R	CON_IE[7:1]							EOL_IE
		W								
0x000C	ADCCONIF_0	R	CON_IF[15:8]							
		W								
0x000D	ADCCONIF_1	R	CON_IF[7:1]							EOL_IF
		W								
0x000E	ADCIMDRI_0	R	CSL_IMD	RVL_IMD	0	0	0	0	0	0
		W								
0x000F	ADCIMDRI_1	R	0	0	RIDX_IMD[5:0]					
		W								

= Unimplemented or Reserved

Figure 9-3. ADC12B_LBA Register Summary (Sheet 1 of 3)

If measured when

a) V_{HBI1} selected with BVHS = 0
$V_{measure} \geq V_{HBI1\_A}$ (rising edge) or $V_{measure} \geq V_{HBI1\_D}$ (falling edge)

or when

a) V_{HBI2} selected with BVHS = 1
$V_{measure} \geq V_{HBI2\_A}$ (rising edge) or $V_{measure} \geq V_{HBI2\_D}$ (falling edge)

then BVHC is set. BVHC status bit indicates that a high voltage at pin VSUP is present. The High Voltage Interrupt flag (BVHIF) is set to 1 when a Voltage High Condition (BVHC) changes state. The Interrupt flag BVHIF can only be cleared by writing a 1. If the interrupt is enabled by bit BVHIE the module requests an interrupt to MCU (BATI).

11.3.2.11 Main Timer Interrupt Flag 2 (TFLG2)

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	TOF	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 11-17. Main Timer Interrupt Flag 2 (TFLG2)

TFLG2 indicates when interrupt conditions have occurred. To clear a bit in the flag register, write the bit to one while TEN bit of TSCR1 .

Read: Anytime

Write: Used in clearing mechanism (set bits cause corresponding bits to be cleared).

Any access to TCNT will clear TFLG2 register if the TFFCA bit in TSCR register is set.

Table 11-14. TRLG2 Field Descriptions

Field	Description
7 TOF	**Timer Overflow Flag** — Set when 16-bit free-running timer overflows from 0xFFFF to 0x0000. Clearing this bit requires writing a one to bit 7 of TFLG2 register while the TEN bit of TSCR1 is set to one .

13.3.2.5 PTU Interrupt Flag Register High (PTUIFH)

Module Base + 0x0004 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PTUDEEF	PTUROIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-7. PTU Interrupt Flag Register High (PTUIFH)

1. Read: Anytime
   Write: Anytime, write 1 to clear

Table 13-7. PTUIFH Register Field Descriptions

Field	Description
1 PTUDEEF	PTU Double bit ECC Error Flag — This bit is set if the read data from the memory contains double bit ECC errors. While this bit is set the trigger generation of both trigger generators stops. 0 No double bit ECC error occurs 1 Double bit ECC error occurs
0 PTUROIF	PTU Reload Overrun Interrupt Flag — If reload event occurs when the PTULDOK bit is not set then this bit will be set. This bit is not set if the reload event was forced by an asynchronous commutation event. 0 No reload overrun occurs 1 Reload overrun occurs

13.3.2.6 PTU Interrupt Flag Register Low (PTUIFL)

Module Base + 0x0005 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	TG0AEIF	TG0REIF	TG0EIF	TG0DIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-8. PTU Interrupt Flag Register Low (PTUIFL)

1. Read: Anytime
   Write: Anytime, write 1 to clear

The WAKE bit in SCI control register 1 (SCICR1) determines how the SCI is brought out of the standby state to process an incoming message. The WAKE bit enables either idle line wakeup or address mark wakeup.

14.4.6.6.1 Idle Input line Wakeup (WAKE = 0)

In this wakeup method, an idle condition on the RXD pin clears the RWU bit and wakes up the SCI. The initial frame or frames of every message contain addressing information. All receivers evaluate the addressing information, and receivers for which the message is addressed process the frames that follow. Any receiver for which a message is not addressed can set its RWU bit and return to the standby state. The RWU bit remains set and the receiver remains on standby until another idle character appears on the RXD pin.

Idle line wakeup requires that messages be separated by at least one idle character and that no message contains idle characters.

The idle character that wakes a receiver does not set the receiver idle bit, IDLE, or the receive data register full flag, RDRF.

The idle line type bit, ILT, determines whether the receiver begins counting logic 1s as idle character bits after the start bit or after the stop bit. ILT is in SCI control register 1 (SCICR1).

14.4.6.6.2 Address Mark Wakeup (WAKE = 1)

In this wakeup method, a logic 1 in the most significant bit (MSB) position of a frame clears the RWU bit and wakes up the SCI. The logic 1 in the MSB position marks a frame as an address frame that contains addressing information. All receivers evaluate the addressing information, and the receivers for which the message is addressed process the frames that follow.Any receiver for which a message is not addressed can set its RWU bit and return to the standby state. The RWU bit remains set and the receiver remains on standby until another address frame appears on the RXD pin.

The logic 1 MSB of an address frame clears the receiver's RWU bit before the stop bit is received and sets the RDRF flag.

Address mark wakeup allows messages to contain idle characters but requires that the MSB be reserved for use in address frames.

NOTE

With the WAKE bit clear, setting the RWU bit after the RXD pin has been idle can cause the receiver to wake up immediately.

14.4.7 Single-Wire Operation

Normally, the SCI uses two pins for transmitting and receiving. In single-wire operation, the RXD pin is disconnected from the SCI. The SCI uses the TXD pin for both receiving and transmitting.

16.3.6 Reserved Register

Module Base + 0x0003 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

= Unimplemented

Figure 16-5. Reserved Register

1. Read: Anytime
   Write: Only in special mode

NOTE

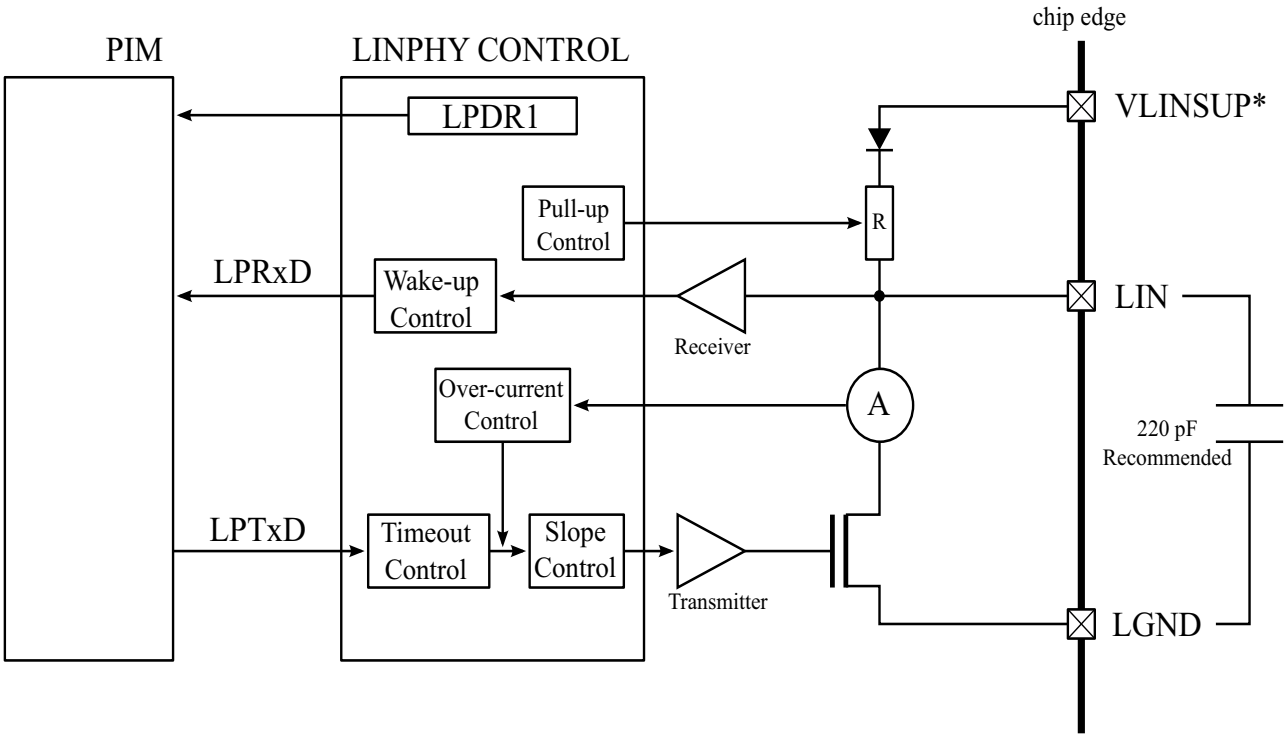
This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special mode can alter the module's functionality.

Table 16-7. Reserved Register Field Descriptions

Field	Description
7-0 Reserved	These reserved bits are used for test purposes. Writing to these bits can alter the module functionality.

17.1.3 Block Diagram

Figure 17-1 shows the block diagram of the LIN Physical Layer. The module consists of a receiver with wake-up control, a transmitter with slope and timeout control, a current sensor with overcurrent protection as well as a registers control block.



*The VLINSUP supply mapping is described in device level documentation

Figure 17-1. LIN Physical Layer Block Diagram

NOTE

The external 220 pF capacitance between LIN and LGND is strongly recommended for correct operation.

17.2 External Signal Description

This section lists and describes the signals that connect off chip as well as internal supply nodes and special signals.

NOTE

FET pre-driver concept shown in Figure 18-24 for the high-side driver applies also to low-side driver. The reference current for the low-side driver is controlled by GSRCLS[2:0].

18.5.2 GDU Intrinsic Dead Time

The basic point of dead time is to prevent cross conduction of the high-side and low-side power MOSFETs.

The GDU adds an amount of dead time to the PWM signals driving the high-side and low-side power MOSFETs. A PWM signal applied to the input of the GDU does not appear instantly on the output. There is propagation delay (t_{delon}, t_{deloff}) through the FET pre-drivers and it takes time to turn on and off the gates of the power MOSFETs (t_{HGON}, t_{HGOFF}) (see Figure 18-25). The propagation delay and the turn on and off time change over temperature. There are differences between propagation delay paths to the high-side MOSFETs and low-side MOSFETs. Worst case must be considered. The turn on time t_{HGON} depends also on the setting of the slew rate control bits GSRCLS[2:0] and GSRCHS[2:0].

Figure 18-25. Driver on/off Delay and on/off Time[1]

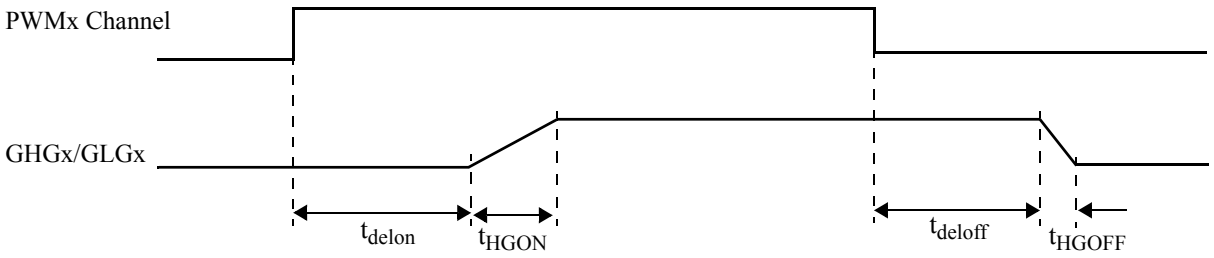
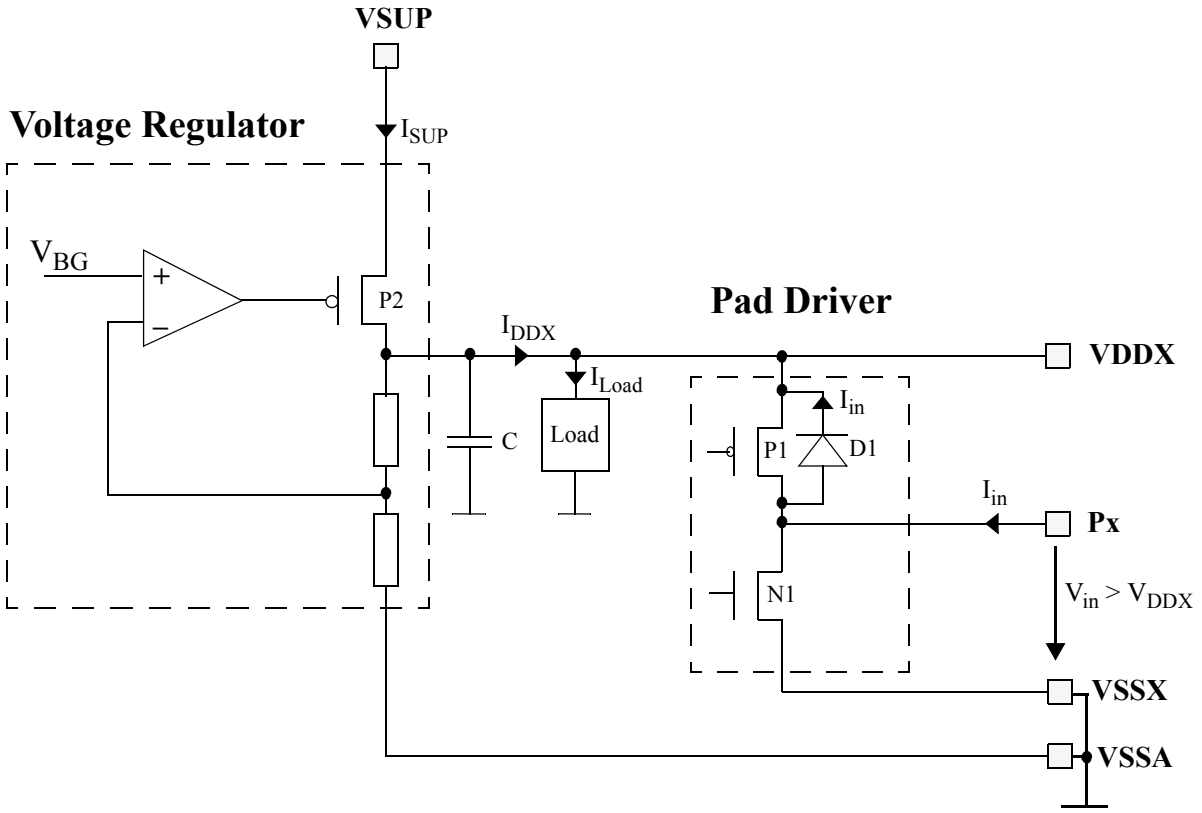


Figure 18-26 shows examples of intrinsic dead times. For example assuming minimum values for t_{HGON} and t_{delon} for the high side gate HG0 and minimum values for t_{HGOFF} and t_{deloff} for low-side gate LG0 no additional dead time setting in the PMF module is required and the PWM channels can change at the same time without cross conduction of the power MOSFETs.

1. Note that t_{HGON} and t_{HGOFF} is the turn on and turn off time for high-side and low-side gate

power; e.g., if the device is in STOP mode with no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

Figure A-1. Current injection on GPIO port if $V_{in} > V_{DDX}$



A.1.4 Absolute maximum ratings

Absolute maximum ratings are stress ratings only. A functional operation outside these ranges is not guaranteed. Stress beyond these limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level.

Table A-2. Absolute maximum ratings

Num	Rating	Symbol	Min	Max	Unit
1	Voltage regulator supply voltage	V_{SUP}	-0.3	42	V
2	High side driver supply voltage	V_{SUPHS}	-0.3	42	V
3	DC voltage on LIN	V_{LIN}	-32	42	V
4	FET-Predriver High-Side Drain	V_{GHD}	-0.3	42	V
5	FET-Predriver Bootstrap Capacitor Connection	V_{VBS}	-0.3	42	V

Table A-10. VDDA, VDDX Domain I/O Characteristics (Junction Temperature From –40°C To +175°C)

(1)Conditions are 4.5 V < V_{DDX}< 5.5 V , unless otherwise noted. Characteristics for all GPIO pins (defined in A.1.2.1/A-670).						
19	Input capacitance	C_{in}	—	7	—	pF
20	Injection current(3) Single pin limit Total device limit, sum of all injected currents	 I_{ICS} I_{ICP}	 –2.5 –25	—	 2.5 25	mA

1. Values are characterized in the range 4.5V < V_{DDA}, V_{DDX}< 5.5V. Production test uses 4.85V < V_{DDA}, V_{DDX}< 5.15V.

2. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8°C to 12°C in the temperature range from 50°C to 125°C.

3. Refer to Section A.1.3, “Current injection” for more details

Table A-11. Pin Timing Characteristics (Junction Temperature From –40°C To +175°C)

Conditions are 4.5 V < V_{DDX}< 5.5 V unless otherwise noted. I/O Characteristics for all GPIO pins (defined in A.1.2.1/A-670).						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Port P, AD interrupt input pulse filtered (STOP)(1)	t_{P_MASK}	—	—	3	µs
2	Port P, AD interrupt input pulse passed (STOP)1	t_{P_PASS}	10	—	—	µs
3	Port P, AD interrupt input pulse filtered ($\overline{\text{STOP}}$) in number of bus clock cycles of period 1/f_{bus}	n_{P_MASK}	—	—	3	—
4	Port P, AD interrupt input pulse passed ($\overline{\text{STOP}}$) in number of bus clock cycles of period 1/f_{bus}	n_{P_PASS}	4	—	—	—
5	$\overline{\text{IRQ}}$ pulse width, edge-sensitive mode ($\overline{\text{STOP}}$) in number of bus clock cycles of period 1/f_{bus}	n_{IRQ}	1	—	—	—
6	$\overline{\text{RESET}}$ pin input pulse filtered	R_{P_MASK}	—	—	12	ns
7	$\overline{\text{RESET}}$ pin input pulse passed	R_{P_PASS}	22	—	—	ns

1. Parameter only applies in stop or pseudo stop mode.

Appendix I
SPI Electrical Specifications

This section provides electrical parametrics and ratings for the SPI.

In **Figure I-1.** the measurement conditions are listed.

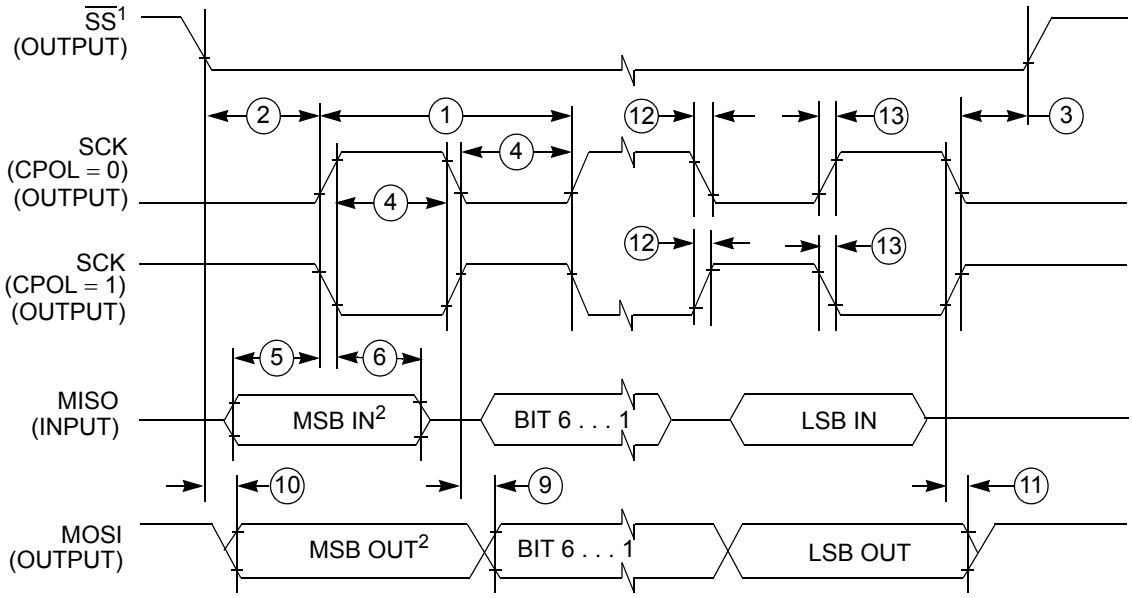
Figure I-1. Measurement Conditions

Description	Value	Unit
Drive mode	full drive mode	—
Load capacitance C_{LOAD}[(1)], on all outputs	50	pF
Thresholds for delay measurement points	(35% / 65%) VDDX	V

1. Timing specified for equal load on all SPI output pins. Avoid asymmetric load.

I.1 Master Mode

In **Figure I-2.** the timing diagram for master mode with transmission format CPHA=0 is depicted.



1. If enabled.
2. LSBFE = 0. For LSBFE = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure I-2. SPI Master Timing (CPHA=0)

In **Figure I-3.** the timing diagram for master mode with transmission format CPHA=1 is depicted.

L.6 0x0380-0x039F FTMRZ

Address	Name		7	6	5	4	3	2	1	0
0x0386	FSTAT	R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT1	MGSTAT0
		W								
0x0387	FERSTAT	R	0	0	0	0	0	0	DFDF	SFDIF
		W								
0x0388	FPROT	R	FPOPEN	RNV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
		W								
0x0389	DFPROT	R	DPOPEN	0	DPS5	DPS4	DPS3	DPS2	DPS1	DPS0
		W								
0x038A	FOPT	R	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0
		W								
0x038B	FRSV1	R	0	0	0	0	0	0	0	0
		W								
0x038C	FCCOB0HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								
0x038D	FCCOB0LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
		W								
0x038E	FCCOB1HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								
0x038F	FCCOB1LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
		W								
0x0390	FCCOB2HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								
0x0391	FCCOB2LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
		W								
0x0392	FCCOB3HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								
0x0393	FCCOB3LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
		W								
0x0394	FCCOB4HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								
0x0395	FCCOB4LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
		W								
0x0396	FCCOB5HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								