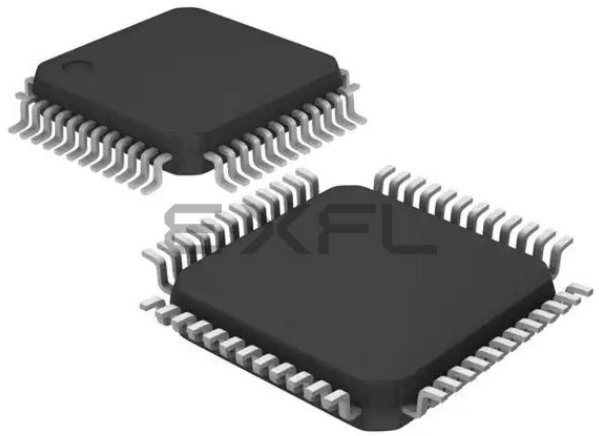

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	15
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmba6f0mlf

1.6 Device memory map

Table 1-3 shows the device register memory map. All modules that can be instantiated more than once on S12 devices are listed with an index number, even if they are only instantiated once on this device family.

Table 1-3. Module register address ranges

Address	Module	Size (Bytes)
0x0000–0x0003	Part ID Register Section 1.6.1	4
0x0004–0x000F	Reserved	12
0x0010–0x001F	INT	16
0x0020–0x006F	Reserved	80
0x0070–0x008F	MMC	32
0x0090–0x00FF	MMC Reserved	112
0x0100–0x017F	DBG	128
0x0180–0x01FF	Reserved	128
0x0200–0x037F	PIM	384
0x0380–0x039F	FTMRZ	32
0x03A0–0x03BF	Reserved	32
0x03C0–0x03CF	SRAM ECC	16
0x03D0–0x03FF	Reserved	48
0x0400–0x042F	TIM1	48
0x0430–0x043F	Reserved	16
0x0440–0x04FF	Reserved	192
0x0500–0x053F	PMF	64
0x0540–0x057F	Reserved	64
0x0580–0x059F	PTU	32
0x05A0–0x05BF	Reserved	32
0x05C0–0x05EF	TIM0	48
0x05F0–0x05FF	Reserved	16
0x0600–0x063F	ADC0	64
0x0640–0x067F	Reserved	64
0x0680–0x069F	Reserved	32
0x06A0–0x06BF	GDU	32
0x06C0–0x06DF	CPMU	32
0x06E0–0x06EF	Reserved	16
0x06F0–0x06F7	BATS	8
0x06F8–0x06FF	Reserved	8
0x0700–0x0707	SCI0	8

1.6.1 Part ID assignments

The part ID is located in four 8-bit registers at addresses 0x0000-0x0003. The read-only value is a unique part ID for each revision of the chip. Table 1-5 shows the assigned part ID number and mask set number.

Table 1-5. Assigned part ID numbers

Device	Mask Set Number	Part ID
MC9S12ZVMB64	N17S	0x06160000

1.7 Signal description and device pinouts

This section describes signals that connect off-chip. It includes pin out diagrams, a table of signal properties, and detailed discussion of signals. Internal inter module signal mapping at device level is described in 1.8 Internal signal mapping.

1.7.1 Pin assignment overview

Table 1-6 provides a summary of which ports are available.

Table 1-6. Port availability by package option

Port	64 LQFP	48 LQFP
Port AD	PAD[8:0]	PAD[4:0]
Port E	PE[1:0]	PE[1:0]
Port L (HVI)	PL[2:0]	PL[2:0]
Port P	PP[1:0]	PP[1:0]
Port T	PT[7:0]	PT[2:0]
sum of ports	24	15

NOTE

To avoid current drawn from floating inputs, all non-bonded pins should be configured as output or configured as input with a pull up or pull down device enabled

1.7.2 Detailed external signal descriptions

This section describes the properties of signals available at device pins. Signal names associated with modules that can be instantiated more than once are indexed, even if the module is only instantiated once. If a signal already includes a channel number, then the index is inserted before the channel number. Thus TIMx_y corresponds to TIM instance x, channel number y.

Table 1-12. Security bits

SEC[1:0]	Security State
00	1 (secured)
01	1 (secured)
10	0 (unsecured)
11	1 (secured)

NOTE

Please refer to the flash block description for more security byte details.

1.10.3 Operation of the secured microcontroller

By securing the device, unauthorized access to the EEPROM and Flash memory contents is prevented. Secured operation has the following effects on the microcontroller:

1.10.3.1 Normal single chip mode (NS)

- .Background debug controller (BDC) operation is completely disabled
- Execution of flash and EEPROM commands is restricted (described in flash block description).

1.10.3.2 Special single chip mode (SS)

- Background debug controller (BDC) commands are restricted
- Execution of flash and EEPROM commands is restricted (described in flash block description).

In special single chip mode the device is in active BDM after reset. In special single chip mode on a secure device, only the BDC mass erase and BDC control and status register commands are possible. BDC access to memory mapped resources is disabled. The BDC can only be used to erase the EEPROM and flash memory without giving access to their contents.

1.10.4 Unsecuring the microcontroller

Unsecuring the microcontroller can be done using three different methods:

1. Back-door key access
2. Reprogramming the security bits
3. Complete memory erase

1.10.4.1 Unsecuring the MCU using the back-door key access

In normal single chip mode, security can be temporarily disabled using the back-door key access method. This method requires that:

- The back-door key has been programmed to a valid value
- The KEYEN[1:0] bits within the flash options/security byte select ‘enabled’.

- The application program programmed into the microcontroller has the capability to write to the back-door key locations

The back-door key values themselves should not normally be stored within the application data, which means the application program would have to be designed to receive the back-door key values from an external source (e.g. through a serial port).

The back-door key access method allows debugging of a secured microcontroller without having to erase the flash. This is particularly useful for failure analysis.

NOTE

No back-door key word is allowed to have the value 0x0000 or 0xFFFF.

1.10.5 Reprogramming the security bits

Security can also be disabled by erasing and reprogramming the security bits within the flash options/security byte to the unsecured value. Since the erase operation will erase the entire sector (0x7F_FE00–0x7F_FFFF) the back-door key and the interrupt vectors will also be erased; this method is not recommended for normal single chip mode. The application software can only erase and program the flash options/security byte if the flash sector containing the flash options/security byte is not protected (see flash protection). Thus flash protection is a useful means of preventing this method. The microcontroller enters the unsecured state after the next reset following the programming of the security bits to the unsecured value.

This method requires that:

- The application software previously programmed into the microcontroller has been designed to have the capability to erase and program the flash options/security byte.
- The flash sector containing the flash options/security byte is not protected.

1.10.6 Complete memory erase

The microcontroller can be unsecured by erasing the entire EEPROM and flash memory contents. If ERASE_FLASH is successfully completed, then the flash unsecures the device and programs the security byte automatically.

1.11 Resets and interrupts

1.11.1 Resets

Table 1-13. lists all reset sources and the vector locations. Resets are explained in detail in the S12CPMU module description.

ratios ($Ratio_{H\_HVI}$, $Ratio_{L\_HVI}$) can be chosen (PIRL) on the analog input or the voltage divider can be bypassed (PTADIRL=1). Additionally in latter case the impedance converter in the ADC signal path can be used or bypassed in direct input mode (PTABYPL).

In run mode the digital input buffer of the selected pin is disabled to avoid shoot-through current (unless PTTEL is set and the voltage divider is not bypassed). Thus pin interrupts cannot be generated.

In stop mode (RPM) the digital input buffer is enabled only if DIENL=1 to support wakeup functionality.

Table 2-47 shows the HVI input configuration depending on register bits and operation mode.

Table 2-47. HVI Input Configurations

Mode	DIENL	PTAENL	Digital Input	Analog Input	Resulting Function
Run	0	0	off	off	Input disabled (Reset)
	0	1	off[1]	enabled	Analog input, interrupt not supported
	1	0	enabled	off	Digital input, interrupt supported
	1	1	off[1]	enabled	Analog input, interrupt not supported
Stop[2]	0	0	off	off	Input disabled, wakeup from stop not supported
	0	1	off	off	
	1	0	enabled	off	Digital input, wakeup from stop supported
	1	1	enabled	off	

1. Enabled if PTTEL=1 & PTADIRL=0)

2. The term “stop mode” is limited to voltage regulator operating in reduced performance mode (RPM; refer to “Low Power Modes” section in device overview). In any other case the HVI input configuration defaults to “run mode”. Therefore set PTAENL=0 before entering stop mode in order to generally support wakeup from stop.

NOTE

An external resistor R_{EXT_HVI} must always be connected to the high-voltage input to protect the device pins from fast transients and to achieve the specified pin input divider ratios when using the HVI in analog mode.

2.5 Initialization and Application Information

2.5.1 Port Data and Data Direction Register writes

It is not recommended to write PORTx/PTx and DDRx in a word access. When changing the register pins from inputs to outputs, the data may have extra transitions during the write access. Initialize the port data register before enabling the outputs.

2.5.2 SCI Baud Rate Detection

The baud rate for SCI0 and SCI1 can be determined by using a timer channel to measure the data rate on the related RXD signal.

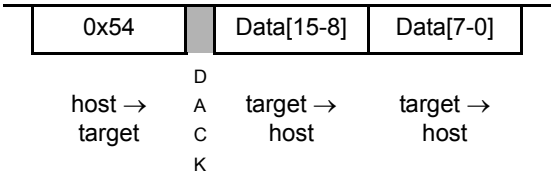
1. Establish the link:

bits[31:0]; the second to trace buffer line bits[63:32]. If ACK handshaking is disabled, the host must wait 16 clock cycles (DLY) after completing the first 32-bit read before starting the second 32-bit read.

5.4.4.13 READ_SAME.sz, READ_SAME.sz_WS

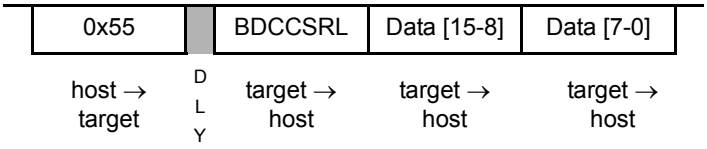
READ_SAME

Read same location specified by previous READ_MEM{_WS} **Non-intrusive**



READ_SAME_WS

Read same location specified by previous READ_MEM{_WS} **Non-intrusive**



Read from location defined by the previous READ_MEM. The previous READ_MEM command defines the address, subsequent READ_SAME commands return contents of same address. The example shows the sequence for reading a 16-bit word size. Byte alignment details are described in Section 5.4.5.2, “BDC Access Of Device Memory Mapped Resources”. If enabled, an ACK pulse is driven before the data bytes are transmitted.

NOTE

READ_SAME{_WS} is a valid command only when preceded by SYNC, NOP, READ_MEM{_WS}, or another READ_SAME{_WS} command. Otherwise, an illegal command response is returned, setting the ILLCMD bit. NOP can be used for inter-command padding without corrupting the address pointer.

5.4.4.14 READ_BDCCSR

Read BDCCSR Status Register **Always Available**

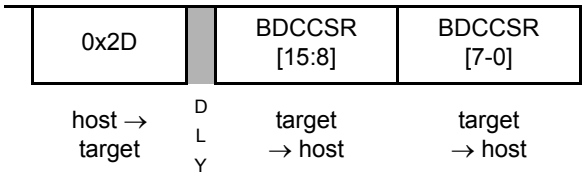


Table 8-17. CPMUHTCTL Field Descriptions

Field	Description
7 ATEMPEN	**DVBE Temperature Sensor Enable Bit** — This bit enables the DVBE temperature sensor. The output voltage of the sensor can be converted with an ADC channel. See device level specification for availability and connectivity 0 DVBE temperature sensor is disabled. 1 DVBE temperature sensor is enabled.In Stop mode the DVBE temperature sensor is always disabled to reduce power consumption.
5 VSEL	**Voltage Access Select Bit** — If set, the bandgap reference voltage V_{BG} can be accessed internally (i.e. multiplexed to an internal Analog to Digital Converter channel). If not set, the die temperature proportional voltage V_{HT} of the temperature sensor can be accessed internally. See device level specification for connectivity. For any of these access the HTE bit must be set. 0 An internal temperature proportional voltage V_{HT} can be accessed internally. 1 Bandgap reference voltage V_{BG} can be accessed internally.
3 HTE	**High Temperature Sensor/Bandgap Voltage Enable Bit** — This bit enables the high temperature sensor and bandgap voltage amplifier. 0 The temperature sensor and bandgap voltage amplifier is disabled. 1 The temperature sensor and bandgap voltage amplifier is enabled.
2 HTDS	**High Temperature Detect Status Bit** — This read-only status bit reflects the temperature status. Writes have no effect. 0 Junction Temperature is below level T_{HTID} or RPM. 1 Junction Temperature is above level T_{HTIA} and FPM.
1 HTIE	High Temperature Interrupt Enable Bit 0 Interrupt request is disabled. 1 Interrupt will be requested whenever HTIF is set.
0 HTIF	**High Temperature Interrupt Flag** — HTIF is set to 1 when HTDS status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (HTIE=1), HTIF causes an interrupt request. 0 No change in HTDS bit. 1 HTDS bit has changed.

NOTE

The voltage at the temperature sensor can be computed as follows:

$V_{HT}(temp) = V_{HT(150)} - (150 - temp) * dV_{HT}$

8.3.2.18 Autonomous Periodical Interrupt Control Register (CPMUAPICTL)

The CPMUAPICTL register allows the configuration of the autonomous periodical interrupt features.

Module Base + 0x0012

	7	6	5	4	3	2	1	0
R	APICLK	0	0	APIES	APIEA	APIFE	APIE	APIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-22. Autonomous Periodical Interrupt Control Register (CPMUAPICTL)

Read: Anytime

Write: Anytime

Table 8-19. CPMUAPICTL Field Descriptions

Field	Description
7 APICLK	**Autonomous Periodical Interrupt Clock Select Bit** — Selects the clock source for the API. Writable only if APIFE = 0. APICLK cannot be changed if APIFE is set by the same write operation. 0 Autonomous Clock (ACLK) used as source. 1 Bus Clock used as source.
4 APIES	**Autonomous Periodical Interrupt External Select Bit** — Selects the waveform at the external pin API_EXTCLK as shown in Figure 8-23. See device level specification for connectivity of API_EXTCLK pin. 0 If APIEA and APIFE are set, at the external pin API_EXTCLK periodic high pulses are visible at the end of every selected period with the size of half of the minimum period (APIR=0x0000 in Table 8-23). 1 If APIEA and APIFE are set, at the external pin API_EXTCLK a clock is visible with 2 times the selected API Period.
3 APIEA	**Autonomous Periodical Interrupt External Access Enable Bit** — If set, the waveform selected by bit APIES can be accessed externally. See device level specification for connectivity. 0 Waveform selected by APIES can not be accessed externally. 1 Waveform selected by APIES can be accessed externally, if APIFE is set.
2 APIFE	**Autonomous Periodical Interrupt Feature Enable Bit** — Enables the API feature and starts the API timer when set. 0 Autonomous periodical interrupt is disabled. 1 Autonomous periodical interrupt is enabled and timer starts running.
1 APIE	Autonomous Periodical Interrupt Enable Bit 0 API interrupt request is disabled. 1 API interrupt will be requested whenever APIF is set.
0 APIF	**Autonomous Periodical Interrupt Flag** — APIF is set to 1 when the in the API configured time has elapsed. This flag can only be cleared by writing a 1.Writing a 0 has no effect. If enabled (APIE = 1), APIF causes an interrupt request. 0 API time-out has not yet occurred. 1 API time-out has occurred.

9.4 Signal Description

This section lists all inputs to the ADC12B_LBA block.

9.4.1 Detailed Signal Descriptions

9.4.1.1 AN*x* (*x* = *n*,..., 2, 1, 0)

This pin serves as the analog input Channel *x*. The maximum input channel number is *n*. Please refer to the device reference manual for the maximum number of input channels.

9.4.1.2 VRH_0, VRH_1, VRH_2, VRL_0, VRL_1

VRH_0/1/2 are the high reference voltages, VRL_0/1 are the low reference voltages for a ADC conversion selectable on a conversion command basis. Please refer to the device overview information for availability and connectivity of these pins.

VRH_2 is only available on ADC12B_LBA V3.

VRL_1 is only available on ADC12B_LBA V1 and V2.

See also Table 9-2.

9.4.1.3 VDDA, VSSA

These pins are the power supplies for the analog circuitry of the ADC12B_LBA block.

9.6.3.2.6 Conversion flow control in case of conversion sequence control bit overrun scenarios

Restart Request Overrun:
If a legal Restart Request is detected and no Restart Event is in progress, the RSTA bit is set due to the request. The set RSTA bit indicates that a Restart Request was detected and the Restart Event is in process. In case further Restart Requests occur while the RSTA bit is set, this is defined a overrun situation. This scenario is likely to occur when bit STR_SEQA is set or when a Restart Event causes a Sequence Abort Event. The request overrun is captured in a background register that always stores the last detected overrun request. Hence if the overrun situation occurs more than once while a Restart Event is in progress, only the latest overrun request is pending. When the RSTA bit is cleared, the latest overrun request is processed and RSTA is set again one cycle later.

LoadOK Overrun:
Simultaneously at any Restart Request overrun situation the LoadOK input is evaluated and the status is captured in a background register which is alternated anytime a Restart Request Overrun occurs while Load OK Request is asserted. The Load OK background register is cleared as soon as the pending Restart Request gets processed.

Trigger Overrun:
If a Trigger occurs whilst bit TRIG is already set, this is defined as a Trigger overrun situation and causes the ADC to cease conversion at the next conversion boundary and to set bit TRIG_EIF. A overrun is also detected if the Trigger Event occurs automatically generated by hardware in “Trigger Mode” due to a Restart Event and simultaneously a Trigger Event is generated via data bus or internal interface. In this case the ADC ceases operation before conversion begins to sample. In “Trigger Mode” a Restart Request Overrun does not cause a Trigger Overrun (bit TRIG_EIF not set).

Sequence Abort Request Overrun:
If a Sequence Abort Request occurs whilst bit SEQA is already set, this is defined as a Sequence Abort Request Overrun situation and the overrun request is ignored.

9.7 Resets

At reset the ADC12B_LBA is disabled and in a power down state. The reset state of each individual bit is listed within Section 9.5.2, “Register Descriptions” which details the registers and their bit-fields.

9.8 Interrupts

The ADC supports three types of interrupts:

- Conversion Interrupt
- Sequence Abort Interrupt
- Error and Conversion Flow Control Issue Interrupt

Each of the interrupt types is associated with individual interrupt enable bits and interrupt flags.

9.8.1 ADC Conversion Interrupt

The ADC provides one conversion interrupt associated to 16 interrupt enable bits with dedicated interrupt flags. The 16 interrupt flags consist of:

- 15 conversion interrupt flags which can be associated to any conversion completion.
- One additional interrupt flag which is fixed to the “End Of List” conversion command type within the active CSL.

The association of the conversion number with the interrupt flag number is done in the conversion command.

9.8.2 ADC Sequence Abort Done Interrupt

The ADC provides one sequence abort done interrupt associated with the sequence abort request for conversion flow control. Hence, there is only one dedicated interrupt flag and interrupt enable bit for conversion sequence abort and it occurs when the sequence abort is done.

Chapter 11
Timer Module (TIM16B4CV3) Block Description

Table 11-1.

V03.02	Apri,12,2010	11.3.2.9/11-378 11.4.3/11-385	-update TCRE bit description
V03.03	Jan,14,2013		-single source generate different channel guide

11.1 Introduction

The basic scalable timer consists of a 16-bit, software-programmable counter driven by a flexible programmable prescaler.

This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform.

This timer could contain up to 4 input capture/output compare channels . The input capture function is used to detect a selected transition edge and record the time. The output compare function is used for generating output signals or for timer software delays.

A full access for the counter registers or the input capture/output compare registers should take place in one clock cycle. Accessing high byte and low byte separately for all of these registers may not yield the same result as accessing them in one word.

11.1.1 Features

The TIM16B4CV3 includes these distinctive features:

- Up to 4 channels available. (refer to device specification for exact number)
- All channels have same input capture/output compare functionality.
- Clock prescaling.
- 16-bit counter.

11.1.2 Modes of Operation

Stop: Timer is off because clocks are stopped.

Freeze: Timer counter keeps on running, unless TSFRZ in TSCR1 is set to 1.

Wait: Counters keeps on running, unless TSWAI in TSCR1 is set to 1.

buffered mode. In addition, if restart is enabled (RSTRTx=1), the commutation event generates both “PWM reload event” and “PWM reload-is-asynchronous event” simultaneously.

12.2.6 Commutation Event Edge Select Signal — async_event_edge_sel[1:0]

These device-internal PMF input signals select the active edge for the async_event input. Refer to the device overview section to determine if the selection is user configurable or tied constant at integration level.

Table 12-5. Commutation Event Edge Selection

async_event_edge-sel[1:0]	async_event active edge
00	direct input
01	rising edge
10	falling edge
11	both edges

12.2.7 PWM Reload Event Signals — pmf_reloada,b,c

These device-internal PMF output signals assert once per control cycle and can serve as triggers for other implemented IP modules. Signal pmf_reloadb and pmf_reloadc are related to time base B and C, respectively, while signal pmf_reloada is off out of reset and can be programmed for time base A, B, or C. Refer to the device overview section to determine the signal connections.

12.2.8 PWM Reload-Is-Asynchronous Signal — pmf_reload_is_async

This device-internal PMF output signal serves as a qualifier to the PMF reload event signal pmf_reloada. Whenever the async_event signal causes pmf_reloada output to assert also the pmf_reload_is_async output asserts for the same duration, except if asynchronous event and generated PWM reload event occur in the same cycle.

Table 12-10. PMFFEN Field Descriptions

Field	Description
6,4-0 FEN[5:0]	Fault *m* Enable — This register cannot be modified after the WP bit is set. 0 FAULT*m* input is disabled 1 FAULT*m* input is enabled for fault protection *m* is 0, 1, 2, 3, 4 and 5

12.3.2.6 PMF Fault Mode Register (PMFFMOD)

Address: Module Base + 0x0005 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	FMOD5	0	FMOD4	FMOD3	FMOD2	FMOD1	FMOD0
W								
Reset	0	0	0	0	0	0	0	0

Figure 12-8. PMF Fault Mode Register (PMFFMOD)

1. Read: Anytime
   Write: Anytime

Table 12-11. PMFFMOD Field Descriptions

Field	Description
6,4-0 FMOD[5:0]	**Fault *m* Pin Recovery Mode** — This bit selects automatic or manual recovery of FAULT*m* input faults. See Section 12.4.13.2, “Automatic Fault Recovery” and Section 12.4.13.3, “Manual Fault Recovery” for more details. 0 Manual fault recovery of FAULT*m* input faults 1 Automatic fault recovery of FAULT*m* input faults *m* is 0, 1, 2, 3, 4 and 5.

12.3.2.7 PMF Fault Interrupt Enable Register (PMFFIE)

Address: Module Base + 0x0006 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	FIE5	0	FIE4	FIE3	FIE2	FIE1	FIE0
W								
Reset	0	0	0	0	0	0	0	0

Figure 12-9. PMF Fault Interrupt Enable Register (PMFFIE)

1. Read: Anytime
   Write: Anytime

2. Wait mode
   All PTU features are available.
3. Freeze Mode
   Depends on the PTUFRZ register bit setting the internal counter is stopped and no trigger events will be generated.
4. Stop mode
   The PTU is disabled and the internal counter is stopped; no trigger events will be generated. The content of the configuration register is unchanged.

13.1.3 Block Diagram

Figure 13-1 shows a block diagram of the PTU module.

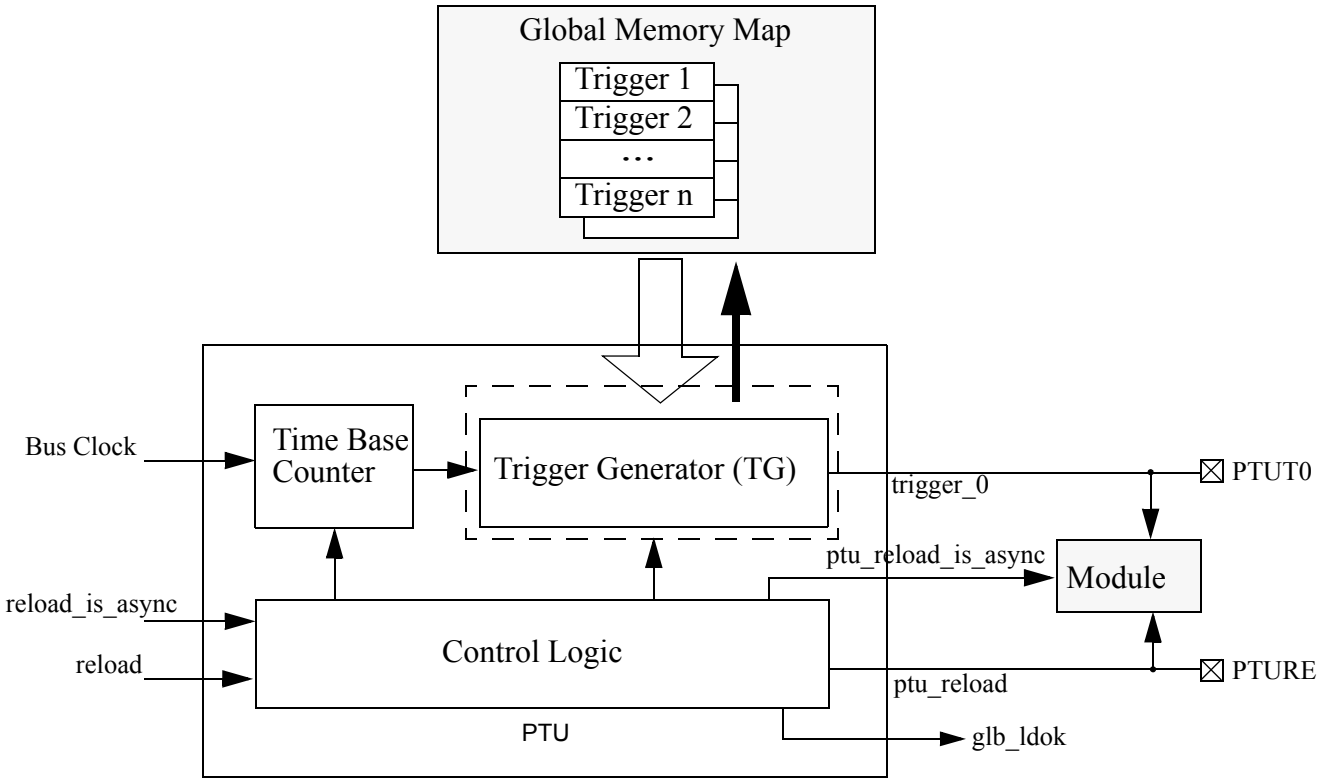


Figure 13-1. PTU Block Block Diagram

13.2 External Signal Description

This section lists the name and description of all external ports.

13.2.1 PTUT0 — PTU Trigger 0

If enabled (PTUT0PE is set) this pin shows the internal trigger_0 event.

13.3.2.5 PTU Interrupt Flag Register High (PTUIFH)

Module Base + 0x0004 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PTUDEEF	PTUROIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-7. PTU Interrupt Flag Register High (PTUIFH)

1. Read: Anytime
   Write: Anytime, write 1 to clear

Table 13-7. PTUIFH Register Field Descriptions

Field	Description
1 PTUDEEF	PTU Double bit ECC Error Flag — This bit is set if the read data from the memory contains double bit ECC errors. While this bit is set the trigger generation of both trigger generators stops. 0 No double bit ECC error occurs 1 Double bit ECC error occurs
0 PTUROIF	PTU Reload Overrun Interrupt Flag — If reload event occurs when the PTULDOK bit is not set then this bit will be set. This bit is not set if the reload event was forced by an asynchronous commutation event. 0 No reload overrun occurs 1 Reload overrun occurs

13.3.2.6 PTU Interrupt Flag Register Low (PTUIFL)

Module Base + 0x0005 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	TG0AEIF	TG0REIF	TG0EIF	TG0DIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-8. PTU Interrupt Flag Register Low (PTUIFL)

1. Read: Anytime
   Write: Anytime, write 1 to clear

To determine the value of a data bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 14-19 summarizes the results of the data bit samples.

Table 14-19. Data Bit Recovery

RT8, RT9, and RT10 Samples	Data Bit Determination	Noise Flag
000	0	0
001	0	1
010	0	1
011	1	1
100	0	1
101	1	1
110	1	1
111	1	0

NOTE

The RT8, RT9, and RT10 samples do not affect start bit verification. If any or all of the RT8, RT9, and RT10 start bit samples are logic 1s following a successful start bit verification, the noise flag (NF) is set and the receiver assumes that the bit is a start bit (logic 0).

To verify a stop bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 14-20 summarizes the results of the stop bit samples.

Table 14-20. Stop Bit Recovery

RT8, RT9, and RT10 Samples	Framing Error Flag	Noise Flag
000	1	0
001	1	1
010	1	1
011	0	1
100	1	1
101	0	1
110	0	1
111	0	0

In Figure 14-22 the verification samples RT3 and RT5 determine that the first low detected was noise and not the beginning of a start bit. The RT clock is reset and the start bit search begins again. The noise flag is not set because the noise occurred before the start bit was found.

18.3.2.11 GDU Phase Log Register (GDUPHL)

Module Base + 0x000C — Access: User read only(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	GPHL[1:0]	
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-13. GDU Phase Log Register (GDUPHL)

1. Read: Anytime
   Write: never

Table 18-12. GDU Phase Log Register Field Descriptions

Field	Description
1:0 GPHL[1:0]	**GDU Phase Log Bits**— If a desaturation error occurs the phase status bits GPHS[1:0] in register GDUSTAT are copied to this register. The GDUPHL register is cleared only on reset. See Section 18.4.5, “Desaturation Error

18.3.2.12 GDU Clock Control Register 2 (GDUCLK2)

Module Base + 0x000D — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	GCPCD[3:0]			
W								
Reset	0	0	0	0	0	0	0	0

Figure 18-14. GDU Clock Control Register 2 (GDUCLK2)

1. Read: Anytime
   Write: Only if GWP=0

Table 18-13. GDUCLK2 Register Field Descriptions

Field	Description
3-0 GCPCD[3:0]	**GDU Charge Pump Clock Divider** — These bits select the clock divider factor which is used to divide down the bus clock frequency f_{BUS} for the charge pump clock f_{CP}. See Table 18-14 for divider factors. These bits cannot be modified after GWP bit is set. See also Section 18.4.4, “Charge Pump

NOTE

The GCPCD bits must be set to the required value before GCPE bit is set. If a different charge pump clock frequency is required GCPE has to be cleared before new values to GCPCD bits are written.

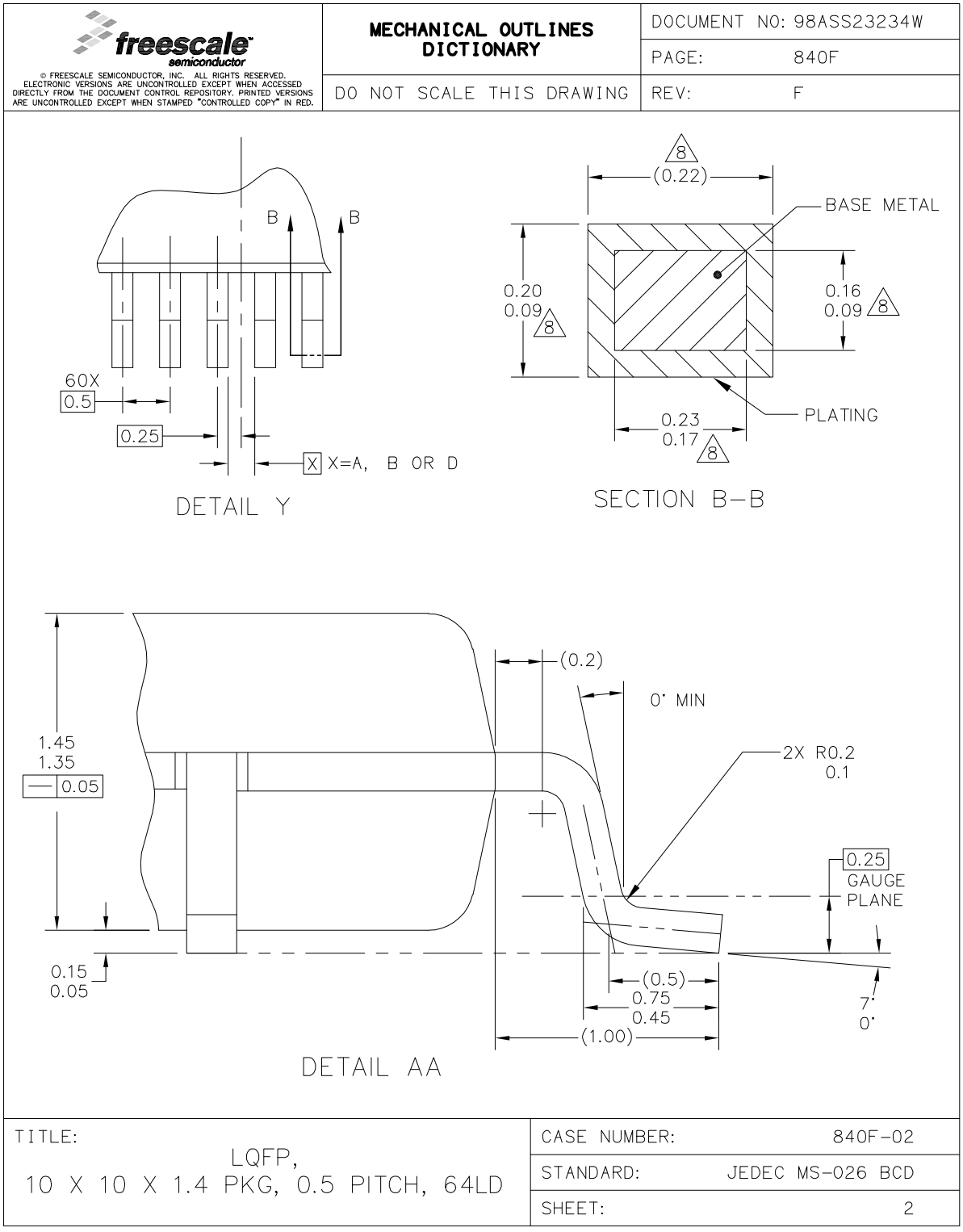


Figure J-2. 64LQFP Mechanical Information (2 of 3)

L.5 0x0200-0x037F PIM Map

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0200	MODRR0	R	0	0	Reserved	0	SCI1RR	S0L0RR2-0		
		W								
0x0201	MODRR1	R	0	0	0	0	0	0	TRIG0RR1-0	
		W								
0x0202	MODRR2	R	0	0	0	0	0	0	0	0
		W								
0x0203	MODRR3	R	0	0	0	T0IC3RR1-0		T0IC2RR	0	0
		W								
0x0204	MODRR4	R	FAULT5RR	0	P0C5RR	P0C4RR	P0C3RR	P0C2RR	P0C1RR	P0C0RR
		W								
0x0205	MODRR5	R	T1IC3RR	T1IC2RR	T1IC1RR	T1IC0RR	0	T1OC2RR	T1OC1RR	0
		W								
0x0206–0x0207	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0208	ECLKCTL	R	NECLK	0	0	0	0	0	0	0
		W								
0x0209	IRQCR	R	IRQE	IRQEN	0	0	0	0	0	0
		W								
0x020A–0x020C	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x020D	Reserved	R	0	0	0	0	0	Reserved	0	Reserved
		W								
0x020E	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x020F	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x0210–0x025F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0260	PTE	R	0	0	0	0	0	0	PTE1	PTE0
		W								