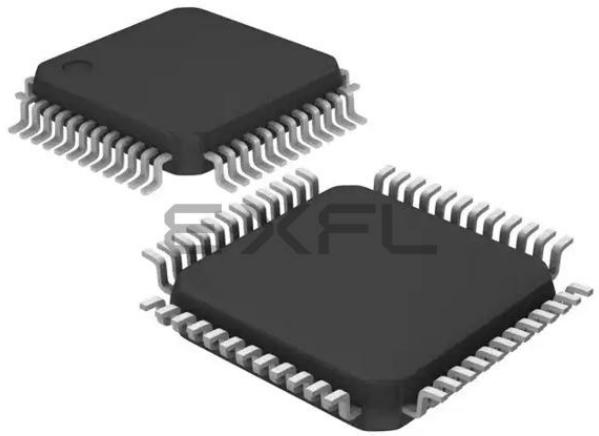

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Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	15
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmba6f0vlf

Rev. No. (Item No.)	Date (Submitted By)	Sections Affected	Substantial Change(s)
V03.10	16 Sep 2015	2.1.1/2-68 2.2/2-71	• Corrections
V03.11	23 Nov 2015	2.4.6/2-110	• Corrections
V03.12	23 Mar 2016		• Corrections

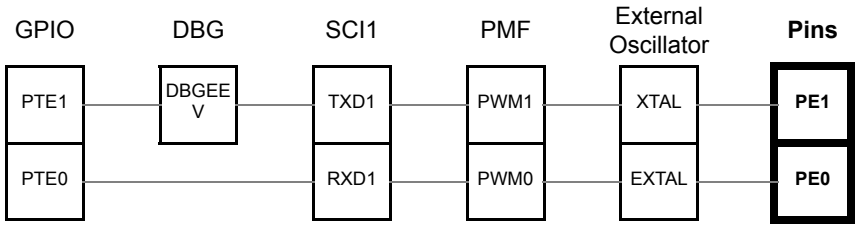
2.1 Introduction

2.1.1 Overview

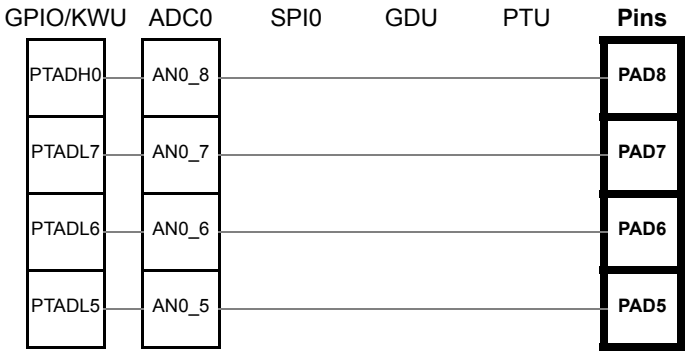
The S12ZVMB-family port integration module establishes the interface between the peripheral modules and the I/O pins for all ports. It controls the electrical pin properties as well as the signal prioritization and multiplexing on shared pins.

This document covers:

- Port E



- Port AD



3.3.2.2 Error Code Register (MMCECH, MMCECL)

Address: 0x0080 (MMCECH)

	7	6	5	4	3	2	1	0
R W	ITR[3:0]				TGT[3:0]			
Reset	0	0	0	0	0	0	0	0

Address: 0x0081 (MMCECL)

	7	6	5	4	3	2	1	0
R W	ACC[3:0]				ERR[3:0]			
Reset	0	0	0	0	0	0	0	0

Figure 3-5. Error Code Register (MMCEC)

Read: Anytime

Write: Write of 0xFFFF to MMCECH:MMCECL resets both registers to 0x0000

Table 3-5. MMCECH and MMCECL Field Descriptions

Field	Description
7-4 (MMCECH) ITR[3:0]	**Initiator Field** — The ITR[3:0] bits capture the initiator which caused the access violation. The initiator is captured in form of a 4 bit value which is assigned as follows: 0: none (no error condition detected) 1: S12ZCPU 2: reserved 3: ADC 4-15: reserved
3-0 (MMCECH) TGT[3:0]	**Target Field** — The TGT[3:0] bits capture the target of the faulty access. The target is captured in form of a 4 bit value which is assigned as follows: 0: none 1: register space 2: RAM 3: EEPROM 4: program flash 5: IFR 6-15: reserved

6.4.2.1 Exact Address Comparator Match

With range comparisons disabled, the match condition is an exact equivalence of address bus with the value stored in the comparator address registers. Qualification of the type of access (R/W) is also possible.

Code may contain various access forms of the same address, for example a 16-bit access of ADDR[n] or byte access of ADDR[n+1] both access n+1. The comparators ensure that any access of the address defined by the comparator address register generates a match, as shown in the example of Table 6-27. Thus if the comparator address register contains ADDR[n+1] any access of ADDR[n+1] matches. This means that a 16-bit access of ADDR[n] or 32-bit access of ADDR[n-1] also match because they also access ADDR[n+1]. The right hand columns show the contents of DBGxA that would match for each access.

Table 6-27. Comparator Address Bus Matches

Access	Address	ADDR[n]	ADDR[n+1]	ADDR[n+2]	ADDR[n+3]
32-bit	ADDR[n]	Match	Match	Match	Match
16-bit	ADDR[n]	Match	Match	No Match	No Match
16-bit	ADDR[n+1]	No Match	Match	Match	No Match
8-bit	ADDR[n]	Match	No Match	No Match	No Match

If the comparator INST bit is set, the comparator address register contents are compared with the PC, the data register contents and access type bits are ignored. The comparator address register must be loaded with the address of the first opcode byte.

6.4.2.2 Address and Data Comparator Match

Comparator A features data comparators, for data access comparisons. The comparators do not evaluate if accessed data is valid. Accesses across aligned 32-bit boundaries are split internally into consecutive accesses. The data comparator mapping to accessed addresses for the CPU is shown in Table 6-28, whereby the Address column refers to the lowest 2 bits of the lowest accessed address. This corresponds to the most significant data byte.

Table 6-28. Comparator Data Byte Alignment

Address[1:0]	Data Comparator
00	DBGxD0
01	DBGxD1
10	DBGxD2
11	DBGxD3

The fixed mapping of data comparator bytes to addresses within a 32-bit data field ensures data matches independent of access size. To compare a single data byte within the 32-bit field, the other bytes within that field must be masked using the corresponding data mask registers. This ensures that any access of that byte (32-bit,16-bit or 8-bit) with matching data causes a match. If no bytes are masked then the data comparator always compares all 32-bits and can only generate a match on a 32-bit access with correct 32-bit data value. In this case, 8-bit or 16-bit accesses within the 32-bit field cannot generate a match even if

Table 6-30. NDB and MASK bit dependency

NDB	DBGADM	Comment
0	0	Do not compare data bus bit.
0	1	Compare data bus bit. Match on equivalence.
1	0	Do not compare data bus bit.
1	1	Compare data bus bit. Match on difference.

6.4.2.4 Range Comparisons

Range comparisons are accurate to byte boundaries. Thus for data access comparisons a match occurs if at least one byte of the access is in the range (inside range) or outside the range (outside range). For opcode comparisons only the address of the first opcode byte is compared with the range.

When using the AB comparator pair for a range comparison, the data bus can be used for qualification by using the comparator A data and data mask registers. The DBGACTL RW and RWE bits can be used to qualify the range comparison on either a read or a write access. The corresponding DBGBCTL bits are ignored. The DBGACTL COMPE/INST bits are used for range comparisons. The DBGBCTL COMPE/INST bits are ignored in range modes.

6.4.2.4.1 Inside Range (CompA_Addr $\leq$ address $\leq$ CompB_Addr)

In the Inside Range comparator mode, comparator pair A and B can be configured for range comparisons by the control register (DBGC2). The match condition requires a simultaneous valid match for both comparators. A match condition on only one comparator is not valid.

6.4.2.4.2 Outside Range (address < CompA_Addr or address > CompB_Addr)

In the Outside Range comparator mode, comparator pair A and B can be configured for range comparisons. A single match condition on either of the comparators is recognized as valid. Outside range mode in combination with opcode address matches can be used to detect if opcodes are from an unexpected range.

NOTE

When configured for data access matches, an outside range match would typically occur at any interrupt vector fetch or register access. This can be avoided by setting the upper or lower range limit to $FFFFFF or $000000 respectively. Interrupt vector fetches do not cause opcode address matches.

6.4.3 Events

Events are used as qualifiers for a state sequencer change of state. The state control register for the current state determines the next state for each event. An event can immediately initiate a transition to the next state sequencer state whereby the corresponding flag in DBGSR is set.

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000E	RESERVED CPMUTEST1	R	0	0	0	0	0	0	0	0
		W								
0x000F	CPMU ARMCOP	R	0	0	0	0	0	0	0	0
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0010	CPMU HTCTL	R	ATEMPEN	0	VSEL	0	HTE	HTDS	HTIE	HTIF
		W								
0x0011	CPMU LVCTL	R	0	0	0	0	0	LVDS	LVIE	LVIF
		W								
0x0012	CPMU APICTL	R	APICLK	0	0	APIES	APIEA	APIFE	APIE	APIF
		W								
0x0013	CPMUACLKTR	R	ACLKTR5	ACLKTR4	ACLKTR3	ACLKTR2	ACLKTR1	ACLKTR0	0	0
		W								
0x0014	CPMUAPIRH	R	APIR15	APIR14	APIR13	APIR12	APIR11	APIR10	APIR9	APIR8
		W								
0x0015	CPMUAPIRL	R	APIR7	APIR6	APIR5	APIR4	APIR3	APIR2	APIR1	APIR0
		W								
0x0016	RESERVED	R	0	0	0	0	0	0	0	0
		W								
0x0017	CPMUHTTR	R	HTOE	0	0	0	HTTR3	HTTR2	HTTR1	HTTR0
		W								
0x0018	CPMU IRCTRIMH	R	TCTRIM[4:0]					0	IRCTRIM[9:8]	
		W								
0x0019	CPMU IRCTRIML	R	IRCTRIM[7:0]							
		W								
0x001A	CPMUOSC	R	OSCE	0	Reserved	0	0	0	0	0
		W								
0x001B	CPMUPROT	R	0	0	0	0	0	0	0	PROT
		W								
0x001C	RESERVED CPMUTEST2	R	0	0	0	0	0	0	0	0
		W								
0x001D	CPMU VREGCTL	R	0	0	0	0	0	0	EXTXON	INTXON
		W								
0x001E	CPMUOSC2	R	0	0	0	0	0	0	OMRE	OSCMOD
		W								
0x001F	RESERVED	R	0	0	0	0	0	0	0	0
		W								

= Unimplemented or Reserved

Figure 8-3. CPMU Register Summary

Table 8-2. CPMURFLG Field Descriptions

Field	Description
6 PORF	**Power on Reset Flag** — PORF is set to 1 when a power on reset occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Power on reset has not occurred. 1 Power on reset has occurred.
5 LVRF	**Low Voltage Reset Flag** — LVRF is set to 1 when a low voltage reset occurs on the VDD, VDDF or VDDX domain. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Low voltage reset has not occurred. 1 Low voltage reset has occurred.
3 COPRF	**COP Reset Flag** — COPRF is set to 1 when a COP (Computer Operating Properly) reset occurs. Refer to 8.5.5, “Computer Operating Properly Watchdog (COP) Reset and 8.3.2.12, “S12CPMU_UHV_V11 COP Control Register (CPMUCOP) for details.This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 COP reset has not occurred. 1 COP reset has occurred.
1 OMRF	**Oscillator Clock Monitor Reset Flag** — OMRF is set to 1 when a loss of oscillator (crystal) clock occurs. Refer to8.5.3, “Oscillator Clock Monitor Reset for details.This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Loss of oscillator clock reset has not occurred. 1 Loss of oscillator clock reset has occurred.
0 PMRF	**PLL Clock Monitor Reset Flag** — PMRF is set to 1 when a loss of PLL clock occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Loss of PLL clock reset has not occurred. 1 Loss of PLL clock reset has occurred.

8.3.2.4 S12CPMU_UHV_V11 Synthesizer Register (CPMUSYNR)

The CPMUSYNR register controls the multiplication factor of the PLL and selects the VCO frequency range.

Module Base + 0x0004

Figure 8-7. S12CPMU_UHV_V11 Synthesizer Register (CPMUSYNR)

Read: Anytime

Write: If PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register), then write anytime. Else write has no effect.

NOTE

Writing to this register clears the LOCK and UPOSC status bits.

8.3.2.11 S12CPMU_UHV_V11 RTI Control Register (CPMURTI)

This register selects the time-out period for the Real Time Interrupt.

The clock source for the RTI is either IRCCLK or OSCCLK depending on the setting of the RTIOSCSEL bit. In Stop Mode with PSTP=1 (Pseudo Stop Mode) and RTIOSCSEL=1 the RTI continues to run, else the RTI counter halts in Stop Mode.

Module Base + 0x000B

	7	6	5	4	3	2	1	0
R W	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
Reset	0	0	0	0	0	0	0	0

Figure 8-14. S12CPMU_UHV_V11 RTI Control Register (CPMURTI)

Read: Anytime

Write: Anytime

NOTE

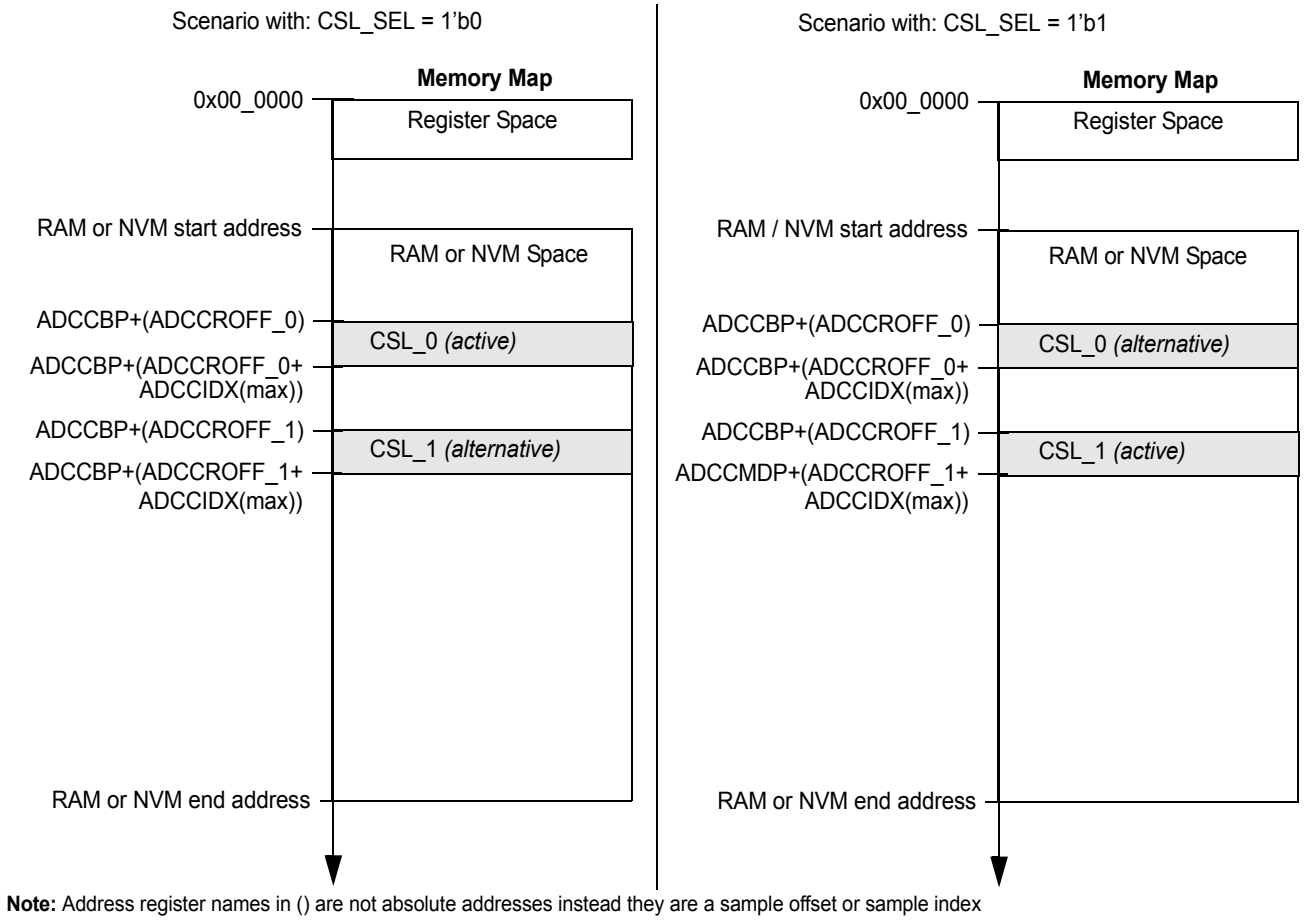
A write to this register starts the RTI time-out period. A change of the RTIOSCSEL bit (writing a different value or loosing UPOSC status) re-starts the RTI time-out period.

Table 8-11. CPMURTI Field Descriptions

Field	Description
7 RTDEC	**Decimal or Binary Divider Select Bit** — RTDEC selects decimal or binary based prescaler values. 0 Binary based divider value. See Table 8-12 1 Decimal based divider value. See Table 8-13
6–4 RTR[6:4]	**Real Time Interrupt Prescale Rate Select Bits** — These bits select the prescale rate for the RTI.See Table 8-12 and Table 8-13.
3–0 RTR[3:0]	**Real Time Interrupt Modulus Counter Select Bits** — These bits select the modulus counter target value to provide additional granularity.Table 8-12 and Table 8-13 show all possible divide values selectable by the CPMURTI register.

9.6.3.2.2 Introduction of the two Command Sequence Lists (CSLs)

The two Command Sequence Lists (CSLs) can be referred to via the Command Base Pointer Register plus the Command and Result Offset Registers plus the Command Index Register (ADCCBP, ADCCROFF_0/1, ADCCIDX).
The final address for conversion command loading is calculated by the sum of these registers (e.g.: ADCCBP+ADCCROFF_0+ADCCIDX or ADCCBP+ADCCROFF_1+ADCCIDX).
Bit CSL_BMOD selects if the CSL is used in double buffer or single buffer mode. In double buffer mode, the CSL can be swapped by flow control bits LDOK and RSTA. For detailed information about when and how the CSL is swapped, please refer to Section 9.6.3.2.5, “The four ADC conversion flow control bits - description of Restart Event + CSL Swap, Section 9.9.7.1, “Initial Start of a Command Sequence List and Section 9.9.7.3, “Restart CSL execution with new/other CSL (alternative CSL becomes active CSL) — CSL swapping
Which list is actively used for ADC command loading is indicated by bit CSL_SEL. The register to define the CSL start addresses (ADCCBP) can be set to any even location of the system RAM or NVM area. It is the user’s responsibility to make sure that the different ADC lists do not overlap or exceed the system RAM or the NVM area, respectively. The error flag IA_EIF will be set for accesses to ranges outside system RAM area and cause an error interrupt if enabled.



Note: Address register names in () are not absolute addresses instead they are a sample offset or sample index

Figure 9-31. Command Sequence List Schema in Double Buffer Mode

Table 10-5. BATIF Register Field Descriptions

Field	Description
1 BVHIF	BATS Interrupt Flag High Detect — The flag is set to 1 when BVHC status bit changes. 0 No change of the BVHC status bit since the last clearing of the flag. 1 BVHC status bit has changed since the last clearing of the flag.
0 BVLIF	BATS Interrupt Flag Low Detect — The flag is set to 1 when BVLC status bit changes. 0 No change of the BVLC status bit since the last clearing of the flag. 1 BVLC status bit has changed since the last clearing of the flag.

10.3.2.5 Reserved Register

Module Base + 0x0006
Module Base + 0x0007

Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

Figure 10-8. Reserved Register

1. Read: Anytime
   Write: Only in special mode

NOTE

These reserved registers are designed for factory test purposes only and are not intended for general user access. Writing to these registers when in special mode can alter the module's functionality.

10.4 Functional Description

10.4.1 General

The BATS module allows measuring the voltage on the VSUP pin. The voltage at the VSUP pin can be routed via an internal voltage divider to an internal Analog to Digital Converter Channel. Also the BATS module can be configured to generate a low and high voltage interrupt based on VSUP. The trigger level of the high and low interrupt are selectable.

10.4.2 Interrupts

This section describes the interrupt generated by the BATS module. The interrupt is only available in CPU run mode. Entering and exiting CPU stop mode has no effect on the interrupt flags.

To make sure the interrupt generation works properly the bus clock frequency must be higher than the Voltage Warning Low Pass Filter frequency (f_{VWLP_filter}).

11.3.2.7 Timer Control Register 3/Timer Control Register 4 (TCTL3 and TCTL4)

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Figure 11-12. Timer Control Register 3 (TCTL3)

Module Base + 0x000B

	7	6	5	4	3	2	1	0
R W	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
Reset	0	0	0	0	0	0	0	0

Figure 11-13. Timer Control Register 4 (TCTL4)

Read: Anytime

Write: Anytime.

Table 11-8. TCTL3/TCTL4 Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
3:0 EDGnB EDGnA	**Input Capture Edge Control** — These four pairs of control bits configure the input capture edge detector circuits.

Table 11-9. Edge Detector Circuit Configuration

EDGnB	EDGnA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge (rising or falling)

buffered mode. In addition, if restart is enabled (RSTRTx=1), the commutation event generates both “PWM reload event” and “PWM reload-is-asynchronous event” simultaneously.

12.2.6 Commutation Event Edge Select Signal — async_event_edge_sel[1:0]

These device-internal PMF input signals select the active edge for the async_event input. Refer to the device overview section to determine if the selection is user configurable or tied constant at integration level.

Table 12-5. Commutation Event Edge Selection

async_event_edge-sel[1:0]	async_event active edge
00	direct input
01	rising edge
10	falling edge
11	both edges

12.2.7 PWM Reload Event Signals — pmf_reloada,b,c

These device-internal PMF output signals assert once per control cycle and can serve as triggers for other implemented IP modules. Signal pmf_reloadb and pmf_reloadc are related to time base B and C, respectively, while signal pmf_reloada is off out of reset and can be programmed for time base A, B, or C. Refer to the device overview section to determine the signal connections.

12.2.8 PWM Reload-Is-Asynchronous Signal — pmf_reload_is_async

This device-internal PMF output signal serves as a qualifier to the PMF reload event signal pmf_reloada. Whenever the async_event signal causes pmf_reloada output to assert also the pmf_reload_is_async output asserts for the same duration, except if asynchronous event and generated PWM reload event occur in the same cycle.

12.3 Memory Map and Registers

12.3.1 Module Memory Map

A summary of the registers associated with the PMF module is shown in Figure 12-2. Detailed descriptions of the registers and bits are given in the subsections that follow.

NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	PMFCFG0	R	WP	MTG	EDGEC	EDGEB	EDGEA	INDEPC	INDEPB	INDEPA
		W								
0x0001	PMFCFG1	R	0	ENCE	BOTNEGC	TOPNEGC	BOTNEGB	TOPNEGB	BOTNEGA	TOPNEGA
		W								
0x0002	PMFCFG2	R	REV1	REV0	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0
		W								
0x0003	PMFCFG3	R	PMFWAI	PMFFRZ	0	VLMODE		PINVC	PINVB	PINVA
		W								
0x0004	PMFFEN	R	0	FEN5	0	FEN4	FEN3	FEN2	FEN1	FEN0
		W								
0x0005	PMFFMOD	R	0	FMOD5	0	FMOD4	FMOD3	FMOD2	FMOD1	FMOD0
		W								
0x0006	PMFFIE	R	0	FIE5	0	FIE4	FIE3	FIE2	FIE1	FIE0
		W								
0x0007	PMFFIF	R	0	FIF5	0	FIF4	FIF3	FIF2	FIF1	FIF0
		W								
0x0008	PMFQSMP0	R	0	0	0	0	QSMP5		QSMP4	
		W								
0x0009	PMFQSMP1	R	QSMP3		QSMP2		QSMP1		QSMP0	
		W								
0x000A-0x000B	Reserved	R	0	0	0	0	0	0	0	0
		W								

= Unimplemented or Reserved

Figure 12-2. Quick Reference to PMF Registers (Sheet 1 of 5)

16.3.9 HSDRV2C Interrupt Flag Register (HSIF)

Module Base + 0x0007 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	HSOCIF1	HSOCIF0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 16-8. HSDRV2C Interrupt Flag Register (HSIF)

1. Read: Anytime
   Write: Write 1 to clear, writing 0 has no effect

Table 16-10. HSDRV Interrupt Flag Register (HSIF) Field Descriptions

Field	Description
1-0 HSOCIFx	HSDRV2C Over-Current Interrupt Flags These flags are set when an over-current event occurs on the associated high-side driver (| I_{HS} | > | I_{OCTHSX} |). While set the associated high-side driver is turned off. Once the flag is cleared, the driver is controlled again by the source selected in PIM module. 0 No over-current event occurred since last clearing of flag 1 An over-current event occurred since last clearing of flag

16.4 Functional Description

16.4.1 General

The HSDRV2C module provides two high-side drivers able to drive LED or resistive loads. The drivers can be controlled directly through register bits or alternatively by dedicated timer or PWM channels. See PIM chapter for routing details.

The following sub-section describes the open-load and over-current detection features for both drivers.

16.4.2 Open Load Detection

A “High-load resistance Open Load Detection” can be enabled for the driver by setting the associated HSCR[HSEOLx] bit (refer to Section 16.3.4, “HSDRV2C Configuration Register (HSCR)”. This detection is only active when the associated driver is enabled and it is not being driven. To detect an open-load condition a small current I_{HVOLDC} will flow through the load. If the driving pin HS[x] stays at a voltage above an internal threshold then an open load will be detected for the associated high-side driver.

The open-load condition is flagged in the HSDRV Status Register (HSSR).

Please note that if the bit time is smaller than the parameter t_{OCLIM} (please refer to electricals), then no overcurrent is reported nor does an overcurrent shutdown occur. However, the current limitation is always engaged in case of a failure.

17.4.3 Modes

Figure 17-11 shows the possible mode transitions depending on control bits, stop mode, and error conditions.

17.4.3.1 Shutdown Mode

The LIN Physical Layer is fully disabled. No wake-up functionality is available. The internal pullup resistor is high ohmic only (330 kΩ) to maintain the LIN Bus pin in the recessive state. LPTxD is not monitored in this mode for a TxD-dominant timeout. All the registers are accessible.

Setting LPE causes the module to leave the shutdown mode and to enter the normal mode or receive only mode (if RXONLY bit is set).

Clearing LPE causes the module to leave the normal or receive only modes and go back to shutdown mode.

17.4.3.2 Normal Mode

The full functionality is available. Both receiver and transmitter are enabled. The internal pullup resistor can be chosen to be high ohmic (330 kΩ) if LPPUE = 0, or LIN compliant (34 kΩ) if LPPUE = 1.

If RXONLY is set, the module leaves normal mode to enter receive only mode.

If the MCU enters stop mode, the LIN Physical Layer enters standby mode.

17.4.3.3 Receive Only Mode

Entering this mode disables the transmitter and immediately stops any on-going transmission. LPTxD is not monitored in this mode for a TxD-dominant timeout.

The receiver is running in full performance mode in all cases.

To return to normal mode, the RXONLY bit must be cleared.

If the device enters stop mode, the module leaves receive only mode to enter standby mode.

17.4.3.4 Standby Mode with Wake-Up Feature

The transmitter of the LIN Physical Layer is disabled and the receiver enters a low power mode.

NOTE

Before entering standby mode, ensure no transmissions are ongoing.

If LPWUE is not set, no wake up feature is available and the standby mode has the same electrical properties as the shutdown mode. This allows a low-power consumption of the device in stop mode if the wake-up feature is not needed.

18.3.2.1 GDU Module Enable Register (GDUE)

Module Base + 0x0000 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	GWP	GOVA	0	0	0	GCSE0	GCPE	GFDE
W								
Reset	0	0	0	0	0	0	0	1

= Unimplemented

Figure 18-3. GDU Module Enable Register (GDUE)

1. Read: Anytime
   Write: Anytime, write protected bits only if GWP=0. On entry in stop mode bits GCSE0, GCPE and GFDE are cleared. After exit from stop mode write protected bits GCPE and GFDE can be written once when GWP=1.

Table 18-2. GDUE Register Field Description

Field	Description
7 GWP	**GDU Write Protect**— This bit enables write protection to be used for the write protectable bits. While clear, GWP allows write protectable bits to be written. When set GWP prevents any further writes to write protectable bits. Once set , GWP is cleared by reset. 0 Write-protectable bits may be written 1 Write-protectable bits cannot be written
6 GOVA	**GDU Overvoltage Action** — This bit cannot be modified after GWP bit is set. 0 If an overvoltage condition on GHD pin occurs and GHHDF is set the high-side FET pre-drivers are turned off and the low-side FET pre-drivers are turned on. 1 If an overvoltage condition on GHD pin occurs and GHHDF is set the high-side FET pre-drivers and the low-side FET pre-drivers are turned off.
2 GCSE0	**GDU Current Sense Amplifier 0 Enable**— This bit enables the current sense amplifier. See Section 18.4.8, “Current Sense Amplifier and Overcurrent Comparator 0 Current sense amplifier 0 is disabled 1 Current sense amplifier 0 is enabled
1 GCPE	**GDU Charge Pump Enable** — This bit enables the charge pump. This bit cannot be modified after GWP bit is set. See Section 18.4.4, “Charge Pump 0 Charge pump is disabled 1 Charge pump is enabled
0 GFDE	**GDU FET Pre-Driver Enable** — This bit enables the low-side and high-side FET pre-drivers. This bit cannot be modified after GWP bit is set.See Section 18.4.2, “Low-Side FET Pre-Drivers and Section 18.4.3, “High-Side FET Pre-Driver. 0 Low-side and high-side drivers are disabled 1 Low-side and high-side drivers are enabled **NOTE** It is not allowed to set and clear GFDE bit periodically in order to switch on and off the FET pre-drivers. In order to switch on and off the FET pre-drivers the PMF module has to be used to mask and un-mask the PWM channels.

Figure 18-22. Short to Ground Detection

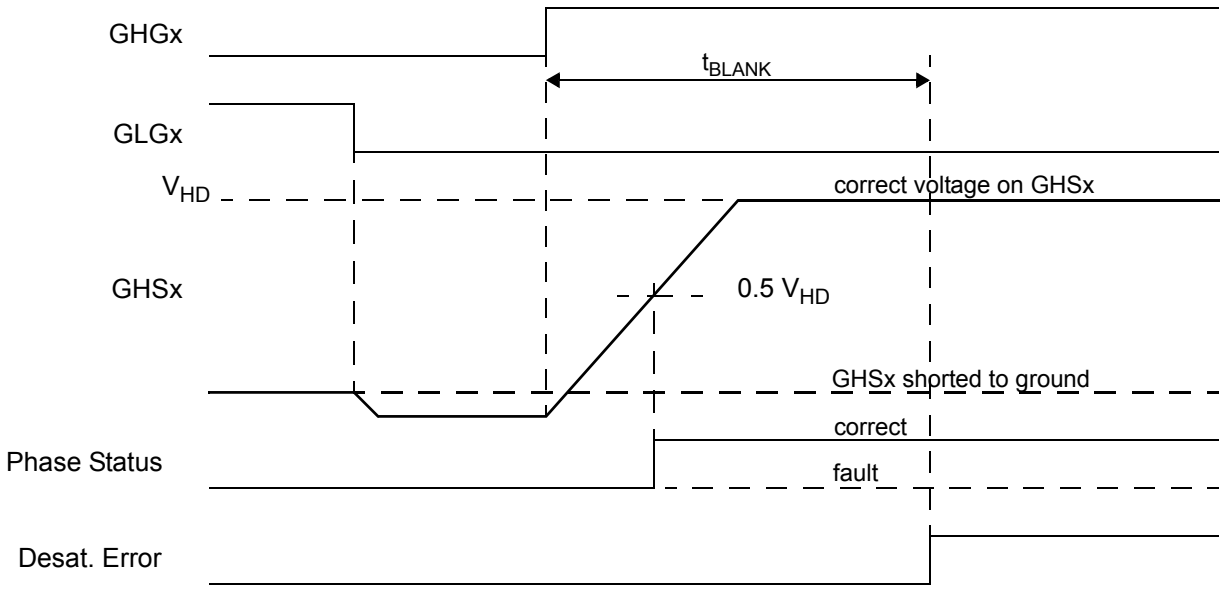


Table 19-5. Program IFR Fields

Global Address	Size (Bytes)	Field Description
0x1F_C000 – 0x1F_C007	8	Reserved
0x1F_C008 – 0x1F_C0B5	174	Reserved
0x1F_C0B6 – 0x1F_C0B7	2	Version ID[1]
0x1F_C0B8 – 0x1F_C0BF	8	Reserved
0x1F_C0C0 – 0x1F_C0FF	64	Program Once Field Refer to Section 19.4.7.6, “Program Once Command”

1. Used to track firmware patch versions, see Section 19.4.2

Table 19-6. Memory Controller Resource Fields (NVM Resource Area[1])

Global Address	Size (Bytes)	Description
0x1F_4000 – 0x1F_41FF	512	Reserved
0x1F_4200 – 0x1F_7FFF	15,872	Reserved
0x1F_8000 – 0x1F_97FF	6,144	Reserved
0x1F_9800 – 0x1F_BFFF	10,240	Reserved
0x1F_C000 – 0x1F_C0FF	256	P-Flash IFR (see Table 19-5)
0x1F_C100 – 0x1F_C1FF	256	Reserved.
0x1F_C200 – 0x1F_FFFF	15,872	Reserved.

1. See Section 19.4.4 for NVM Resources Area description.

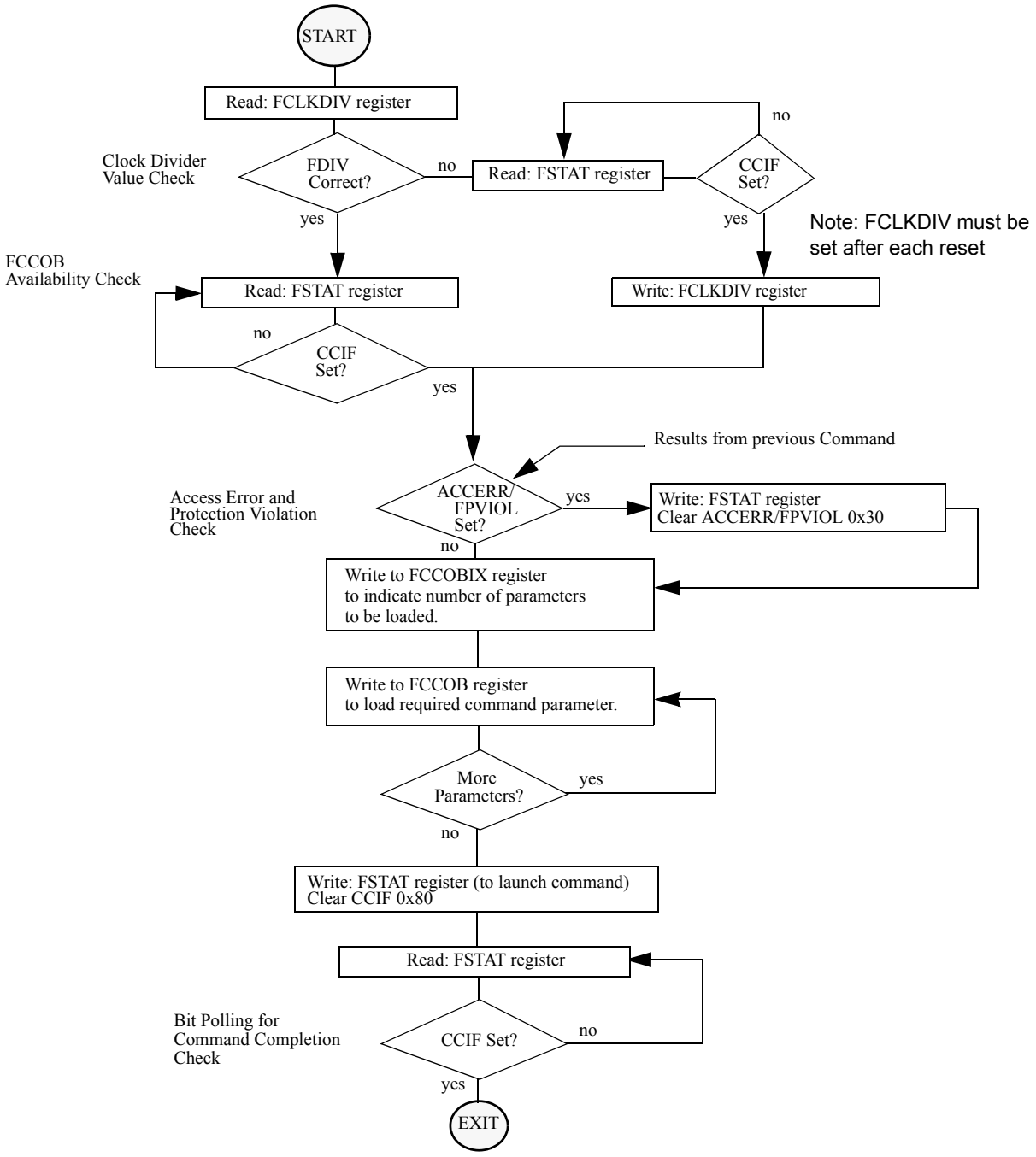


Figure 19-30. Generic Flash Command Write Sequence Flowchart

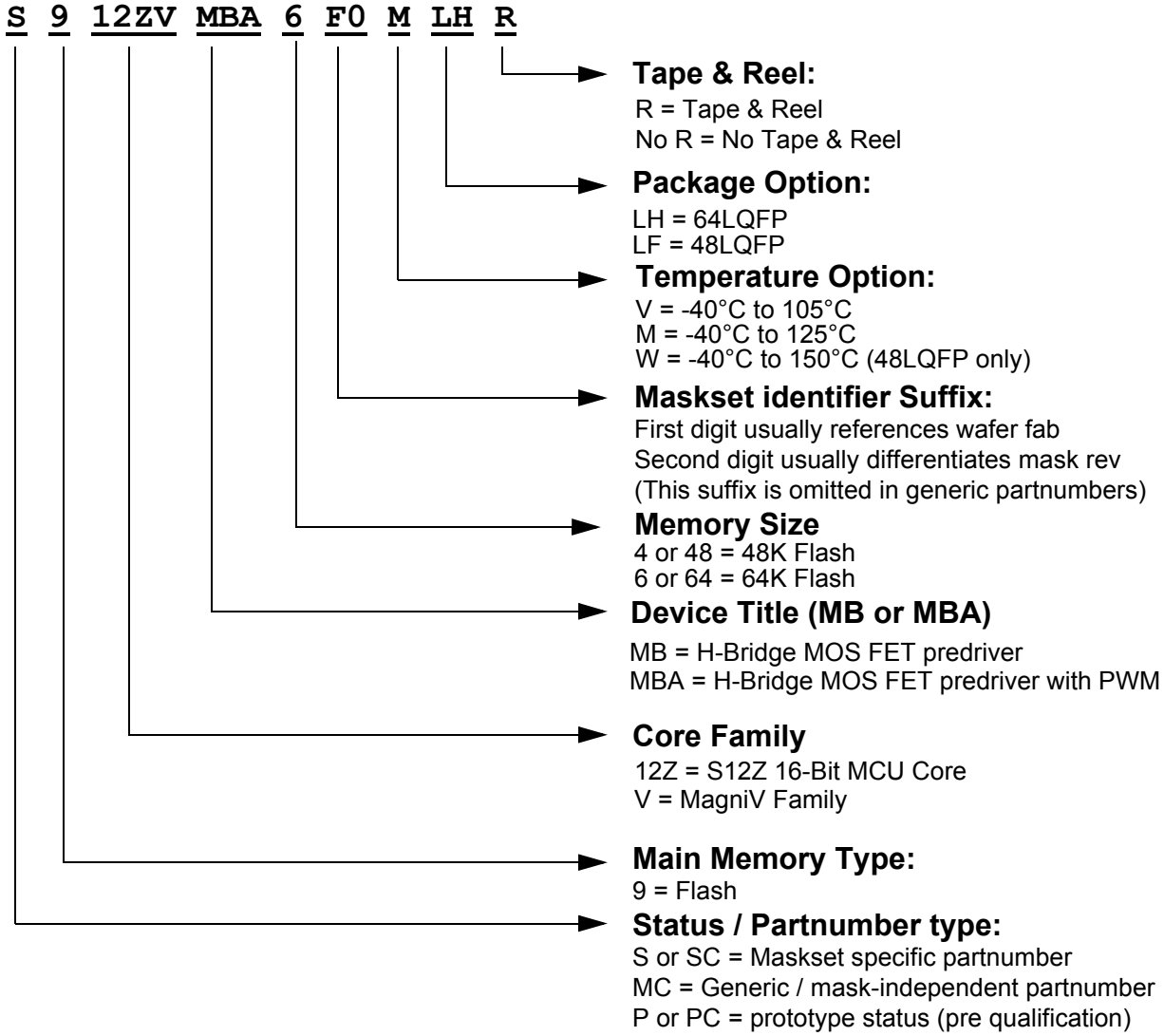
Appendix K
Ordering Information

Customers can choose either the mask-specific partnumber or the generic, mask-independent partnumber. Ordering a mask-specific partnumber enables the customer to specify which particular maskset they receive whereas ordering the generic partnumber means that the currently preferred maskset (which may change over time) is shipped. In either case, the marking on the device always shows the generic, mask-independent partnumber and the mask set number. To order specific partnumbers, please contact your local sales office. The below figure illustrates the structure of a typical mask-specific ordering number.

NOTES

Not every combination is offered. Device overview section lists available derivatives.

The mask identifier suffix and the Tape & Reel suffix are always both omitted from the partnumber which is actually marked on the device.



L.9 0x0500-x053F PMF15B6C

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0523	PMFCNTA	R	PMFCNTA							
		W								
0x0524	PMFMODA	R	0	PMFMODA						
		W								
0x0525	PMFMODA	R	PMFMODA							
		W								
0x0526	PMFDTMA	R	0	0	0	0	PMFDTMA			
		W								
0x0527	PMFDTMA	R	PMFDTMA							
		W								
0x0528	PMFENCB	R	PWMENB	GLDOKB	0	0	0	RSTRTB	LDOKB	PWMRIEB
		W								
0x0529	PMFFQCB	R	LDFQB				HALFB	PRSCB		PWMRFB
		W								
0x052A	PMFCNTB	R	0	PMFCNTB						
		W								
0x052B	PMFCNTB	R	PMFCNTB							
		W								
0x052C	PMFMODB	R	0	PMFMODB						
		W								
0x052D	PMFMODB	R	PMFMODB							
		W								
0x052E	PMFDTMB	R	0	0	0	0	PMFDTMB			
		W								
0x052F	PMFDTMB	R	PMFDTMB							
		W								
0x0530	PMFENCC	R	PWMENC	GLDOKC	0	0	0	RSTRTC	LDOKC	PWMRIEC
		W								
0x0531	PMFFQCC	R	LDFQC				HALFC	PRSCC		PWMRFC
		W								