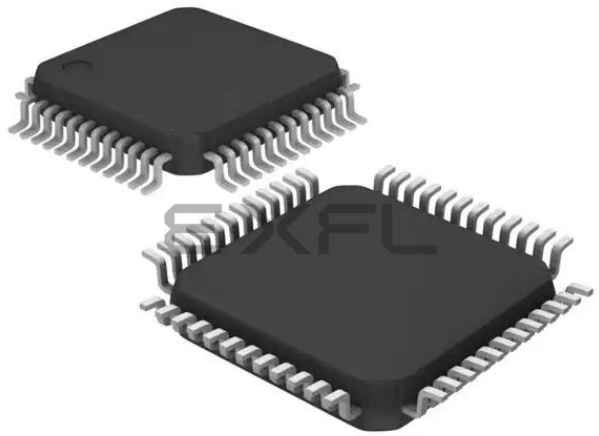

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	15
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmba6f0wlfr

Appendix A
MCU Electrical Specifications

Appendix B
CPMU Electrical Specifications (VREG, OSC, IRC, PLL)

Appendix C
ADC Electrical Specifications

Appendix D
LINPHY Electrical Specifications

Appendix E
GDU Electrical Specifications

Appendix F
HSDRV Electrical Specifications

Appendix G
NVM Electrical Specifications

Appendix H
BATS Electrical Specifications

When BDM is activated, the CPU finishes executing the current instruction. Thereafter only BDC commands can affect CPU register contents until the BDC GO command returns from active BDM to user code or a device reset occurs. When BDM is activated by a breakpoint, the type of breakpoint used determines if BDM becomes active before or after execution of the next instruction.

NOTE

Attempting to activate BDM using a BGND instruction whilst the BDC is disabled, the CPU requires clock cycles for the attempted BGND execution. However BACKGROUND commands issued whilst the BDC is disabled are ignored by the BDC and the CPU execution is not delayed.

5.4.3 Clock Source

The BDC clock source can be mapped to a constant frequency clock source or a PLL based fast clock. The clock source for the BDC is selected by the CLKSW bit as shown in Figure 5-5. The BDC internal clock is named BDCSI clock. If BDCSI clock is mapped to the BDCCLK by CLKSW then the serial interface communication is not affected by bus/core clock frequency changes. If the BDC is mapped to BDCFCLK then the clock is connected to a PLL derived source at device level (typically bus clock), thus can be subject to frequency changes in application. Debugging through frequency changes requires SYNC pulses to re-synchronize. The sources of BDCCLK and BDCFCLK are specified at device level.

BDC accesses of internal device resources always use the device core clock. Thus if the ACK handshake protocol is not enabled, the clock frequency relationship must be taken into account by the host.

When changing the clock source via the CLKSW bit a minimum delay of 150 cycles at the initial clock speed must elapse before a SYNC can be sent. This guarantees that the start of the next BDC command uses the new clock for timing subsequent BDC communications.

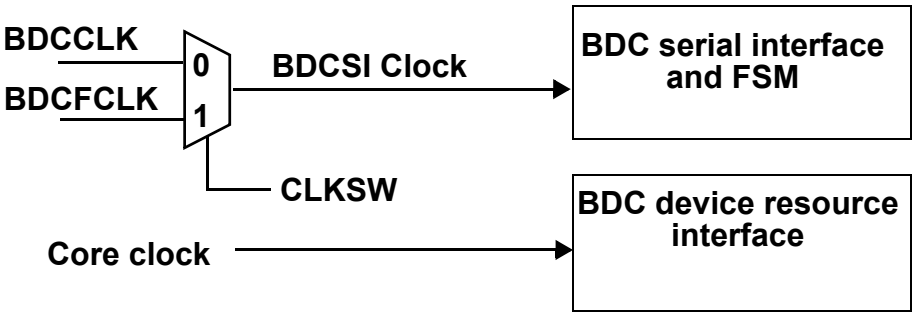


Figure 5-5. Clock Switch

5.4.4 BDC Commands

BDC commands can be classified into three types as shown in Table 5-7.

If the ACK pulse handshake protocol is enabled and STEAL is cleared, then the BDC waits for the first free bus cycle to make a non-intrusive access. If no free bus cycle occurs within 512 core clock cycles then the BDC aborts the access, sets the NORESP bit and uses a long ACK pulse to indicate an error condition to the host.

Table 5-8 summarizes the BDC command set. The subsequent sections describe each command in detail and illustrate the command structure in a series of packets, each consisting of eight bit times starting with a falling edge. The bar across the top of the blocks indicates that the BKGD line idles in the high state. The time for an 8-bit command is 8 × 16 target BDCSI clock cycles.

The nomenclature below is used to describe the structure of the BDC commands. Commands begin with an 8-bit hexadecimal command code in the host-to-target direction (most significant bit first)

```
/       =  separates parts of the command
d       =  delay 16 target BDCSI clock cycles (DLY)
dack    =  delay (16 cycles) no ACK; or delay (=> 32 cycles) then ACK.(DACK)
ad24    =  24-bit memory address in the host-to-target direction
rd8     =  8 bits of read data in the target-to-host direction
rd16    =  16 bits of read data in the target-to-host direction
rd24    =  24 bits of read data in the target-to-host direction
rd32    =  32 bits of read data in the target-to-host direction
rd64    =  64 bits of read data in the target-to-host direction
rd.sz   =  read data, size defined by sz, in the target-to-host direction
wd8     =  8 bits of write data in the host-to-target direction
wd16    =  16 bits of write data in the host-to-target direction
wd32    =  32 bits of write data in the host-to-target direction
wd.sz   =  write data, size defined by sz, in the host-to-target direction
ss      =  the contents of BDCCSRL in the target-to-host direction
sz      =  memory operand size (00 = byte, 01 = word, 10 = long)
           (sz = 11 is reserved and currently defaults to long)
crn     =  core register number, 32-bit data width
WS      =  command suffix signaling the operation is with status
```

Table 5-8. BDC Command Summary

Command Mnemonic	Command Classification	ACK	Command Structure	Description
SYNC	Always Available	N/A	N/A[1]	Request a timed reference pulse to determine the target BDC communication speed
ACK_DISABLE	Always Available	No	0x03/d	Disable the communication handshake. This command does not issue an ACK pulse.
ACK_ENABLE	Always Available	Yes	0x02/dack	Enable the communication handshake. Issues an ACK pulse after the command is executed.
BACKGROUND	Non-Intrusive	Yes	0x04/dack	Halt the CPU if ENBDC is set. Otherwise, ignore as illegal command.

Table 6-30. NDB and MASK bit dependency

NDB	DBGADM	Comment
0	0	Do not compare data bus bit.
0	1	Compare data bus bit. Match on equivalence.
1	0	Do not compare data bus bit.
1	1	Compare data bus bit. Match on difference.

6.4.2.4 Range Comparisons

Range comparisons are accurate to byte boundaries. Thus for data access comparisons a match occurs if at least one byte of the access is in the range (inside range) or outside the range (outside range). For opcode comparisons only the address of the first opcode byte is compared with the range.

When using the AB comparator pair for a range comparison, the data bus can be used for qualification by using the comparator A data and data mask registers. The DBGACTL RW and RWE bits can be used to qualify the range comparison on either a read or a write access. The corresponding DBGBCTL bits are ignored. The DBGACTL COMPE/INST bits are used for range comparisons. The DBGBCTL COMPE/INST bits are ignored in range modes.

6.4.2.4.1 Inside Range (CompA_Addr $\leq$ address $\leq$ CompB_Addr)

In the Inside Range comparator mode, comparator pair A and B can be configured for range comparisons by the control register (DBGC2). The match condition requires a simultaneous valid match for both comparators. A match condition on only one comparator is not valid.

6.4.2.4.2 Outside Range (address < CompA_Addr or address > CompB_Addr)

In the Outside Range comparator mode, comparator pair A and B can be configured for range comparisons. A single match condition on either of the comparators is recognized as valid. Outside range mode in combination with opcode address matches can be used to detect if opcodes are from an unexpected range.

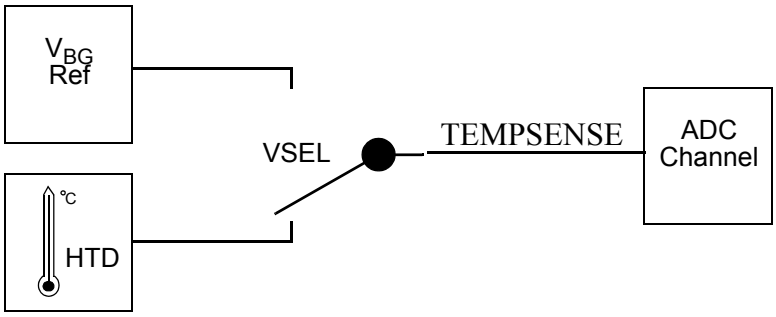
NOTE

When configured for data access matches, an outside range match would typically occur at any interrupt vector fetch or register access. This can be avoided by setting the upper or lower range limit to $FFFFFF or $000000 respectively. Interrupt vector fetches do not cause opcode address matches.

6.4.3 Events

Events are used as qualifiers for a state sequencer change of state. The state control register for the current state determines the next state for each event. An event can immediately initiate a transition to the next state sequencer state whereby the corresponding flag in DBGSR is set.

Figure 8-20. Voltage Access Select



9.3 Key Features

- Programmer's Model with List Based Architecture for conversion command and result value organization
- Selectable resolution of 8-bit, 10-bit,
- Channel select control for n external analog input channels
- Provides up to eight device internal channels (please see the device reference manual for connectivity information and Figure 9-2)
- Programmable sample time
- A sample buffer amplifier for channel sampling (improved performance in view to influence of channel input path resistance versus conversion accuracy)
- Left/right justified result data
- Individual selectable VRH_0/1 and VRL_0/1 inputs (ADC12B_LBA V1 and V2) or VRH_0/1/2 inputs (ADC12B_LBA V3) on a conversion command basis (please see Figure 9-2, Table 9-2)
- Special conversions for selected VRH_0/1 (V1 and V2) or VRH_0/1/2 (V3), VRL_0/1 (V1 and V2) or VRL_0 (V3), (VRL_0/1 + VRH_0/1) / 2 (V1 and V2) or (VRL_0 + VRH_0/1/2) / 2 (V3) (please see Table 9-2)
- 15 conversion interrupts with flexible interrupt organization per conversion result
- One dedicated interrupt for "End Of List" type commands
- Command Sequence List (CSL) with a maximum number of 64 command entries
- Provides conversion sequence abort
- Restart from top of active Command Sequence List (CSL)
- The Command Sequence List and Result Value List are implemented in double buffered manner (two lists in parallel for each function)
- Conversion Command (CSL) loading possible from System RAM or NVM
- Single conversion flow control register with software selectable access path
- Two conversion flow control modes optimized to different application use cases
- Four option bits in the conversion command for top level SoC specific feature/function implementation option (Please refer to the device reference manual for details of the top level feature/function if implemented)

9.5.2.24 ADC Command and Result Offset Register 1 (ADCCROFF1)

It is important to note that these bits do not represent absolute addresses instead it is an sample offset (object size 16bit for RVL, object size 32bit for CSL).

Module Base + 0x0025

	7	6	5	4	3	2	1	0
R	0	CMDRES_OFF1[6:0]						
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-27. ADC Command and Result Offset Register 1 (ADCCROFF1)

Read: Anytime

Write: These bits are writable if bit ADC_EN clear or bit SMOD_ACC set

Table 9-32. ADCCROFF1 Field Descriptions

Field	Description
6-0 CMDRES_OFF1 [6:0]	**ADC Result Address Offset Value** — These bits represent the conversion command and result offset value relative to the conversion command base pointer address and result base pointer address in the memory map to refer to CSL_1 and RVL_1. It is used to calculate the address inside the system RAM to which the result at the end of the current conversion is stored to and the area (RAM or NVM) from which the conversion commands are loaded from. These bits do not represent absolute addresses instead it is an sample offset (object size 16bit for RVL, object size 32bit for CSL).,These bits can only be modified if bit ADC_EN is clear. See also Section 9.6.3.2.2, “Introduction of the two Command Sequence Lists (CSLs) and Section 9.6.3.2.3, “Introduction of the two Result Value Lists (RVLs) for more details.

If measured when

a) V_{HBI1} selected with BVHS = 0
$V_{measure} \geq V_{HBI1\_A}$ (rising edge) or $V_{measure} \geq V_{HBI1\_D}$ (falling edge)

or when

a) V_{HBI2} selected with BVHS = 1
$V_{measure} \geq V_{HBI2\_A}$ (rising edge) or $V_{measure} \geq V_{HBI2\_D}$ (falling edge)

then BVHC is set. BVHC status bit indicates that a high voltage at pin VSUP is present. The High Voltage Interrupt flag (BVHIF) is set to 1 when a Voltage High Condition (BVHC) changes state. The Interrupt flag BVHIF can only be cleared by writing a 1. If the interrupt is enabled by bit BVHIE the module requests an interrupt to MCU (BATI).

Chapter 11
Timer Module (TIM16B4CV3) Block Description

Table 11-1.

V03.02	Apri,12,2010	11.3.2.9/11-378 11.4.3/11-385	-update TCRE bit description
V03.03	Jan,14,2013		-single source generate different channel guide

11.1 Introduction

The basic scalable timer consists of a 16-bit, software-programmable counter driven by a flexible programmable prescaler.

This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform.

This timer could contain up to 4 input capture/output compare channels . The input capture function is used to detect a selected transition edge and record the time. The output compare function is used for generating output signals or for timer software delays.

A full access for the counter registers or the input capture/output compare registers should take place in one clock cycle. Accessing high byte and low byte separately for all of these registers may not yield the same result as accessing them in one word.

11.1.1 Features

The TIM16B4CV3 includes these distinctive features:

- Up to 4 channels available. (refer to device specification for exact number)
- All channels have same input capture/output compare functionality.
- Clock prescaling.
- 16-bit counter.

11.1.2 Modes of Operation

Stop: Timer is off because clocks are stopped.

Freeze: Timer counter keeps on running, unless TSFRZ in TSCR1 is set to 1.

Wait: Counters keeps on running, unless TSWAI in TSCR1 is set to 1.

NOTE

IPOL*x* bits are buffered so only one PWM register is used per PWM cycle. If an IPOL*x* bit changes during a PWM period, the new value does not take effect until the next PWM period.

IPOL*x* bits take effect at the end of each PWM cycle regardless of the state of the related LDOK bit or global load OK.

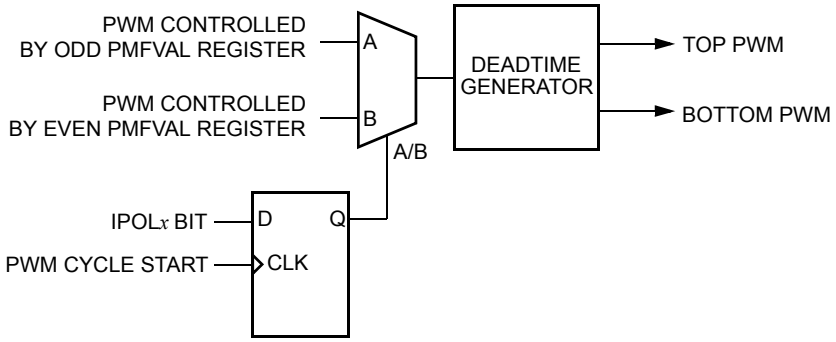


Figure 12-55. Internal Correction Logic when ISENS = 01

To detect the current status, the voltage on each $\overline{IS}$ input is sampled twice in a PWM period, at the end of each deadtime. The value is stored in the DT*n* bits in the PMF Deadtime Sample register (PMFDTMS). The DT*n* bits are a timing marker especially indicating when to toggle between PWM value registers. Software can then set the IPOL*x* bit to toggle PMFVAL registers according to DT*n* values.

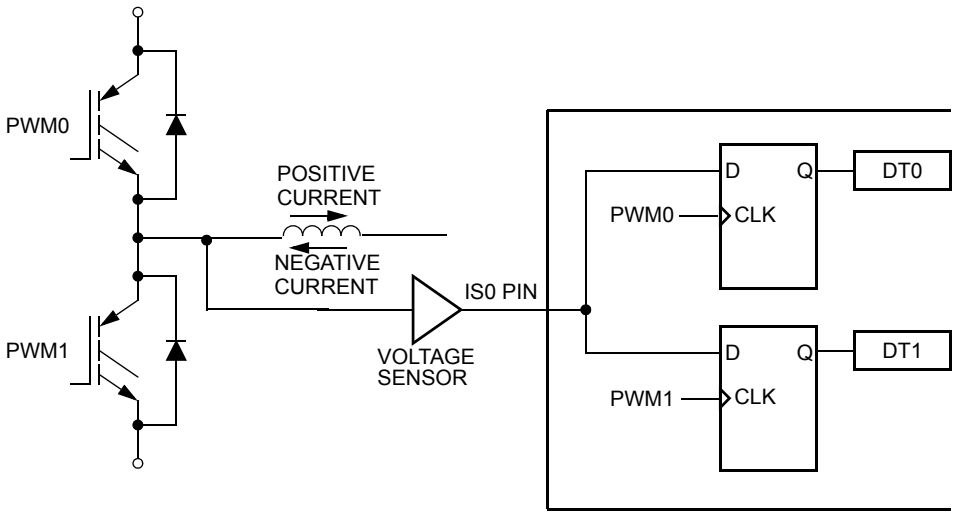


Figure 12-56. Current Status Sense Scheme for Deadtime Correction

Both D flip-flops latch low, DT0 = 0, DT1 = 0, during deadtime periods if current is large and flowing out of the complementary circuit. See Figure 12-56. Both D flip-flops latch the high, DT0 = 1, DT1 = 1, during deadtime periods if current is also large and flowing into the complementary circuit.

However, under low-current, the output voltage of the complementary circuit during deadtime is somewhere between the high and low levels. The current cannot free-wheel through the opposition anti-body diode, regardless of polarity, giving additional distortion when the current crosses zero.

Chapter 13
Programmable Trigger Unit (PTUV3)

Table 13-1. Revision History Table

Rev. No. (Item No.)	Data	Sections Affected	Substantial Change(s)
3.0	16. Jul. 2013		- removed second TG

Table 13-2. Terminology

Term	Meaning
TG	Trigger Generator
EOL	End of trigger list

13.1 Introduction

In PWM driven systems it is important to schedule the acquisition of the state variables with respect to PWM cycle.

The Programmable Trigger Unit (PTU) is intended to completely avoid CPU involvement in the time acquisitions of state variables during the control cycle that can be half, full, multiple PWM cycles.

All acquisition time values are stored inside the global memory map, basically inside the system memory; see the MMC section for the supported memory area. In such cases the pre-setting of the acquisition times needs to be completed during the previous control cycle to where the actual acquisitions are to be made.

13.1.1 Features

The PTU module includes these distinctive features:

- One 16 bit counter as time base for all trigger events
- One trigger generator(TG0)
- Up to 32 trigger events per trigger generator
- Global Load OK support, to guarantee coherent update of all control loop modules
- Trigger values stored inside the global memory map, basically inside system memory
- Software generated reload event and Trigger event generation for debugging

13.1.2 Modes of Operation

The PTU module behaves as follows in the system power modes:

1. Run mode
   All PTU features are available.

If enabled (TG0EIE is set) an interrupt will be generated.

13.4.5.6 Trigger Generator Done

The trigger generator done flag (TG0DIF) is set if the loaded trigger value contains 0x0000 or if the number of maximum trigger events (32) was reached. Please note, that the time which is required to load the next trigger value defines the delay between the generation of the last trigger and the assertion of the done flag. If enabled (TG0DIE is set) an interrupt is generated.If the trigger value loaded from the memory contains double bit ECC errors (PTUDEEF flag is set) then the data are ignored and the trigger generator done flag (TG0DIF) is not set.

13.4.6 Debugging

To see the internal status of the trigger generator the register TG0LIST, TG0TNUM, and TG0TV can be used. The TG0LIST register shows the number of currently used list. The TG0TNUM shows the number of generated triggers since the last reload event. If the maximum number of triggers was generated then this register shows zero. The trigger value loaded from the memory to generate the next trigger event is visible inside the TG0TV register. If the execution of the trigger list is done then these registers are unchanged until the next reload event. The next PWM reload event clears the TG0TNUM register and toggles the used trigger list if PTULDOK was set.

To generate a reload event or trigger event independent from the PWM status the debug register bits PTUFRE or TG0FTE can be used. A write one to this bits will generate the associated event. This behavior is not available during stop or freeze mode.

Table 15-2. SPICR1 Field Descriptions (continued)

Field	Description
2 CPHA	**SPI Clock Phase Bit** — This bit is used to select the SPI clock format. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Sampling of data occurs at odd edges (1,3,5,...) of the SCK clock. 1 Sampling of data occurs at even edges (2,4,6,...) of the SCK clock.
1 SSOE	**Slave Select Output Enable** — The $\overline{SS}$ output feature is enabled only in master mode, if MODFEN is set, by asserting the SSOE as shown in Table 15-3. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.
0 LSBFE	**LSB-First Enable** — This bit does not affect the position of the MSB and LSB in the data register. Reads and writes of the data register always have the MSB in the highest bit position. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Data is transferred most significant bit first. 1 Data is transferred least significant bit first.

Table 15-3. $\overline{SS}$ Input / Output Selection

MODFEN	SSOE	Master Mode	Slave Mode
0	0	$\overline{SS}$ not used by SPI	$\overline{SS}$ input
0	1	$\overline{SS}$ not used by SPI	$\overline{SS}$ input
1	0	$\overline{SS}$ input with MODF feature	$\overline{SS}$ input
1	1	$\overline{SS}$ is slave select output	$\overline{SS}$ input

15.3.2.2 SPI Control Register 2 (SPICR2)

Module Base +0x0001

	7	6	5	4	3	2	1	0
R	0	XFRW	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-4. SPI Control Register 2 (SPICR2)

Read: Anytime

Write: Anytime; writes to the reserved bits have no effect

17.2.1 LIN — LIN Bus Pin

This pad is connected to the single-wire LIN data bus.

17.2.2 LGND — LIN Ground Pin

This pin is the device LIN ground connection. It is used to sink currents related to the LIN Bus pin. A de-coupling capacitor external to the device (typically 220 pF, X7R ceramic) between LIN and LGND can further improve the quality of this ground and filter noise.

17.2.3 VLINSUP — Positive Power Supply

External power supply to the chip. The VLINSUP supply mapping is described in device level documentation.

17.2.4 LPTxD — LIN Transmit Pin

This pin can be routed to the SCI, LPDR1 register bit, an external pin, or other options. Please refer to the PIM chapter of the device specification for the available routing options.

This input is only used in normal mode; in other modes the value of this pin is ignored.

17.2.5 LPRxD — LIN Receive Pin

This pin can be routed to the SCI, an external pin, or other options. Please refer to the PIM chapter of the device specification for the available routing options.

In standby mode this output is disabled, and sends only a short pulse in case the wake-up functionality is enabled and a valid wake-up pulse was received in the LIN Bus.

17.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the LIN Physical Layer.

17.3.1 Module Memory Map

A summary of the registers associated with the LIN Physical Layer module is shown in Table 17-2. Detailed descriptions of the registers and bits are given in the subsections that follow.

NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Table 19-36. Erase Verify Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if an invalid global address [23:0] is supplied see Table 19-3)
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

19.4.7.3 Erase Verify P-Flash Section Command

The Erase Verify P-Flash Section command will verify that a section of code in the P-Flash memory is erased. The Erase Verify P-Flash Section command defines the starting point of the code to be verified and the number of phrases.

Table 19-37. Erase Verify P-Flash Section Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x03	Global address [23:16] of a P-Flash block
FCCOB1	Global address [15:0] of the first phrase to be verified	
FCCOB2	Number of phrases to be verified	

Upon clearing CCIF to launch the Erase Verify P-Flash Section command, the Memory Controller will verify the selected section of Flash memory is erased. The CCIF flag will set after the Erase Verify P-Flash Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 19-38. Erase Verify P-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 19-29)
		Set if an invalid global address [23:0] is supplied see Table 19-3)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
		Set if the requested section crosses a the P-Flash address boundary
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

A.1.6 Recommended capacitor values

Table A-5. Recommended capacitor values (nominal component values)

Num	Characteristic	Symbol	Typical	Unit
1	VDDX decoupling capacitor (1)	C_{VDDX1}	100-220	nF
2	VDDA decoupling capacitor 1	C_{VDDA}	100-220	nF
3	VDDX stability capacitor (2) (3)	C_{VDD5}	4.7-10	μF
4	VLS decoupling capacitor 1	C_{VLS}	100-220	nF
5	VLS stability capacitor 2 (4)	C_{VLS}	4.7-10	μF
6	LIN decoupling capacitor 1	C_{LIN}	220	pF

1. X7R ceramic
2. 4.7μF ceramic or 10μF tantalum
3. Can be placed anywhere on the 5V supply node (VDDA, VDDX)
4. Can be placed anywhere on the VLS node

A.1.7 Operating conditions

This section describes the operating conditions of the device. Unless otherwise noted these conditions apply to the following electrical parameters.

Appendix J
Package Information

J.1 64LQFP Package Mechanical Information

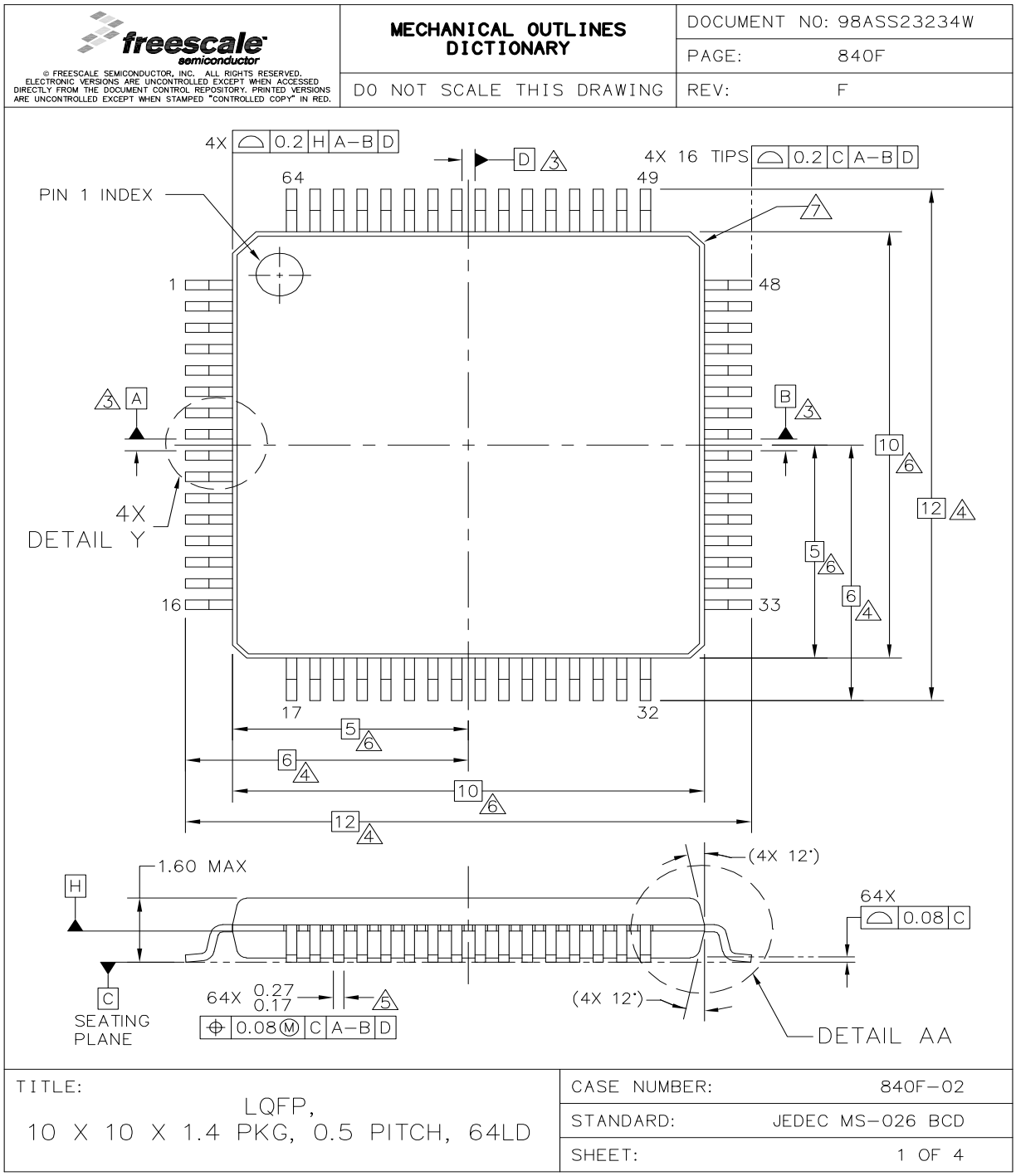


Figure J-1. 64LQFP Mechanical Information (1 of 3)

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x02F7	PIFP	R	0	0	0	0	0	0	PIFP1	PIFP0
		W								
0x02F8	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02F9	OCPEP	R	0	0	0	0	0	0	0	OCPEP0
		W								
0x02FA	OCIEP	R	0	0	0	0	0	0	0	OCIEP0
		W								
0x02FB	OCIFP	R	0	0	0	0	0	0	0	OCIFP0
		W								
0x02FC	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02FD	RDRP	R	0	0	0	0	0	0	0	RDRP0
		W								
0x02FE–0x02FF	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0300–0x032F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0330	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0331	PTIL	R	0	0	0	0	0	PTIL2	PTIL1	PTIL0
		W								
0x0332	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0333	PTPSL	R	0	0	0	0	0	PTPSL2	PTPSL1	PTPSL0
		W								
0x0334	PPSL	R	0	0	0	0	0	PPSL2	PPSL1	PPSL0
		W								
0x0335	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0336	PIEL	R	0	0	0	0	0	PIEL2	PIEL1	PIEL0
		W								

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0594	TG0L0IDX	R	0	TG0L10DX[6:0]						
		W								
0x0595	TG0L1IDX	R	0	TG0L1IDX[6:0]						
		W								
0x0596 - 0x059E	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x059F	PTUDEBUG	R	0	PTUREPE	0	PTUT0PE	0	0	0	0
		W						PTUFRE		TG0FTE

L.11 0x05C0-0x05EF TIM0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x05C0	TIM0TIOS	R					IOS3	IOS2	IOS1	IOS0
		W								
0x05C1	TIM0CFORC	R	0	0	0	0	0	0	0	0
		W					FOC3	FOC2	FOC1	FOC0
0x05C2	Reserved	R								
		W								
0x05C3	Reserved	R								
		W								
0x05C4	TIM0TCNTH	R	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
		W								
0x05C5	TIM0TCNTL	R	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
		W								
0x05C6	TIM0TSCR1	R	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
		W								
0x05C7	TIM0TTOV	R					TOV3	TOV2	TOV1	TOV0
		W								
0x05C8	Reserved	R								
		W								
0x05C9	TIM0TCTL2	R	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
		W								
0x05CA	Reserved	R								
		W								
0x05CB	TIM0TCTL4	R	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
		W								

L.13 0x06A0-0x06BF GDU

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x06A3	GDUDSE	R	0	0	GDHSIF[1:0]		0	0	GDLSIF[1:0]	
		W								
0x06A4	GDUSTAT	R	0	GPHS[1:0]		0	GOCS0	0	GHHDS	GLVLSS
		W								
0x06A5	GDUSRC	R	0	GSRCHS[2:0]			0	GSRCLS[2:0]		
		W								
0x06A6	GDUF	R	GSUF	GHHDF	GLVLSF	0	GOCIF0	0	GHHDIF	GLVLSIF
		W								
0x06A7-0x06A8	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x06A9	GDUPHMUX	R	0	0	0	0	0	0	GPHMX[1:0]	
		W								
0x06AA	GDUCSO	R	0	0	0	0	0	GCSO0[2:0]		
		W								
0x06AB	GDUDSLVL	R	GDSFHS	GDSLHS[2:0]			GDSFLS	GDSLLS[2:0]		
		W								
0x06AC	GDUPHL	R	0	0	0	0	0	0	GPHL[1:0]	
		W								
0x06AD	GDUCLK2	R	0	0	0	0	GCPCD[3:0]			
		W								
0x06AE	GDUOC0	R	GOCA0	GOCE0	0	GOCT0[4:0]				
		W								
0x06AF	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x06B0	GDUCTR1	R	0	0	0	0	0	GBSWOFF[1:0]		TDEL
		W								
0x06B1-0x06BF	Reserved	R	0	0	0	0	0	0	0	0
		W								