Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 16
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5602pef0vll6r

Table of Contents

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between three master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master completes its transactions. Requesting masters will be treated with equal priority and will be granted access a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- 3 master ports:
  - e200z0 core complex instruction port
  - e200z0 core complex Load/Store Data port
  - eDMA
- 3 slave ports:
  - Flash memory (Code and Data)
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 32-bit internal data paths
- Fixed Priority Arbitration based on Port Master
- Temporary dynamic priority elevation of masters

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels.

The eDMA module provides the following features:

- 16 channels support independent 8-, 16- or 32-bit single value or block transfers
- Supports variable-sized queues and circular queues
- Source and destination address registers are independently configured to either post-increment or to remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, DSPIs, ADC, FlexPWM, eTimer and CTU
- Programmable DMA channel multiplexer allows assignment of any DMA source to any available DMA channel with as many as 30 request sources
- eDMA abort operation through software

1.5.4 Flash memory

The MPC5602P provides 320 KB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash memory module is interfaced to the system bus by a dedicated flash memory controller. It supports a 32-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit wide prefetch buffers. Prefetch buffer hits allow no-wait responses. Normal flash memory array accesses are registered and are forwarded to the system bus on the following cycle, incurring two wait-states.

lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol (PCP) for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the same resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority: modifying the priority can be used to implement the priority ceiling protocol for accessing shared resources.
- 1 external high priority interrupt (NMI) directly accessing the main core and I/O processor (IOP) critical interrupt mechanism

1.5.7 System status and configuration module (SSCM)

The system status and configuration module (SSCM) provides central device functionality.

The SSCM includes these features:

- System configuration and status
  - Memory sizes/status
  - Device mode and security status
  - Determine boot vector
  - Search code flash for bootable sector
  - DMA status
- Debug status port enable and selection
- Bus and peripheral abort enable/disable

1.5.8 System clocks and clock generation

The following list summarizes the system clock and clock generation on the MPC5602P:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider (÷1, ÷2, ÷4, ÷8)
- FlexPWM module and eTimer module running at the same frequency as the e200z0h core
- Internal 16 MHz RC oscillator for rapid start-up and safe mode: supports frequency trimming by user application

1.5.9 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4–40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

The FMPLL has the following major features:

- Input clock frequency: 4–40 MHz
- Maximum output frequency: 64 MHz
- Voltage controlled oscillator (VCO)—frequency 256–512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the FMPLL to relock

- LIN slave mode features:
  - Autonomous LIN header handling
  - Autonomous LIN response handling
  - Optional discarding of irrelevant LIN responses using ID filter
- UART mode:
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
  - Parity, Noise and Framing errors
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods

1.5.23 Deserial serial peripheral interface (DSPI)

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the MPC5602P MCU and external devices.

The DSPI modules provide these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- Up to 8 chip select lines available:
  - 8 on DSPI_0
  - 4 each on DSPI_1 and DSPI_2
- 8 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering up to 4 transfers on the transmit and receive side
- Queueing operation possible through use of the I/O processor or eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.24 Pulse width modulator (FlexPWM)

The pulse width modulator module (PWM) contains four PWM submodules each of which is set up to control a single half-bridge power stage. There are also three fault channels.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), permanent magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

The FlexPWM block implements the following features:

- 16-bit resolution for center, edge-aligned, and asymmetrical PWMs

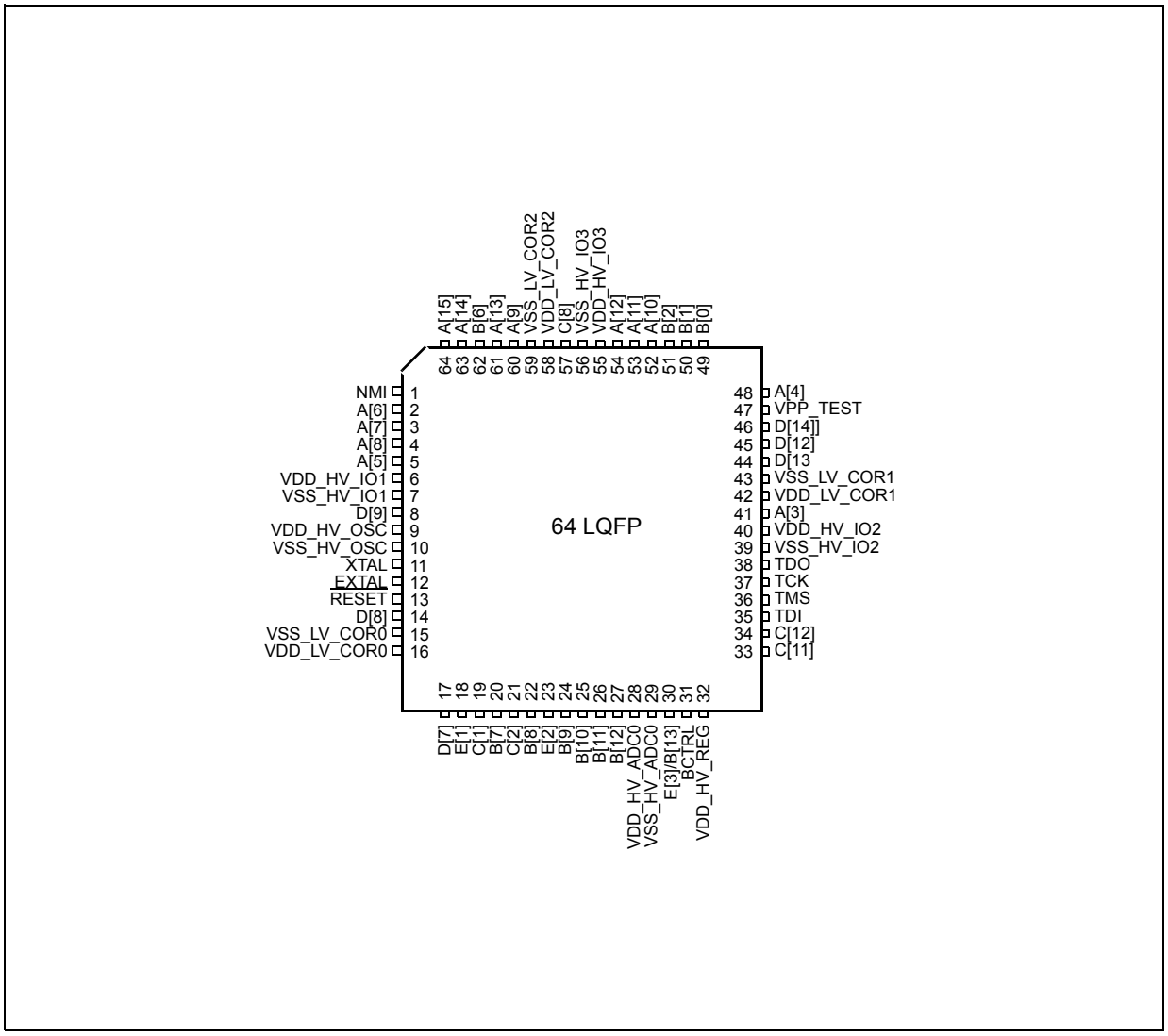

Figure 2. 64-pin LQFP pinout(top view)

Table 5. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	GPIO[52] — — B[3]	SIUL — — FlexPWM_0	I/O — — O	Slow	Medium	—	90
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] CS3 F[0] —	SIUL DSPI_0 FCU_0 —	I/O O O —	Slow	Medium	—	22
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3 —	GPIO[54] CS2 — — FAULT[1]	SIUL DSPI_0 — — FlexPWM_0	I/O O — — I	Slow	Medium	—	23
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3	GPIO[55] CS3 F[1] CS4	SIUL DSPI_1 FCU_0 DSPI_0	I/O O O O	Slow	Medium	17	26
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3	GPIO[56] CS2 — CS5	SIUL DSPI_1 — DSPI_0	I/O O — O	Slow	Medium	14	21
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] X[0] TXD —	SIUL FlexPWM_0 LIN_1 —	I/O O O —	Slow	Medium	8	15
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] A[0] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	53
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] B[0] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	54
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] X[1] — — RXD	SIUL FlexPWM_0 — — LIN_1	I/O O — — I	Slow	Medium	45	70
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] A[1] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	44	67
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3	GPIO[62] B[1] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	46	73

3.5 Thermal characteristics

3.5.1 Package thermal characteristics

Table 10. LQFP thermal characteristics

Symbol	Parameter	Conditions	Typical value		Unit
			100-pin	64-pin	
$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection[1]	Single layer board—1s	63	57	°C/W
		Four layer board—2s2p	51	41	°C/W
$R_{\theta JB}$	Thermal resistance junction-to-board[2]	Four layer board—2s2p	33	22	°C/W
$R_{\theta JCtop}$	Thermal resistance junction-to-case (top)[3]	Single layer board—1s	15	13	°C/W
Ψ_{JB}	Junction-to-board, natural convection[4]	Operating conditions	33	22	°C/W
Ψ_{JC}	Junction-to-case, natural convection[5]	Operating conditions	1	1	°C/W

1 Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.

2 Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as RthJB or Theta-JB.

3 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.2 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in Equation 2 as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

NOTE

The voltage regulator output cannot be used to drive external circuits. Output pins are to be used only for decoupling capacitance.

$V_{DD\_LV\_COR}$ must be generated using internal regulator and external NPN transistor. It is not possible to provide $V_{DD\_LV\_COR}$ through external regulator.

For the MPC5602P microcontroller, capacitor(s), with total values not below C_{DEC1}, should be placed between $V_{DD\_LV\_CORx}/V_{SS\_LV\_CORx}$ close to external ballast transistor emitter. 4 capacitors, with total values not below C_{DEC2}, should be placed close to microcontroller pins between each $V_{DD\_LV\_CORx}/V_{SS\_LV\_CORx}$ supply pairs and the $V_{DD\_LV\_REGCOR}/V_{SS\_LV\_REGCOR}$ pair . Additionally, capacitor(s) with total values not below C_{DEC3}, should be placed between the $V_{DD\_HV\_REG}/V_{SS\_HV\_REG}$ pins close to ballast collector. Capacitors values have to take into account capacitor accuracy, aging and variation versus temperature.

All reported information are valid for voltage and temperature ranges described in recommended operating condition, Table 8 and Table 9.

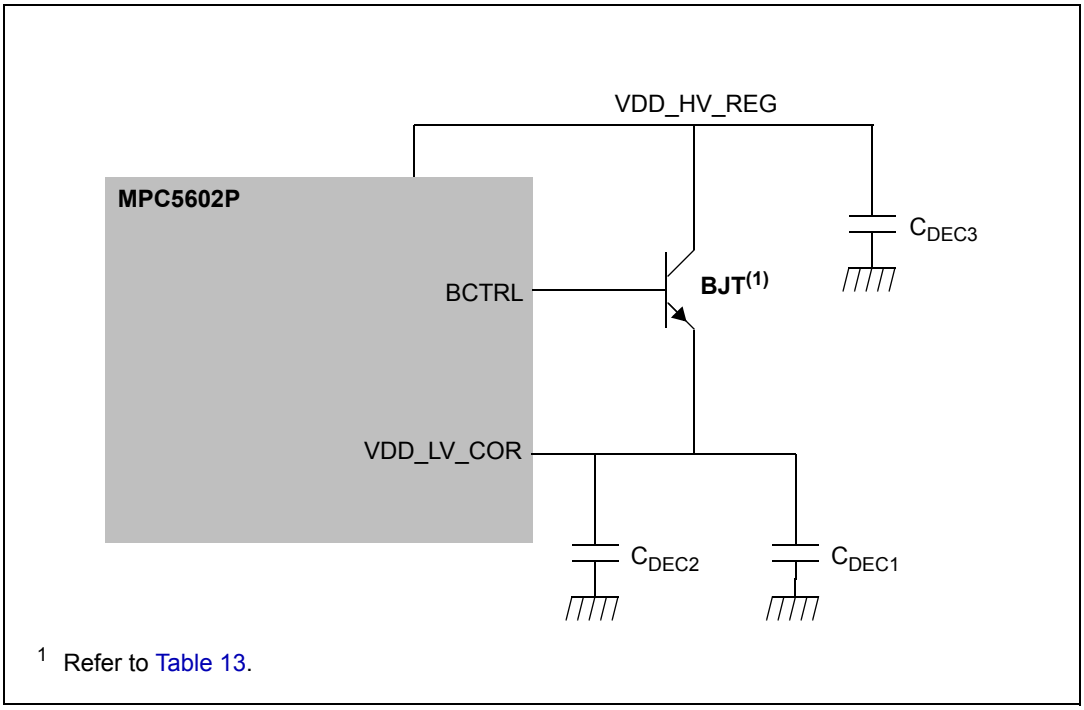

Figure 8. Voltage regulator configuration

Table 13. Approved NPN ballast components

Part	Manufacturer	Approved derivatives[1]
BCP68	ON Semi	BCP68
	NXP	BCP68-25
	Infineon	BCP68-25
BCX68	Infineon	BCX68-10; BCX68-16; BCX-25
BC868	NXP	BC868

- LVDLVCOR monitors low voltage digital power domain

Table 15. Low voltage monitor electrical characteristics

Symbol	C	Parameter	Conditions[1]	Value		Unit
				Min	Max	
V_{PORH}	T	Power-on reset threshold	—	1.5	2.7	V
V_{PORUP}	P	Supply for functional POR module	T_A = 25 °C	1.0	—	V
$V_{REGLVDMOK\_H}$	P	Regulator low voltage detector high threshold	—	—	2.95	V
$V_{REGLVDMOK\_L}$	P	Regulator low voltage detector low threshold	—	2.6	—	V
$V_{FLLVDMOK\_H}$	P	Flash low voltage detector high threshold	—	—	2.95	V
$V_{FLLVDMOK\_L}$	P	Flash low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDMOK\_H}$	P	I/O low voltage detector high threshold	—	—	2.95	V
$V_{IOLVDMOK\_L}$	P	I/O low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDM5OK\_H}$	P	I/O 5 V low voltage detector high threshold	—	—	4.4	V
$V_{IOLVDM5OK\_L}$	P	I/O 5 V low voltage detector low threshold	—	3.8	—	V
$V_{MLVDDOK\_H}$	P	Digital supply low voltage detector high	—	—	1.145	V
$V_{MLVDDOK\_L}$	P	Digital supply low voltage detector low	—	1.08	—	V

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified

3.9 Power up/down sequencing

To prevent an overstress event or a malfunction within and outside the device, the MPC5602P implements the following sequence to ensure each module is started only when all conditions for switching it ON are available:

- A POWER_ON module working on voltage regulator supply controls the correct start-up of the regulator. This is a key module ensuring safe configuration for all voltage regulator functionality when supply is below 1.5 V. Associated POWER_ON (or POR) signal is active low.
- Several low voltage detectors, working on voltage regulator supply monitor the voltage of the critical modules (voltage regulator, I/Os, flash memory and low voltage domain). LVDs are gated low when POWER_ON is active.
- A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, flash memory and 16 MHz RC oscillator needed during power-up phase and reset phase. When POWER_OK is low the associated modules are set into a safe state.

Table 18. Supply current (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	C	Parameter		Conditions		Value[1]		Unit
						Typ	Max	
$I_{DD\_LV\_CORx}$	T	Supply current	RUN—Maximum mode[2]	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	40 MHz	44	55	mA
	P				64 MHz	52	65	
	T		RUN—Typical mode[3]		40 MHz	38	46	
					64 MHz	45	54	
	P		HALT mode[4]		—	1.5	10	
			STOP mode[5]		—	1	10	
I_{DD_FLASH}	T		Flash during read	$V_{DD\_HV\_FL}$ at 5.0 V	—	8	10	
			Flash during erase operation on 1 flash module	$V_{DD\_HV\_FL}$ at 5.0 V	—	15	19	
I_{DD_ADC}	T		ADC	$V_{DD\_HV\_ADC0}$ at 5.0 V f_{ADC} = 16 MHz	ADC_0	3	4	
I_{DD_OSC}	T		Oscillator	$V_{DD\_HV\_OSC}$ at 5.0 V	8 MHz	2.6	3.2	
$I_{DD\_HV\_REG}$	D		Internal regulator module current consumption	$V_{DD\_HV\_REG}$ at 5.5 V		—	10	

1 All values to be confirmed after characterization/data collection.

2 Maximum mode: FlexPWM, ADC, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, PLL_0 enabled, 125 °C ambient. I/O supply current excluded.

3 Typical mode configurations: DSPI, LINFlex, FlexCAN, 15 output pins, PLL_0, 105 °C ambient. I/O supply current excluded.

4 Halt mode configurations: Code fetched from SRAM, code flash memory and data flash memory in low power mode, OSC/PLL_0 are OFF, core clock frozen, all peripherals disabled.

5 STOP “P” mode Device Under Test (DUT) configuration: Code fetched from SRAM, code flash memory and data flash memory off, OSC/PLL_0 are OFF, core clock frozen, all peripherals disabled.

to ground. For instance, assuming a conversion rate of 1 MHz, with C_S+C_{P2} equal to 3 pF, a resistance of 330 kΩ is obtained (R_{EQ} = 1 / (fc × (C_S+C_{P2})), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S+C_{P2}) and the sum of R_S + R_F, the external circuit must be designed to respect the Equation 4:

Eqn. 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on resistive path.

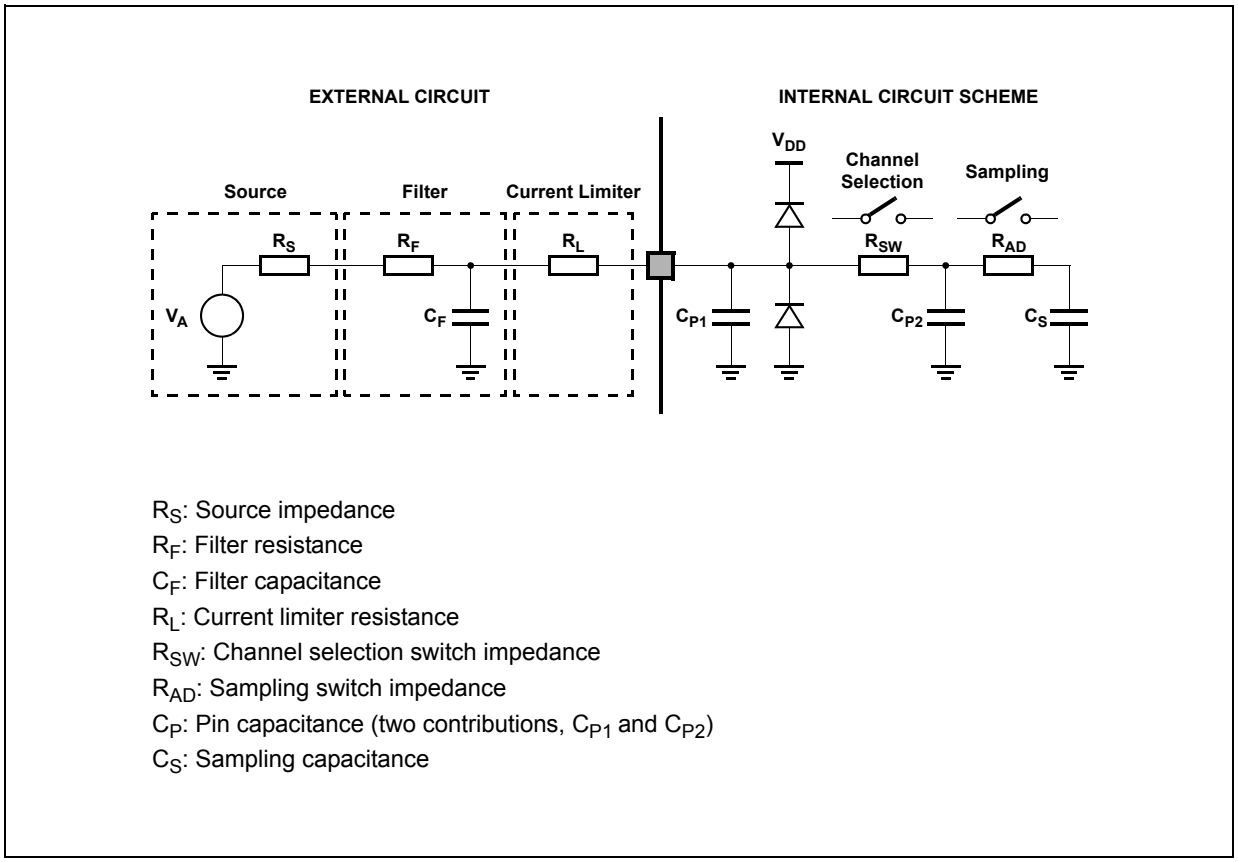

Figure 14. Input equivalent circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 14): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch closed).

3.14.2 ADC conversion characteristics

Table 28. ADC conversion characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{CK}	SR	—	ADC clock frequency (depends on ADC configuration) (The duty cycle depends on ADC clock[2] frequency)	—	3[3]	—	60	MHz
f_s	SR	—	Sampling frequency	—	—	—	1.53	MHz
t_s	—	D	Sampling time[4]	f_{ADC} = 20 MHz, INPSAMP = 3	125	—	—	ns
				f_{ADC} = 9 MHz, INPSAMP = 255	—	—	28.2	µs
t_c	—	P	Conversion time[5]	f_{ADC} = 20 MHz[6], INPCMP = 1	0.650	—	—	µs
t_{ADC_PU}	SR	—	ADC power-up delay (time needed for ADC to settle exiting from software power down; PWDN bit = 0)	—	—	—	1.5	µs
C_S[7]	—	D	ADC input sampling capacitance	—	—	—	2.5	pF
C_{P1}[7]	—	D	ADC input pin capacitance 1	—	—	—	3	pF
C_{P2}[7]	—	D	ADC input pin capacitance 2	—	—	—	1	pF
R_{SW}[7]	—	D	Internal resistance of analog source	$V_{DD\_HV\_ADC0}$ = 5 V ± 10%	—	—	0.6	kΩ
				$V_{DD\_HV\_ADC0}$ = 3.3 V ± 10%	—	—	3	kΩ
R_{AD}[7]	—	D	Internal resistance of analog source	—	—	—	2	kΩ
I_{INJ}	—	T	Input current injection	Current injection on one ADC input, different from the converted one. Remains within TUE specification	–5	—	5	mA
INL	CC	P	Integral non-linearity	No overload	–1.5	—	1.5	LSB
DNL	CC	P	Differential non-linearity	No overload	–1.0	—	1.0	LSB
E_O	CC	T	Offset error	—	—	±1	—	LSB
E_G	CC	T	Gain error	—	—	±1	—	LSB
TUE	CC	P	Total unadjusted error without current injection	—	–2.5	—	2.5	LSB
TUE	CC	T	Total unadjusted error with current injection	—	–3	—	3	LSB

1 V_{DD} = 3.3 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified and analog input voltage from $V_{SS\_HV\_ADC0}$ to $V_{DD\_HV\_ADC0}$.

2 AD_clk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.

3 When configured to allow 60 MHz ADC, the minimum ADC clock speed is 9 MHz, below which the precision is lost.

4 During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_s. After the end of the sampling time t_s, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_s depend on programming.

5 This parameter includes the sampling time t_s.

Table 30. Flash memory module life

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100,000	—	cycles
P/E	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10,000	100,000	cycles
P/E	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1,000	100,000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0–1,000 P/E cycles	20	—	years
			Blocks with 10,000 P/E cycles	10	—	years
			Blocks with 100,000 P/E cycles	5	—	years

1 Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

Table 31. Flash memory read access timing

Symbol	C	Parameter	Conditions[1]	Max value	Unit
f_{max}	C	Maximum working frequency for code flash memory at given number of wait states in worst conditions	2 wait states	66	MHz
			0 wait states	18	
f_{max}	C	Maximum working frequency for data flash memory at given number of wait states in worst conditions	8 wait states	66	MHz

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

3.15.2 Flash memory power supply DC characteristics

Table 32 shows the power supply DC characteristics on external supply.

Table 32. Flash memory power supply DC electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{FLPW}	CC	D	Sum of the current consumption on $V_{DD\_HV\_IOx}$ and $V_{DD\_LV\_CORx}$ during low-power mode	Code flash memory	—	—	900	µA
I_{FPWD}	CC	D	Sum of the current consumption on $V_{DD\_HV\_IOx}$ and $V_{DD\_LV\_CORx}$ during power-down mode	Code flash memory	—	—	150	µA
				Data flash memory	—	—	150	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

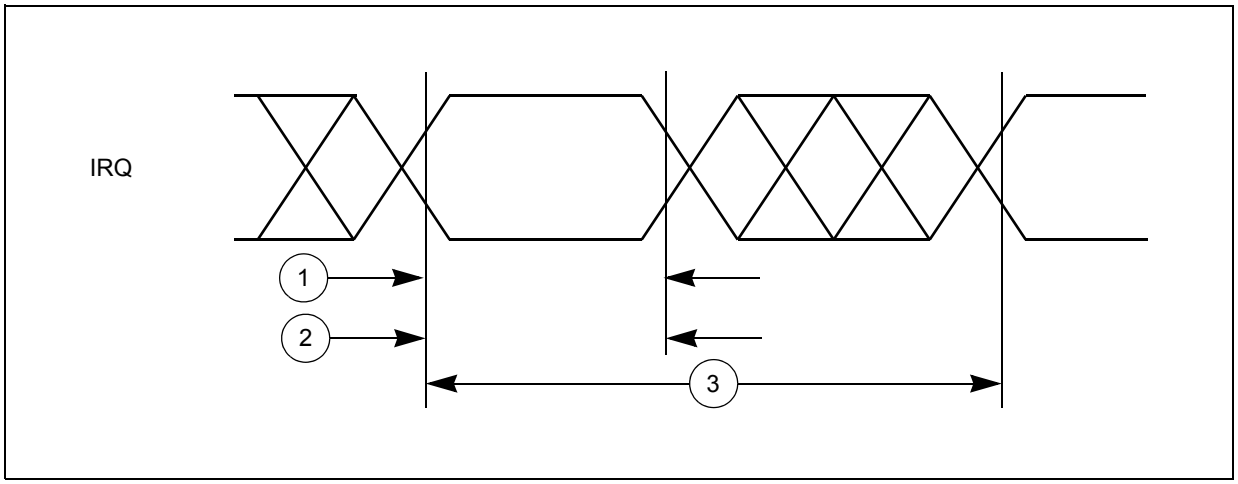

Figure 26. External interrupt timing

3.17.5 DSPI timing

Table 39. DSPI timing[1]

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{SCK}	CC	D	DSPI cycle time	Master (MTFE = 0)	60	—	ns
					Slave (MTFE = 0)	60	—	
2	t_{CSC}	CC	D	CS to SCK delay	—	16	—	ns
3	t_{ASC}	CC	D	After SCK delay	—	26	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	—	0.4 * t_{SCK}	0.6 * t_{SCK}	ns
5	t_A	CC	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	30	ns
6	t_{DIS}	CC	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT high impedance or invalid	—	16	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	CC	D	Data setup time for inputs	Master (MTFE = 0)	35	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	35	—	
					Master (MTFE = 1, CPHA = 1)	35	—	
10	t_{HI}	CC	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	11	—	
					Master (MTFE = 1, CPHA = 1)	–5	—	

4 Package characteristics

4.1 Package mechanical data

4.1.1 100 LQFP mechanical outline drawing

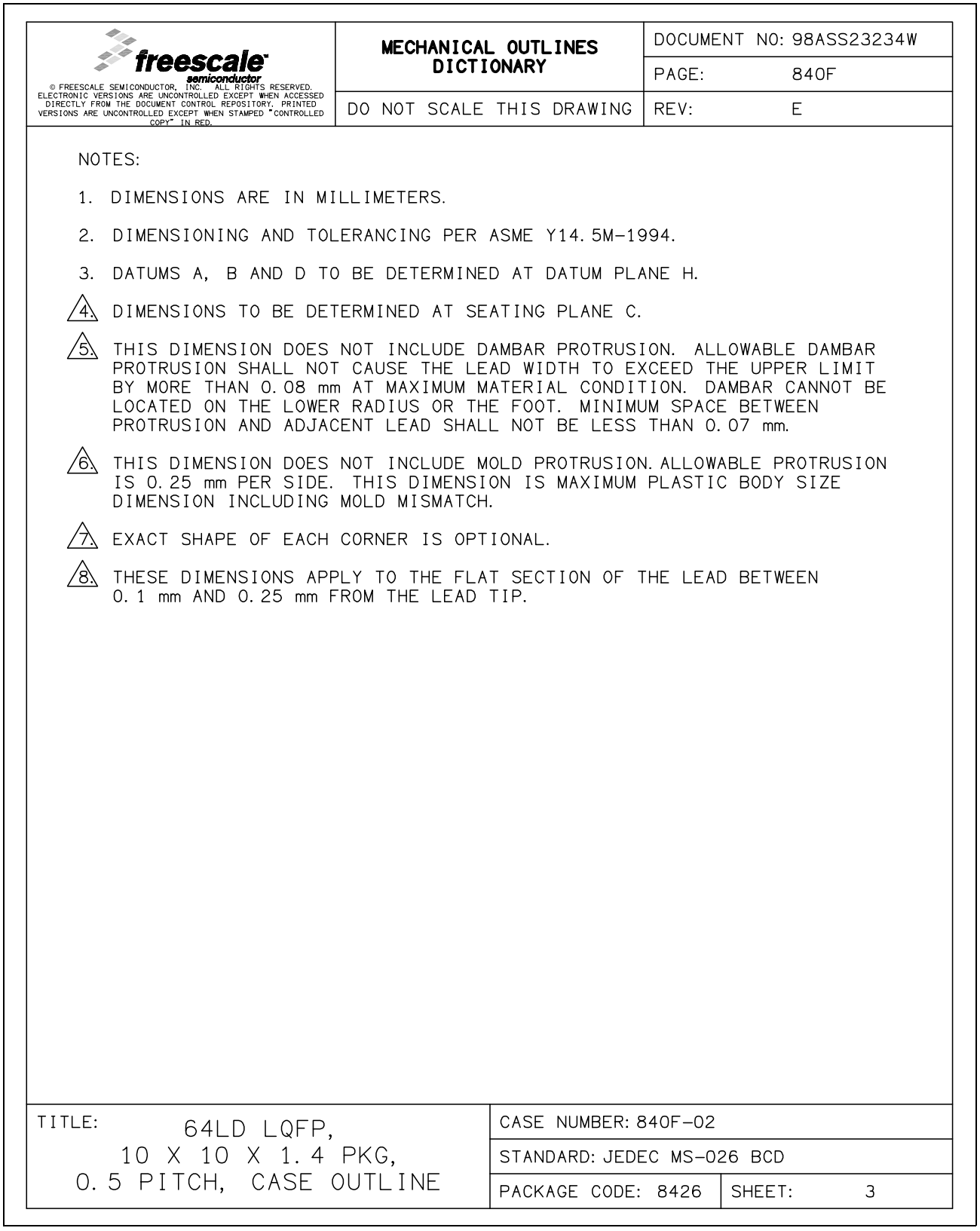

Figure 41. 64LQFP package mechanical drawing (part 3)

5 Ordering information

Figure 42. Commercial product code structure

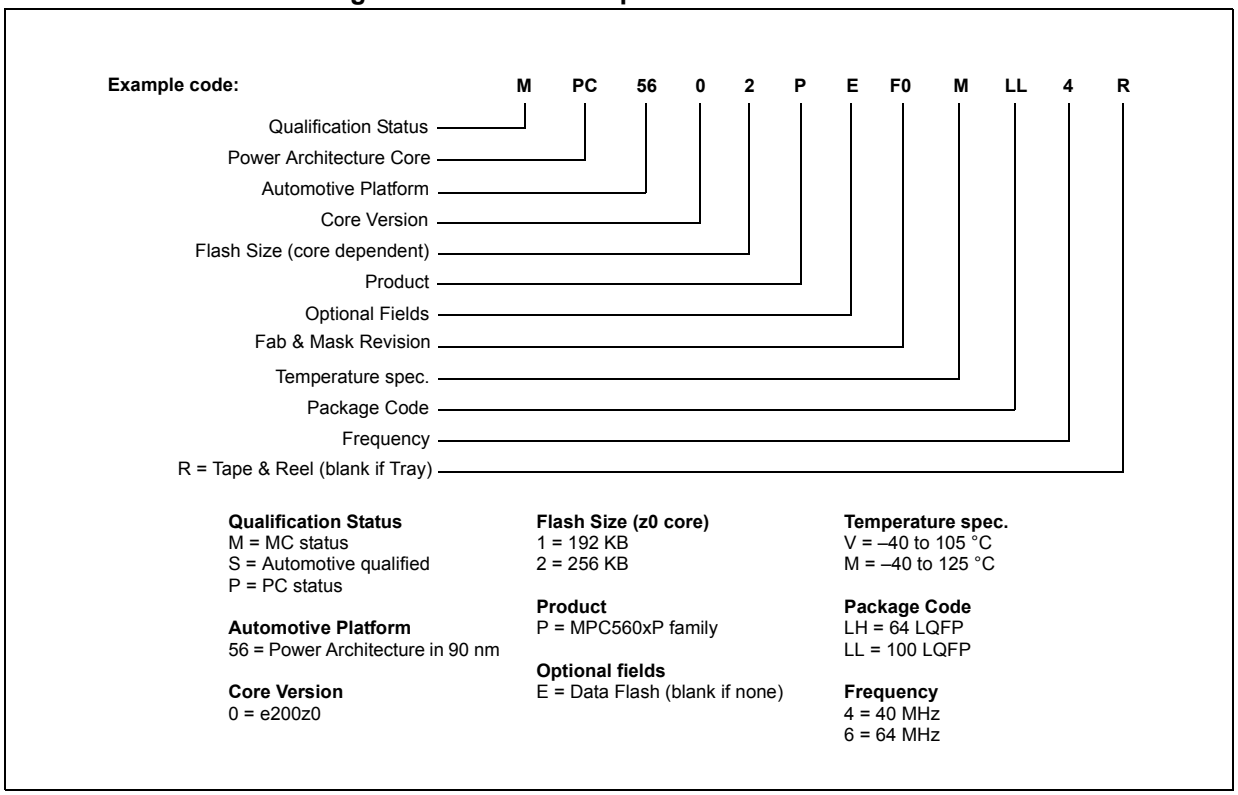

Table 40. Revision history (continued)

Revision	Date	Description of
3	16 Dec 2010	"Introduction" section: • Changed title (was "Overview") • Updated contents "MPC5602P device comparison" table: • Added sentence above table • Removed "FlexRay" row "MPC5602P block diagram": added the following blocks: MC_CGM, MC_ME, MC_PCU, MC_RGM, CRC, and SSCM Added "MPC5602P series block summary" table "Pin muxing" section: removed information on "Symmetric pads" "Electrical characteristics" section: • Updated "Caution" note • Demoted "NVUSRO register" section to subsection of "DC electrical characteristics" section • "NVUSRO register" section: deleted "NVUSRO[WATCHDOG_EN] field description" section Updated "EMI testing specifications" table "Low voltage monitor electrical characteristics" table: updated $V_{MLVDDOK\_H}$ max value "DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)" table: removed $_{VOL\_SYM}$, and V_{OH_SYM} rows "Supply current (5.0 V, NVUSRO[PAD3V5V] = 0)" table: • $I_{DD\_LV\_CORE}$, RUN—Maximum mode, 40/64 MHz: updated typ/max values • $I_{DD\_LV\_CORE}$, RUN—Airbag mode, 40/64 MHz: updated typ/max values • $I_{DD\_LV\_CORE}$, RUN—Maximum mode, "P" parameter classification: removed • I_{DD_FLASH}: removed rows • I_{DD_ADC}, Maximum mode: updated typ/max values • I_{DD_OSC}: updated max value Updated "DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)" table "Supply current (3.3 V, NVUSRO[PAD3V5V] = 1)" table: • $I_{DD\_LV\_CORE}$, RUN—Maximum mode, 40/64 MHz: updated typ/max values • $I_{DD\_LV\_CORE}$, RUN—Airbag mode, 40/64 MHz: updated typ/max values • I_{DD_FLASH}: removed rows • I_{DD_ADC}, Maximum mode: updated typ/max values • I_{DD_OSC}: updated max value Added "I/O consumption" table Removed "I/O weight" table Updated "Main oscillator electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)" table Updated "Main oscillator electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)" table "Input clock characteristics" table: updated f_{CLK} max value "PLLMRFM electrical specifications (V_{DDPLL} = 1.08 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)" table: • Updated supply voltage range for V_{DDPLL} in the table title • Updated f_{SCM} max value • Updated C_{JITTER} row • Updated f_{MOD} max value Updated "16 MHz RC oscillator electrical characteristics" table Updated "ADC conversion characteristics" table

Table 40. Revision history (continued)

Revision	Date	Description of
4	11 May 2011	Editorial and formatting changes throughout Section 1, “Introduction: Reorganized contents MPC5602P block diagram: reorganized blocks above and below peripheral bridge; made arrow going from peripheral bridge to crossbar switch bidirectional Updated Section 1.5, “Feature list: • changed core feature from “64 MHz” to “Up to 64 MHz” • memory organization • moved “16-channel eDMA controller” item to “Interrupts and events” item • LINFlex: changed “2 LINFlex modules” to “Up to 2 LINFlex modules” • DSPI: changed “3 DSPI channels“ to “Up to 3 DSPI channels” • ADC: changed “16 input channels“ to “Up to 16 input channels” Added Section 1.5, “Feature details 64-pin and 100-pin LQFP pinout diagrams: replaced instances of HV_AD0 with HV_ADC0 System pins: updated “XTAL” and “EXTAL” rows Updated LQFP thermal characteristics Updated EMI testing specifications Section 3.8.1, “Voltage regulator electrical characteristics: removed BCP56 from named BJTs; replaced two configuration diagrams and two electrical characteristics tables with single diagram and single table Voltage regulator electrical characteristics: updated $V_{DD\_LV\_REGCOR}$ row Low voltage monitor electrical characteristics: updated $V_{MLVDDOK\_H}$ max value—was 1.15 V; is 1.145 V Supply current (5.0 V, NVUSRO[PAD3V5V] = 0): changed symbol $I_{DD\_LV\_CORE}$ to $I_{DD\_LV\_CORx}$; changed parameter classification from T to P for $I_{DD\_LV\_CORx}$ RUN—Maximum mode at 64 MHz; added I_{DD_FLASH} characteristics; replaced instances of “Airbag” mode with “Typical mode” Supply current (3.3 V, NVUSRO[PAD3V5V] = 1): changed symbol $I_{DD\_LV\_CORE}$ to $I_{DD\_LV\_CORx}$; replaced instances of “Airbag” mode with “Typical mode” DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1): corrected parameter description for V_{OL_F}—was “Fast, high level output voltage”; is “Fast, low level output voltage” Added Section 3.10.4, “Input DC electrical characteristics definition Main oscillator output electrical characteristics tables: replaced instances of EXTAL with XTAL; added load capacitance parameter FMPLL electrical characteristics: updated conditions and table title; removed f_{sys} row; updated $f_{FMPLLOUT}$ values; replaced instances of V_{DDPLL} with $V_{DD\_LV\_COR0}$; replaced instances of V_{SSPLL} with $V_{SS\_LV\_COR0}$ 16 MHz RC oscillator electrical characteristics: removed rows $\Delta_{RCMTRIM}$ and $\Delta_{RCMSTEP}$ ADC characteristics and error definitions: updated symbols ADC conversion characteristics: updated symbols; added row t_{ADC_PU} Added Section 3.15.2, “Flash memory power supply DC characteristics Added Section 3.15.3, “Start-up/Switch-off timings Removed section “Generic timing diagrams”
4 (cont’d)	11 May 2011	Updated Start-up reset requirements diagram Removed FlexCAN timing characteristics RESET electrical characteristics: added row for t_{POR} In the range of figures “DSPI Classic SPI Timing — Master, CPHA = 0” to “DSPI PCS Strobe (PCSS) Timing”: added note Table A-1: added “DUT”, “NPN”, and “RISC”