Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	I²C, I²S, PCM, SPI, UART
Clock Rate	1.28MHz
Non-Volatile Memory	PRAM (24kB)
On-Chip RAM	16kB
Voltage - I/O	1.80V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-TFQFN Exposed Pad
Supplier Device Package	52-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/0w344-004-xtp

3.0 BelaSigna 200 Design and Layout Strategies

BelaSigna 200 is designed to allow both digital and analog processing in a single system. Due to the mixed-signal nature of this system, the design of the printed circuit board (PCB) layout is critical to maintain the high audio fidelity of BelaSigna 200. To avoid coupling noise into the audio signal path, keep the digital traces away from the analog traces. To avoid electrical feedback coupling, isolate the input traces from the output traces.

3.1 Recommended Ground Design Strategy

The ground plane should be partitioned into two: the analog ground plane (AGND) and the digital ground plane (DGND). These two planes should be connected together at a single point, known as the star point. The star point should be located at the ground terminal of a capacitor on the output of the power regulator as illustrated in Figure 2.

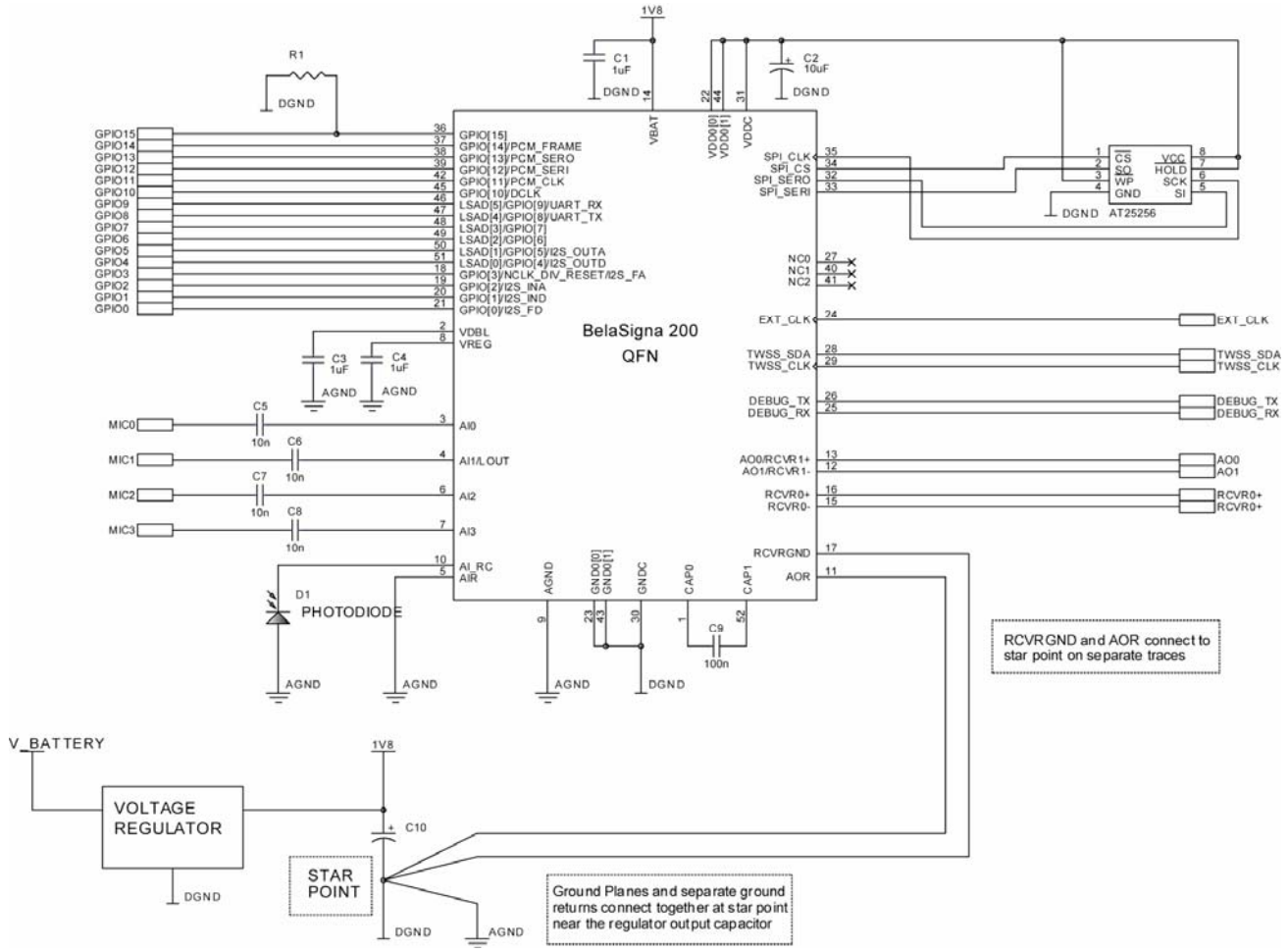


Figure 2: Schematic of Ground Scheme

The DGND plane is used as the ground return for digital circuits and should be placed under digital circuits.

The AGND plane should be kept as noise-free as possible. It is used as the ground return for analog circuits and it should surround analog components and pins. It should not be connected to or placed under any noisy circuits such as RF chips, switching supplies or

digital pads of BelaSigna 200 itself. Analog ground returns associated with the audio output stage should connect back to the star point on separate individual traces.

For more information on the recommended ground design strategy, see Table 1.

In some designs, space constraints may make separate ground planes impractical. In this case a star configuration strategy should be used. Each analog ground return should connect to the star point with separate traces.

3.2 Internal Power Supplies

Power management circuitry in BelaSigna 200 generates separate digital (VDDC) and analog (VREG, VDBL) regulated supplies. Each supply requires an external decoupling capacitor, even if the supply is not used externally. Decoupling capacitors should be placed as close as possible to the power pads. Further details are provided in Table 1. Non-critical signals are outlined in Table 2.

Table 1: Critical Signal

Pin Name	Description	Routing Guideline
VBAT	Power supply	Place 1µF (min) decoupling capacitor close to pin. Connect negative terminal of capacitor to DGND plane.
VREG, VDBL	Internal regulator for analog sections	Place separate 1µF decoupling capacitors close to each pin. Connect negative capacitor terminal to AGND. Keep away from digital traces and output traces. VREG may be used to generate microphone bias. VDBL shall not be used to supply external circuitry.
AGND	Analog ground return	Connect to AGND plane.
VDDC	Internal regulator for digital sections	Place 10µF decoupling capacitor close to pin. Connect negative terminal of capacitor to DGND. Should be connected to VDDO pins and to EEPROM power.
GNDO, GNDC	Digital ground return (pads and core)	Connect to digital ground.
AI0, AI1 / LOUT, AI2, AI3	Microphone inputs	Keep as short as possible. Keep away from all digital traces and audio outputs. Avoid routing in parallel with other traces. Connect unused inputs to AGND.
AIR	Input stage reference voltage	Connect to AGND. If no analog ground plane, should share trace with microphone grounds to star point.
AO0, AO1	Analog audio output	Keep away from microphone inputs.
RCVR0+, RCVR0-, RCVR1+, RCVR1-	Direct digital audio output	Keep away from analog traces, particularly microphone inputs. Corresponding traces should be of approximately the same length.
AOR	Output stage reference voltage	Connect to star point. Share trace with power amplifier (if present).
RCVRGND	Output stage ground return	Connect to star point.
EXT_CLK	External clock input / internal clock output	Minimize trace length. Keep away from analog signals. If possible, surround with digital ground.
AI_RC	Infrared receiver input	If used, minimize trace length to photodiode.

4.2 CSP Package Option

4.2.1. CSP Mechanical Information

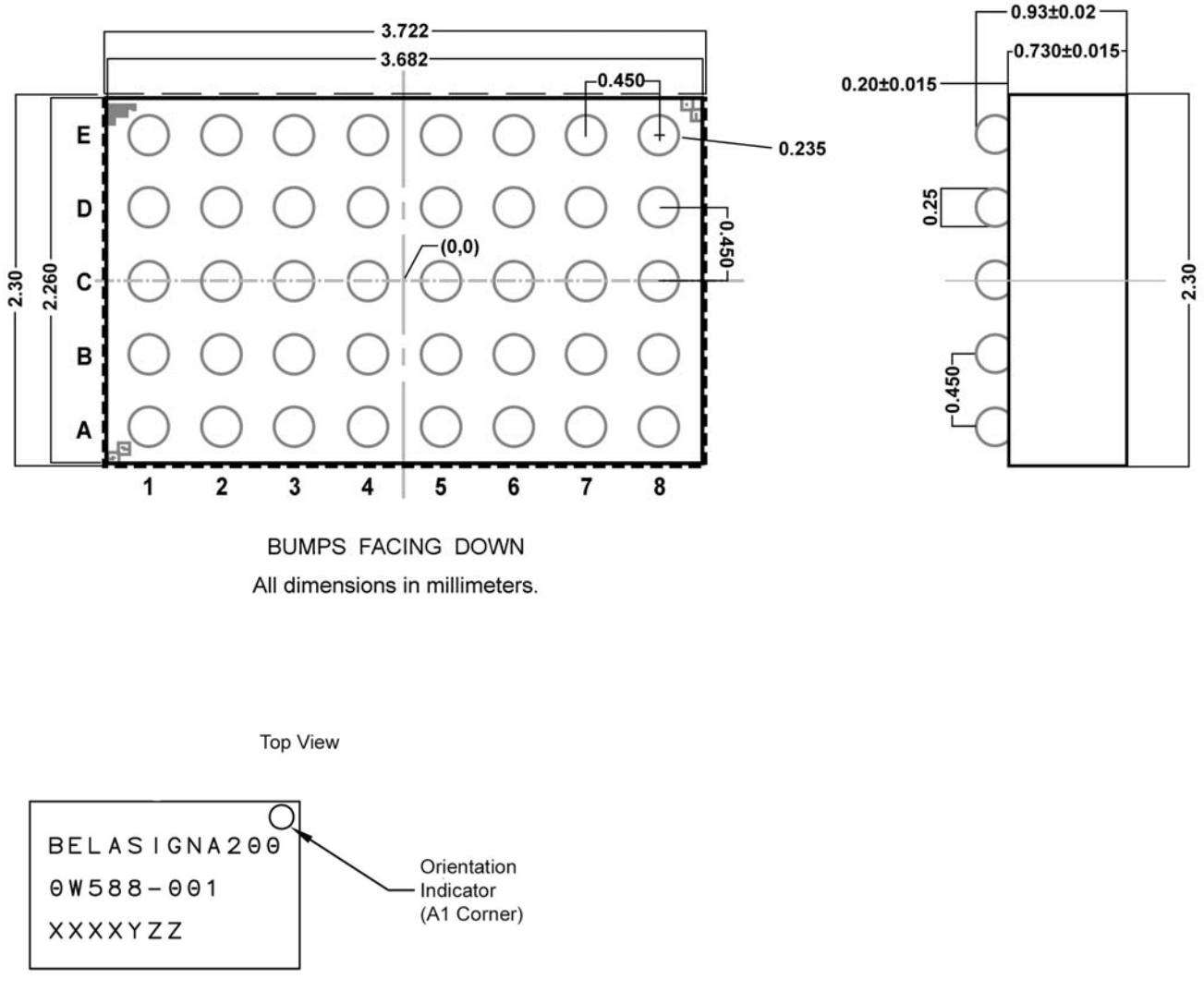


Figure 7: CSP Mechanical Drawings

4.2.2. CSP Pad Out

Table 4: Pad Out (Advance Information)

Pad Index	Pad Name	Pad Function	I/O	U/D
B2	CAP0	Charge pump capacitor pin 0	N/A	N/A
A2	CAP1	Charge pump capacitor pin 1	N/A	N/A
A1	VDBL	Double voltage	O	N/A
C3	VREG	Regulated voltage for microphone bias	O	N/A
B3	A|0	Audio signal input to ADC0	I	N/A
B1	A|1/LOUT	Audio signal input to ADC0/line level output signal from preamp 0	I/O	N/A
C2	A|2	Audio signal input to ADC1	I	N/A
C1	A|3	Audio signal input to ADC1	I	N/A
B4	A|R	Reference voltage for microphone	N/A	N/A
C4	AGND	Analog ground	N/A	N/A
D1	AOR	Reference voltage for DAC	N/A	N/A
E1	AO1/RCVR1-	Audio signal output from DAC1/output from direct digital drive 1-	O	N/A
D2	AO0/RCVR1+	Audio signal output from DAC0/output from direct digital drive 1+	O	N/A
D3	RCVR0-	Output from direct digital drive 0	O	N/A
E3	RCVR0+	Output from direct digital drive 0	O	N/A
D4	RCVRGND	Receiver return current	N/A	N/A
E2	VBAT	Positive power supply	I	N/A
E5	VDD	Core logic, EEPROM and pad supply	I	N/A
A6	GNDO	Digital pads ground	N/A	N/A
E6	GNDC	Core logic and pads ground	N/A	N/A
D6	EXT_CLK	External clock input/internal clock output	I/O	U
E7	DEBUG_RX	Debug port receive	I	U
D7	DEBUG_TX	Debut port transmit	O	U
E8	TWSS_SDA	TWSS data	I/O	U
D8	TWSS_CLK	TWSS clock	I	U
C8	SPI_SERO	Serial peripheral interface serial data out	I/O	D
C7	SPI_SERI	Serial peripheral interface serial data in	I	U
B8	SPI_CS	Serial peripheral interface chip select	I/O	D
C6	SPI_CLK	Serial peripheral interface clock	I/O	N/A
A8	GPIO[14]/PCM_FRAME	General-purpose I/O/PCM interface frame	I/O	U
B7	GPIO[13]/PCM_OUT	General-purpose I/O/PCM interface output	I/O	U
A7	GPIO[12]/PCM_IN	General-purpose I/O/PCM interface input	I/O	U
B6	GPIO[11]/PCM_CLK	General-purpose I/O/PCM interface clock	I/O	U
A5	GPIO[10]/DCLK	General-purpose I/O/class D receiver clock	I/O	U
B5	LSAD[5]/GPIO[9]/UART_RX	Low-speed A/D/general-purpose I/O/general-purpose UART receive	I/O	U
A4	LSAD[4]/GPIO[8]/UART_TX	Low-speed A/D input/general-purpose I/O/general-purpose UART transmit	I/O	U
C5	LSAD[3]/GPIO[7]	Low-speed A/D input/general purpose I/P	I/O	U
A3	LSAD[1]/GPIO[5]/I2S_OUT A	Low-speed A/D inputs/general-purpose I/O/I2S interface analog blocks output	I/O	U
D5	LSAD[0]/GPIO[4]/I2S_OUT D	Low-speed A/D inputs/general-purpose I/O/I2S interface analog blocks output	I/O	U
E4	GPIO[3]/ NCLK_DIV_RESET/I2S_FA	General-purpose I/O/clock divider reset/I2S interface analog blocks frame output	I/O	U

4.2.3. CSP Environmental Characteristics

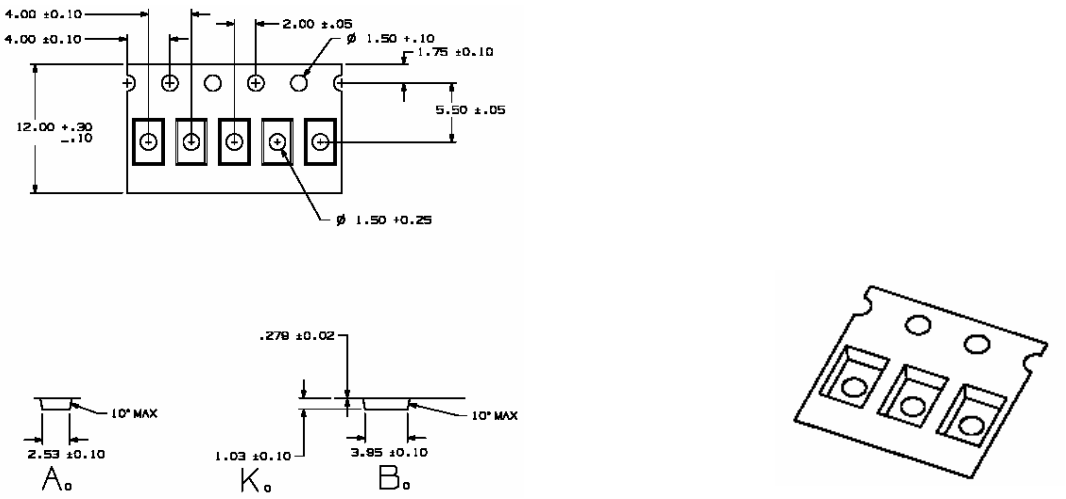
All parts supplied against this specification have been qualified as follows:

Table 5:

Packaging Level	
Moisture sensitivity level (MSL)	JEDEC Level 3 30°C / 60% RH for 192 hours
Pressure cooker test (PCT)	121°C / 100% RH / 2 atm for 168 hours
Thermal cycling test (TCT)	-65°C to 150°C for 1000 cycles
Highly accelerated stress test (HAST)	130°C / 85% RH for 100 hours
High temperature stress test (HTST)	150°C for 1000 hours
Board Level	
Temperature	-40°C to 125°C for 1000 cycles with no failures (for board thickness <40mils and underfilled CSP)
Drop	1m height with no failures

4.2.4. CSP Carrier Information

The devices will be provided in standard 7” Tape & Reel carrier with 5,000 parts per reel.



Note: all dimensions in millimeters

Figure 8: CSP Tape Dimensions

4.2.5. CSP Design Considerations

In order to achieve the highest level of miniaturization, the CSP package is constrained in ways that will factor into design decisions. The CSP will only operate in HV mode, and therefore requires a 1.8V operating voltage. The number of pins is reduced to 40 (compared to 49 active pins on the QFN). This reduction eliminates access to GPIOs (0,1,2,6,15), LSAD 2, the I2S interface, and the IR remote receiver.

For PCB manufacture with BelaSigna 200 CSP, ON Semiconductor recommends Solder-on-Pad (SoP) surface finish. With SoP, the solder mask opening should be solder mask-defined and copper pad geometry will be dictated by the PCB vendor’s design requirements.

5.0 Development Tools

5.1 Evaluation and Development Kit (EDK)

BelaSigna 200 is supported by a set of development tools included in the evaluation and development kit (EDK).

The EDK is intended for use by DSP software developers and hardware systems integrators. It consists of the following components:

- Hardware
    - BelaSigna 200 evaluation and development board (contains BelaSigna 200 device)
- Software
    - Complete assembly tool chain (assembler, linker, librarian, etc.)
    - Low-level hardware-specific libraries
    - Basic algorithm toolkit (BAT)
    - Basic operating system libraries (BOS)
    - WOLA windows and microcode
    - Real-time debugger
    - EEPROM file system manager
    - UltraEdit IDE
    - WOLA toolbox for Matlab for rapid application development and prototyping

BAT and BOS provide all the common processing routines in an easy-to-call macro structure. This streamlines the assembly level coding by encapsulating redundant work, while maintaining the true efficiency of hardware-level coding.

For advanced DSP developers or application developers, ON Semiconductor provides an application development extension to the EDK, which contains the following:

- Python language installer (version 2.2)
- The wxPython GUI toolkit
- Embedding toolkit (used to build standalone Python applications)
- ON Semiconductor extension
    - Python interface (pyLLCOM) to ON Semiconductor's low-level communications library (LLCOM)
    - File I/O library (supports standard ON Semiconductor file formats)
    - EEPROM access library
    - DSH (ON Semiconductor Python Shell – standard command-line shell with customizations for BelaSigna 200)

5.2 BelaSigna 200 Rapid Prototyping Module

The rapid prototyping module (RPM) is fast and easy for designers to integrate with existing and future products that are not yet DSP-enabled. It also allows for the quick implementation of field trials and rapid prototyping to evaluate the benefits of BelaSigna 200. The RPM features BelaSigna 200 along with a 256-Kbit EEPROM for storing a variety of custom algorithms. On-board power regulation circuitry allows the RPM to run off a wide variety of power supplies. A fast oscillator (included on the RPM) running at 24.576MHz provides a choice of many sampling frequencies and can be enabled for when heavy-duty signal processing is required.

5.3 BelaSigna 200 Demonstrator

The BelaSigna 200 demonstrator lets device manufacturers quickly and easily assess the speech- and audio-centric benefits delivered by BelaSigna 200 in a full-featured, self-contained portable unit. The demonstrator is housed in a durable, portable, lightweight package complete with belt clip to facilitate demonstrations in the field. This tool can be easily utilized in real world scenarios to experience the benefits of noise reduction, signal enhancement and a variety of other algorithms. The demonstrator can be connected to a wired headset and function like a dongle to communicate with a Bluetooth mobile phone.

Contact your account manager for more information.

6.0 Architecture Overview

6.1 RCore DSP

The RCore is a 16-bit fixed-point, dual-Harvard-architecture DSP. It includes efficient normalize and de-normalize instructions, plus support for double-precision operations to provide the additional dynamic range needed for many applications. All memory locations in the system are accessible by the RCore using several addressing modes including indirect and circular modes. The RCore generally assumes master functionality of the system.

6.1.1. RCore DSP Architecture

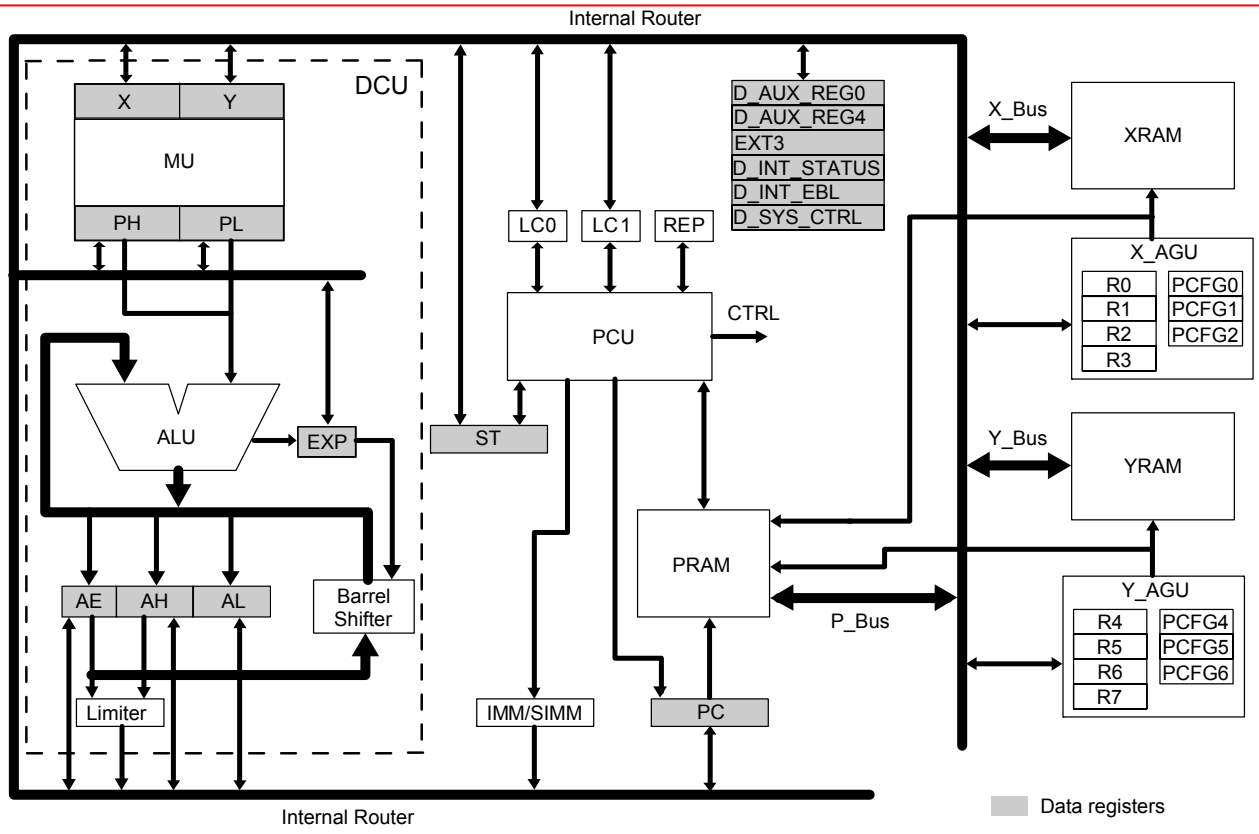


Figure 9: RCore Programming Model

The RCore is a single-cycle pipelined multiply-accumulate (MAC) architecture that feeds into a 40-bit accumulator complete with barrel shifter for fast normalization and de-normalization operations. Program execution is controlled by a sequencer that employs a three-stage pipeline (FETCH, DECODE, EXECUTE). Furthermore, the RCore incorporates pointer configuration registers for low cycle-count address generation when accessing the three memories: program memory (PRAM), X data memory (XRAM) and Y data memory (YRAM).

7.0 Instruction Set

Table 6: Instruction Set

Instruction	Description
ABS A [,Cond] [,DW]	Calculate absolute value of A on condition
ADD A, Reg [,C]	Add register to A
ADD A, (Rij) [,C]	Add memory to A
ADD A, DRAM [,B]	Add (DRAM) to A
ADD A, (Rij)p [,C]	Add program memory to A
ADD A, Rc [,C]	Add Rc register to A
ADDI A, IMM [,C]	Add IMM to A
ADSI A, SIMM	Add signed SIMM to A
AND A, Reg	AND register with AH to AH
AND A, (Rij)	AND memory with AH to AH
AND A, DRAM [,B]	AND (DRAM) with AH to AH
AND A, (Rij)p	AND program memory with AH to AH
AND A, Rc	AND Rc register with AH to AH
ANDI A, IMM	AND IMM with AH to AH
ANSI A, SIMM	AND unsigned SIMM with AH to AH
BRA PRAM [,Cond]	Branch to new address on condition
BREAK	Stop the DSP for debugging purposes
CALL PRAM [,Cond] [,B]	Push PC and branch to new address on condition
CLB A	Calculate the leading bits on A
CLR A [,DW]	Clear accumulator
CLR Reg	Clear register
CMP A, Reg [,C]	Compare register to A
CMP A, (Rij) [,C]	Compare memory to A
CMP A, DRAM [,B]	Compare (DRAM) to A
CMP A, (Rij)p [,C]	Compare program memory to A
CMP A, Rc [,C]	Compare Rc register to A
CMPI A, IMM [,C]	Compare IMM to A
CMSI A, SIMM	Compare signed SIMM to A
CMPL A [,Cond] [,DW]	Calculate logical inverse of A on condition
DADD [Cond] [,P]	Add PH | PL to A, update PH | PL on condition
DBNZ0/1 PRAM	Branch to new address if LC0/1 <> 0

Instruction	Description
DCMP	Compare PH | PL to A
DEC A [,Cond] [,DW]	Decrement A on condition
DEC Reg [Cond]	Decrement register on condition
DEC (Rij) [,Cond]	Decrement memory on condition
DSUB [Cond] [,P]	Subtract PH | PL from A, update PH | PL on condition
EOR A, Reg	Exclusive-OR register with AH to AH
EOR A, (Rij)	Exclusive-OR memory with AH to AH
EOR A, DRAM [,B]	Exclusive-OR (DRAM) with AH to AH
EOR A, (Rij)p	Exclusive-OR program memory with AH to AH
EOR A, Rc	Exclusive-OR Rc register with AH to AH
EORI A, IMM	Exclusive-OR IMM with AH to AH
EOSI A, SIMM	Exclusive-OR unsigned SIMM with AH to AH
INC A [,Cond] [,DW]	Increment A on condition
INC Reg [,Cond]	Increment register on condition
INC (Rij) [,Cond]	Increment memory on condition
LD Rc, Rc	Load Rc register with Rc register
LD Reg, Reg	Load register with register
LD Reg, (Rij)	Load register with memory
LD (Rij), Reg	Load memory with register
LD A, DRAM [,B]	Load A with (DRAM)
LD DRAM, A [,B]	Load (DRAM) with A
LD Rc, (Rij)	Load Rc register with memory
LD (Rij), Rc	Load memory with Rc register
LD Reg, (Rij)p	Load register with program memory
LD (Rij)p, Reg	Load program memory with register
LD Reg, (Reg)p	Load register with program memory via register
LD Reg, Rc	Load register with Rc register
LD Rc, Reg	Load Rc register with register
LDI Reg, IMM	Load register with IMM
LDI Rc, IMM	Load Rc register with IMM
LDI (Rij), IMM	Load memory with IMM

Table 7: Instruction Set Continued

Instruction	Description
LDLC0/1 SIMM	Load loop counter with 8-bit unsigned SIMM
LDSI A, SIMM	Load A with signed SIMM
LDSI Rij, SIMM	Load pointer register with unsigned SIMM
MLD (Rj), (Ri) [,SQ]	Multiplier load and clear A
MLD Reg, (Ri) [,SQ]	Multiplier load and clear A
MODR Rj, Ri	Pointer register modification
MPYA (Rj), (Ri) [,SQ]	Multiplier load and accumulate
MPYA Reg, (Ri) [,SQ]	Multiplier load and accumulate
MPYS (Rj), (Ri) [,SQ]	Multiplier load and accumulate negative
MPYS Reg, (Ri) [,SQ]	Multiplier load and accumulate negative
MSET (Rj), (Ri) [,SQ]	Multiplier load
MSET Reg, (Ri) [,SQ]	Multiplier load
MUL [Cond] [,A] [,P]	Update A and/or PH | PL with X*Y on condition
NEG A [,Cond] [,DW]	Calculate negative value of A on condition
NOP	No operation
OR A, Reg	OR register with AH to AH
OR A, (Rij)	OR memory with AH to AH
OR A, DRAM [,B]	OR (DRAM) with AH to AH
OR A, (Rij)p	OR program memory with AH to AH
OR A, Rc	OR Rc register with AH to AH
ORI A, IMM	OR IMM with AH to AH
ORSI A, SIMM	OR unsigned SIMM with AH to AH
POP Reg [,B]	Pop register from stack
POP Rc [,B]	Pop Rc register from stack
PUSH Reg [,B]	Push register on stack
PUSH Rc [,B]	Push Rc register on stack

Instruction	Description
PUSH IMM [,B]	Push IMM on stack
REP n	Repeat next instruction n+1 times (9-bit unsigned)
REP Reg	Repeat next instruction Reg+1 times
REP (Rij)	Repeat next instruction (Rij)+1 times
RES Reg, Bit	Clear bit in register
RES (Rij), Bit	Clear bit in memory
RET [B]	Return from subroutine
RND A	Round A with AL
SET Reg, Bit	Set bit in register
SET (Rij), Bit	Set bit in memory
SET_IE	Set interrupt enable flag
SHFT n	Shift A by +/- n bits (6-bit signed)
SHFT A [,Cond] [,INV]	Shift A by EXP bits on condition
SLEEP [IE]	Sleep
SUB A, Reg [,C]	Subtract register from A
SUB A, (Rij) [,C]	Subtract memory from A
SUB A, DRAM [,B]	Subtract (DRAM) from A
SUB A, (Rij)p [,C]	Subtract program memory from A
SUB A, Rc [,C]	Subtract Rc register from A
SUBI A, IMM [,C]	Subtract IMM from A
SUSI A, SIMM	Subtract signed SIMM from A
SWAP A [,Cond]	Swap AH, AL on condition
TGL Reg, Bit	Toggle bit in register
TGL (Rij), Bit	Toggle bit in memory
TST Reg, Bit	Test bit in register
TST (Rij), Bit	Test bit in memory

Table 8: Notation

Symbol	Meaning
A B	Accumulator update Memory bank selection (X or Y)
C	Carry bit
Cond	Condition in status register
DRAM	Low data (X or Y) memory address (8 bits)
DW	Double word
IE	Interrupt enable flag
IMM	Immediate data (16 bits)

Symbol	Meaning
INV	Inverse shift
P PRAM	PH | PL update Program memory address (16 bits)
Rc	Rc register (R0..7, PCFG0..2, PCFG4..6, LC0/1)
Reg	Data register (AL, AH, X, Y, ST, PC, PL, PH, EXT0, EXP, AE, EXT3..EXT7)
Ri / Rj / Rij	Pointer to X / Y / either data memory
SIMM	Short immediate data (10 bits)
SQ	Square

8.0 Description of Analog Blocks

8.1 Input Stage

The analog audio input stage is comprised of two individual channels. For each channel, one of two possible inputs is routed to the input of the programmable preamplifier that can be configured for bypass or gain values of 12 to 30dB (3-dB steps).

The analog signal is filtered to remove frequencies above 10kHz before it is passed into the high-fidelity 16-bit oversampling ΣΔ A/D converter. Subsequently, any necessary sample rate decimation is performed to downsample the signal to the desired sampling rate. During decimation the level of the signal can be adjusted digitally for optimal gain matching between the two input channels. Any undesired DC component can be removed by a configurable DC-removal filter that is part of the decimation circuitry. The DC removal filter can be bypassed or configured for cut-off frequencies at 5, 10 and 20Hz.

A built-in feature allows a sampling delay to be configured between channel zero and channel one. This is useful in beam-forming applications.

For power consumption savings either of the input channels can be disabled via software.

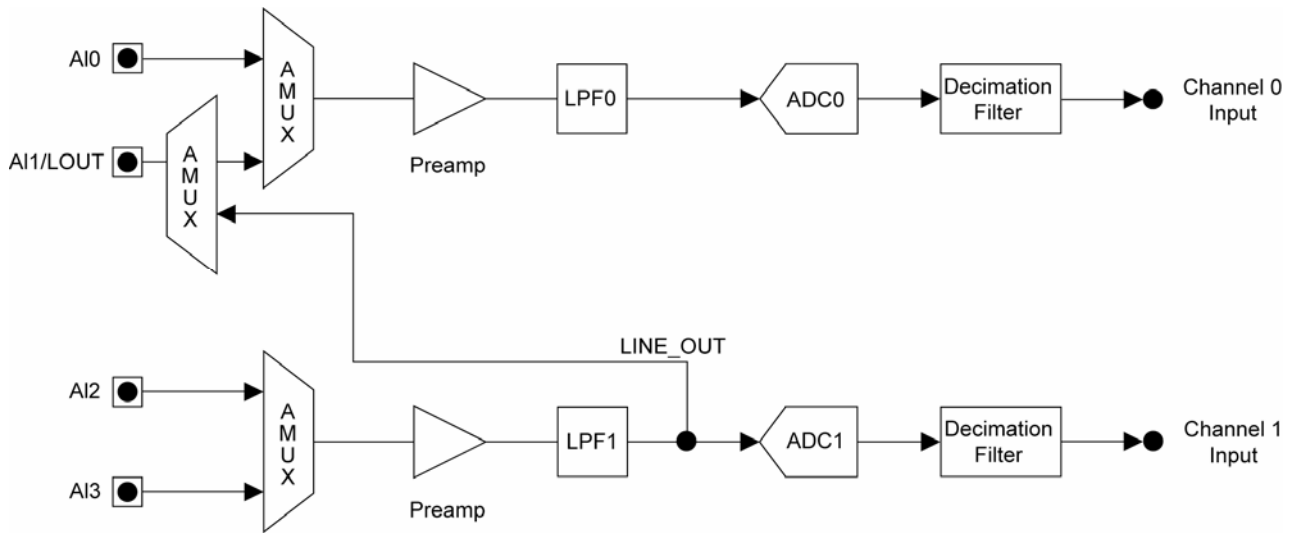


Figure 12: Input Stage

8.2 Output Stage

The analog audio output stage is composed of two individual channels. The first part of the output stage interpolates the signal for highly oversampled D/A conversion and automatically configures itself for the desired oversampling rate. Here, the signal is routed to both the ΣΔ D/A converter and the direct digital outputs. The D/A converter translates the signal into a high-fidelity analog signal and passes it into a reconstruction filter to smooth out the effects of sampling. The reconstruction filter has a fixed cut-off frequency at 10kHz.

From the reconstruction filter, the signal passes through the programmable output attenuator, which can adjust the signal for various line-level outputs or mute the signal altogether. The attenuator can be bypassed or configured to a value in the interval -12 to -30dB (3-dB steps).

The direct digital output provides a bridge driven by a pulse-density modulated output that can be used to directly drive an output transducer without the need for an external power amplifier.

9.2 External Analog Interfaces

9.2.1. Low-Speed A/D Converters (LSAD)

Six LSAD inputs are available on BelaSigna 200. Combined with two internal LSAD inputs (supply and ground) this gives a total of eight multiplexed inputs to the LSAD converter. The multiplexed inputs are sampled sequentially at 1.6kHz per channel. The native data format for the LSAD is 10-bit two's complement. However, a total of eight operation modes are provided that allow a configurable input dynamic range in cases where certain minimum and maximum values for the converted inputs are desired; such as in the case of a volume control where only input values up to a certain magnitude are allowed.

11.0 Electrical Characteristics

11.1 Absolute Maximum Ratings

Table 10: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Supply voltage		2.0	V
Operating temperature range[2]	-40	85	°C
Storage temperature range	-55	125	°C
Voltage at any input pin	-0.3	2.1	V
Caution: Class 2 ESD sensitivity, JESD22-A114-B (2000V)			

11.2 Electrical Characteristics

Conditions: Temperature = 25°C, f_{SYS_CLK} = 1.28MHz (internal), f_{MCLK} = 1.28MHz, f_{SAMP} = 16kHz, V_{bat} = 1.8V

Table 11: Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Overall (1µF VBAT external capacitor)						
Supply voltage	Vbat		1.03	1.25	1.8	V
Current consumption[4]	Ibat	Vbat = 1.8V		650		µA
VREG (1µF external capacitor)						
Regulated output	VREG	unloaded	0.9	1.0	1.1	V
PSRR		@ 1kHz	35	50		dB
Load current	Ireg				2	mA
Load regulation				12	18	mV/mA
Line regulation				2	5	mV/V
VDBL (1µF external capacitor)						
Regulated output	VDBL		1.8	2.0	2.2	V
PSRR		@ 1kHz		45		dB
Load current	Ireg				2	mA
Load regulation		Charge pump cap = 100nF		130	200	mV/mA
Line regulation				5	8	mV/V
VDDC (1µF external capacitor)						
HV output	HV	HV mode		Vbat		V

[2] Audio performance parameters may degrade outside the range of 0 to 70 degrees C. Internal oscillator speed will vary with temperature
[3] Device will operate down to 0.9V but with degraded system specifications
[4] DSP core active; single channel; direct digital output enabled and connected to 100kΩ resistance

11.4 Digital Characteristics

Conditions: Temperature = 25°C, f_{SYS_CLK} = 1.28MHz (internal), f_{MCLK} = 1.28MHz, f_{SAMP} = 16kHz, V_{bat} = 1.8V

Table 13: Digital Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Stage						
Direct digital output load current	Ido				25	mA
Direct digital output resistance	Rdo			10	20	Ω
Direct digital output 0 dynamic range		Unweighted, 100Hz to 22kHz BW		77		dB
Direct digital output 0 THD+N		Unweighted, 100Hz to 10kHz BW input at 1kHz		-63		dB
Direct digital output 1 dynamic range		Unweighted, 100Hz to 22kHz BW		75		dB
Direct digital output 1 THD+N		Unweighted, 100Hz to 10kHz BW input at 1kHz		-62		dB
Internal Oscillator Characteristics						
Clock frequency (internal)	f_{SYS_CLK}			1.28		MHz
Oscillator jitter				0.4	1.0	ns
Oscillator start-up voltage			0.55	0.7	0.85	V
Oscillator settling time		Time required for frequency change of ±20%		1		ms
Other						
Clock frequency (external)	f_{SYS_CLK}	HV mode			33	MHz
High-level input voltage	VIH[7]		1.45	1.8	2.0	V
Low-level input voltage	VIL[7]			0	0.35	V
High-level output voltage Rout = 50ohm	VOH[7]	Isource = 1mA	1.45	1.8		V
Low-level output voltage Rout = 50ohm	VOL	Isink = 1mA		0.05	0.1	V
Input capacitance (digital I/O pads)	CIN				5	pF
Output capacitance (digital I/O pads)	COUT	Maximum load			100	pF
Pull-up resistors	Rup		215	430	645	KΩ
Pull-down resistors	Rdown		215	430	645	kΩ

[7] Digital low (0) represented below 20% of Vbat. Digital high (1) represented above 80% of Vbat.

12.0 Timing Diagrams

12.1 PCM Interface Timing Diagrams

12.1.1. 16-bit

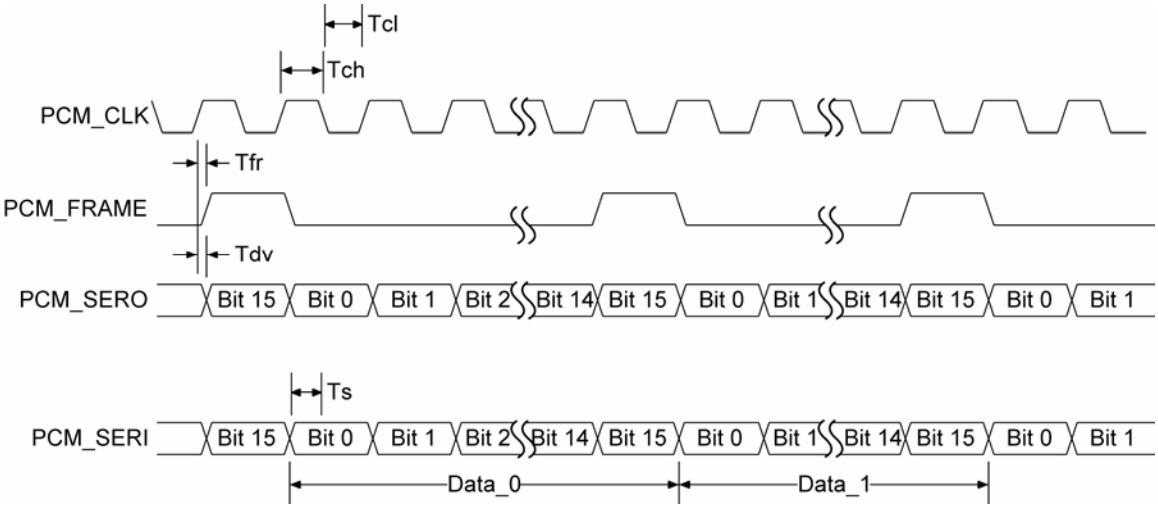


Figure 14: LSB Advanced Short

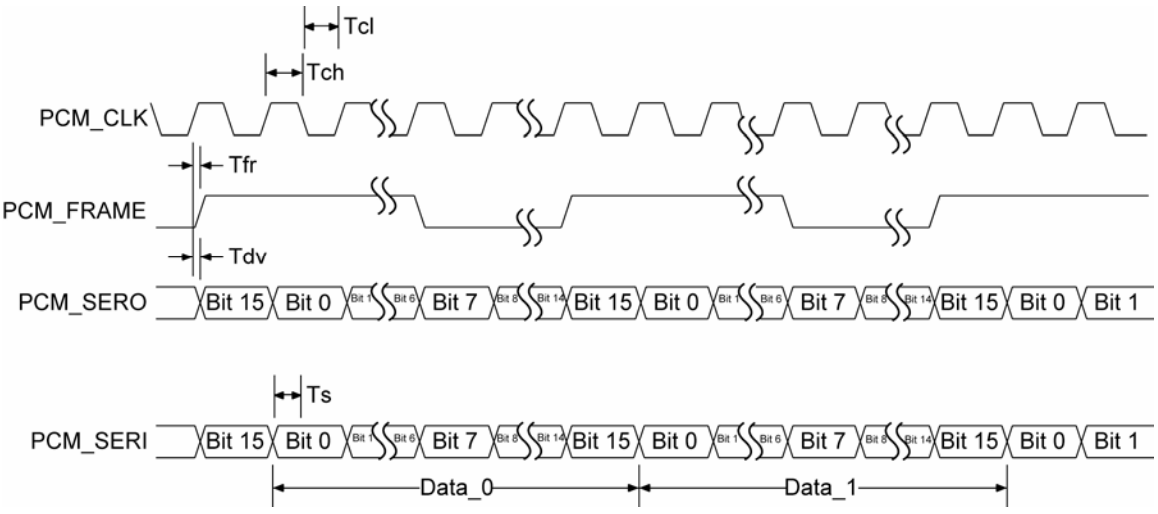


Figure 15: LSB Advanced Wide

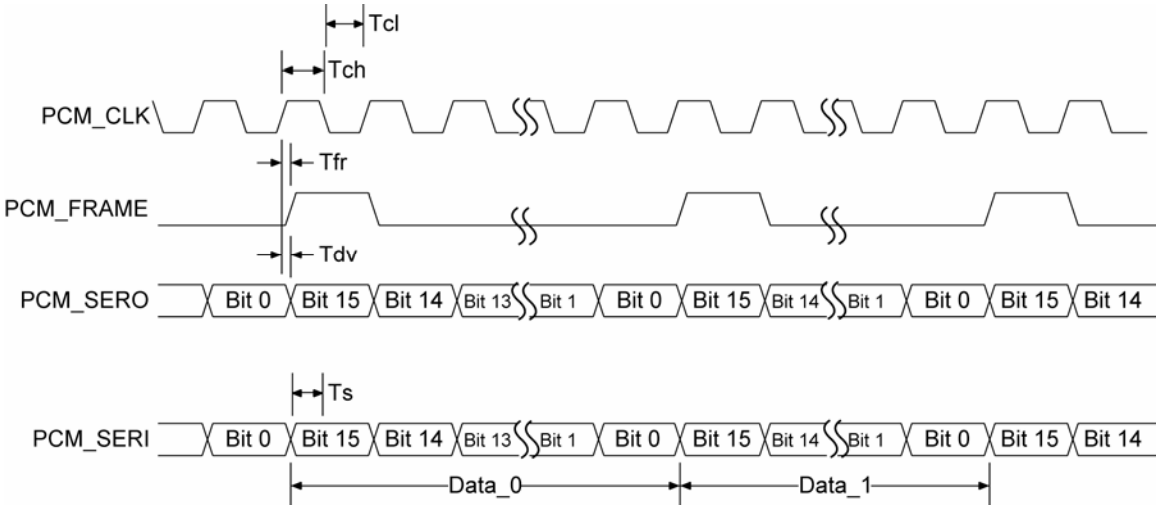


Figure 20: MSB Del Short

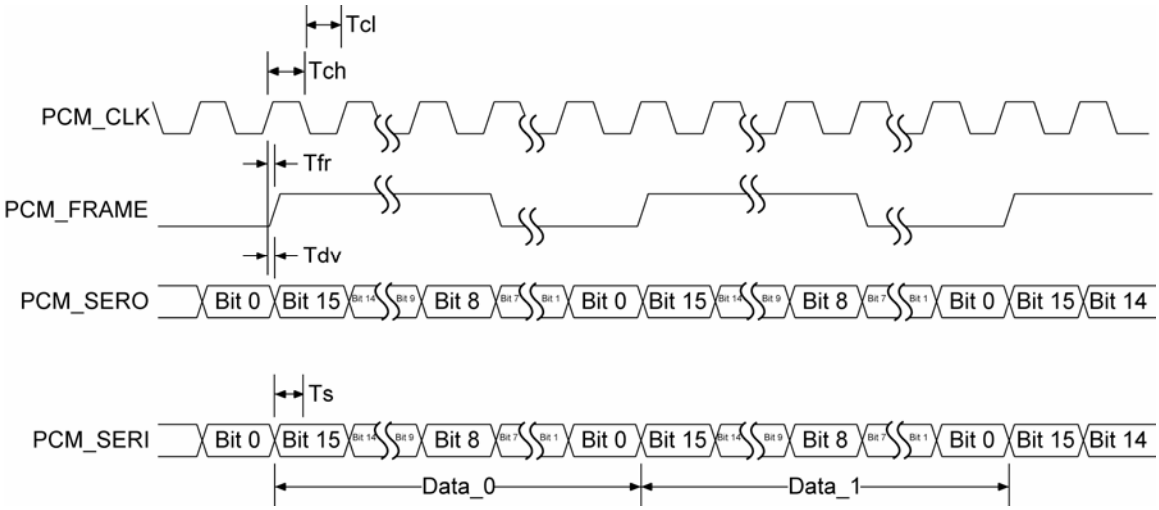


Figure 21: MSB Del Wide

12.1.2. 32-bit

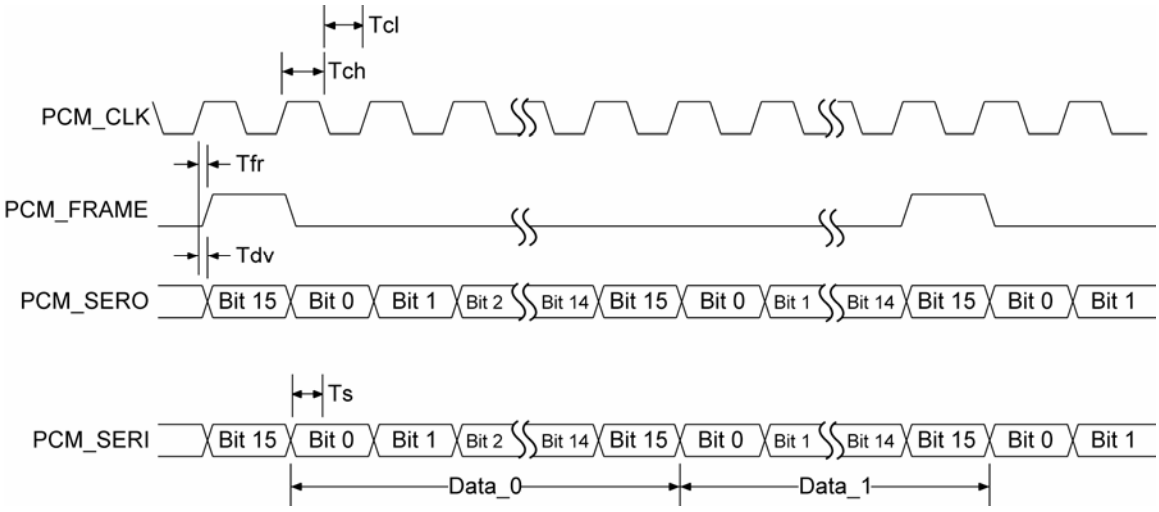


Figure 22: LSB Advanced Short

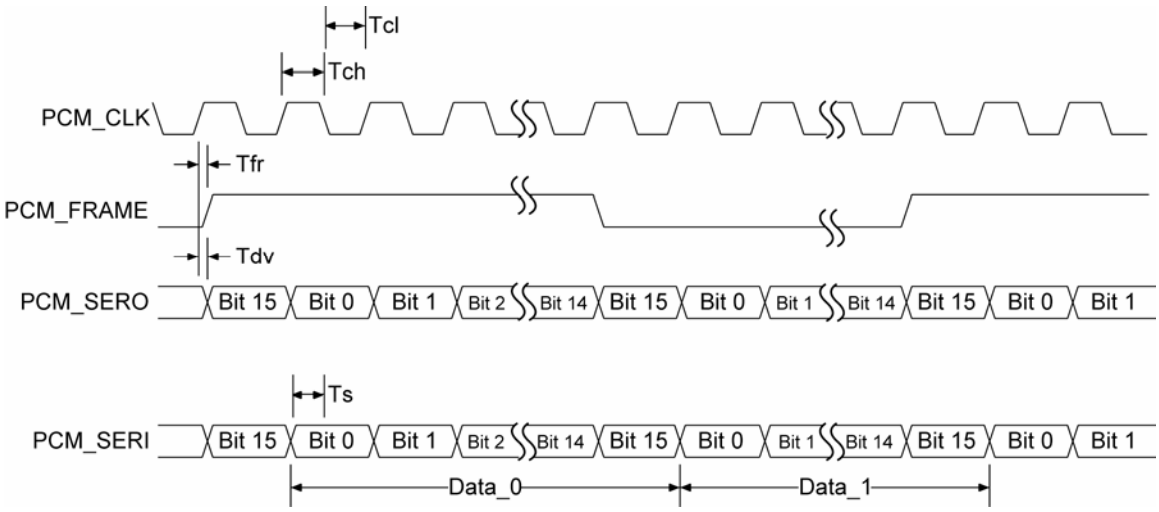


Figure 23: LSB Advanced Wide

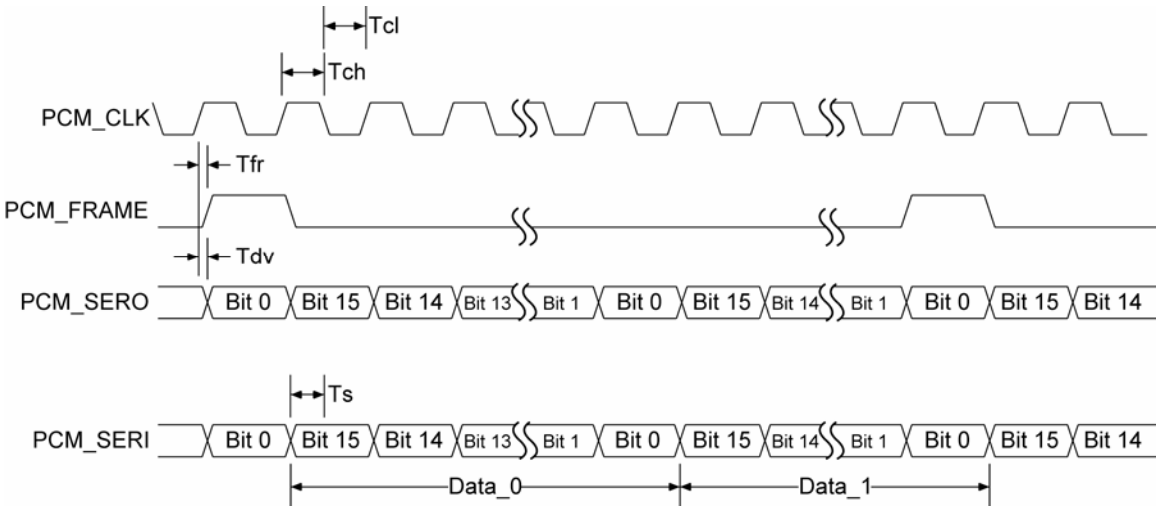


Figure 26: MSB Advanced Short

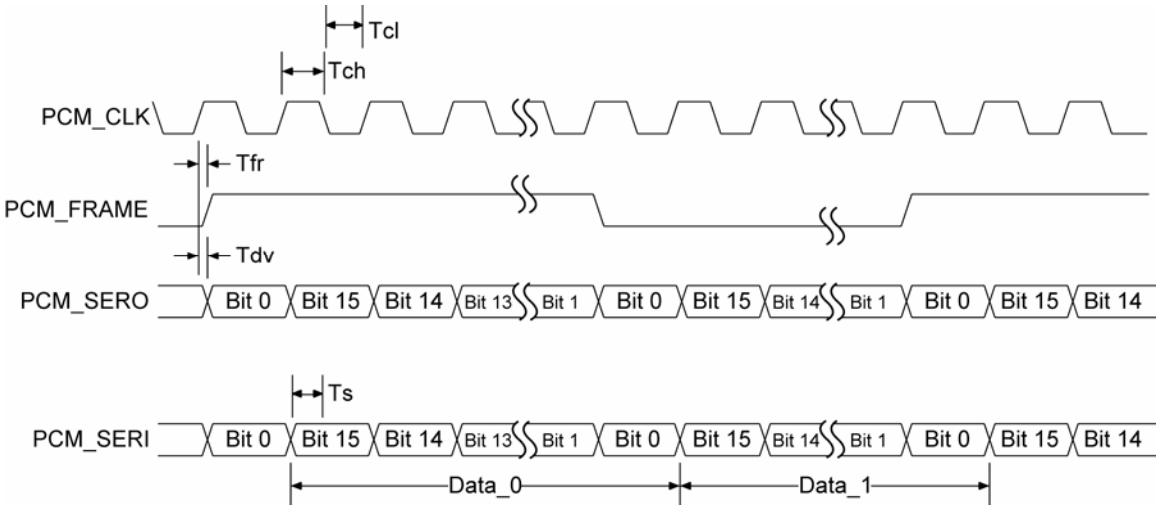


Figure 27: MSB Advanced Wide

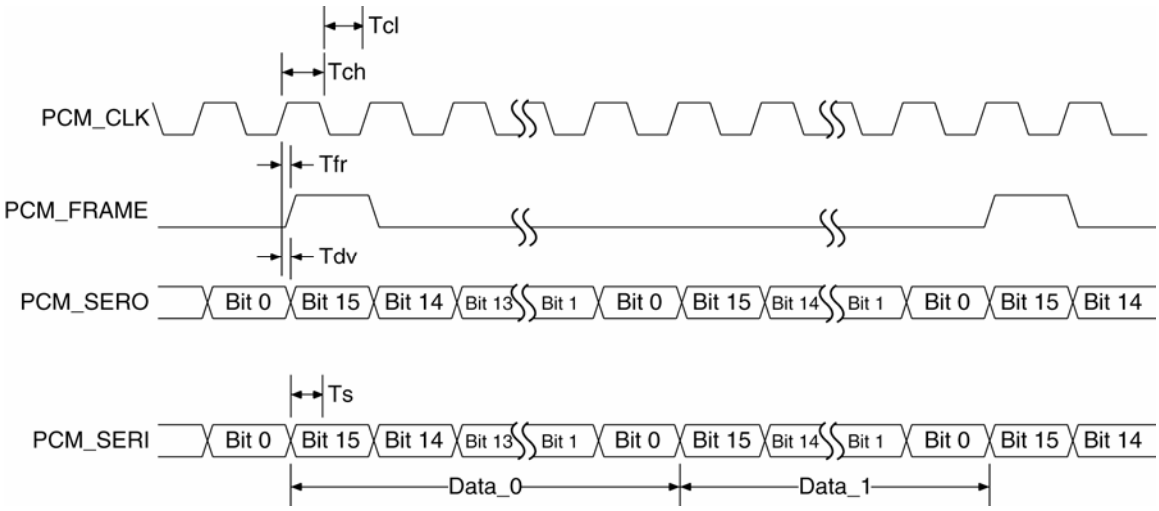


Figure 28: MSB Del Short

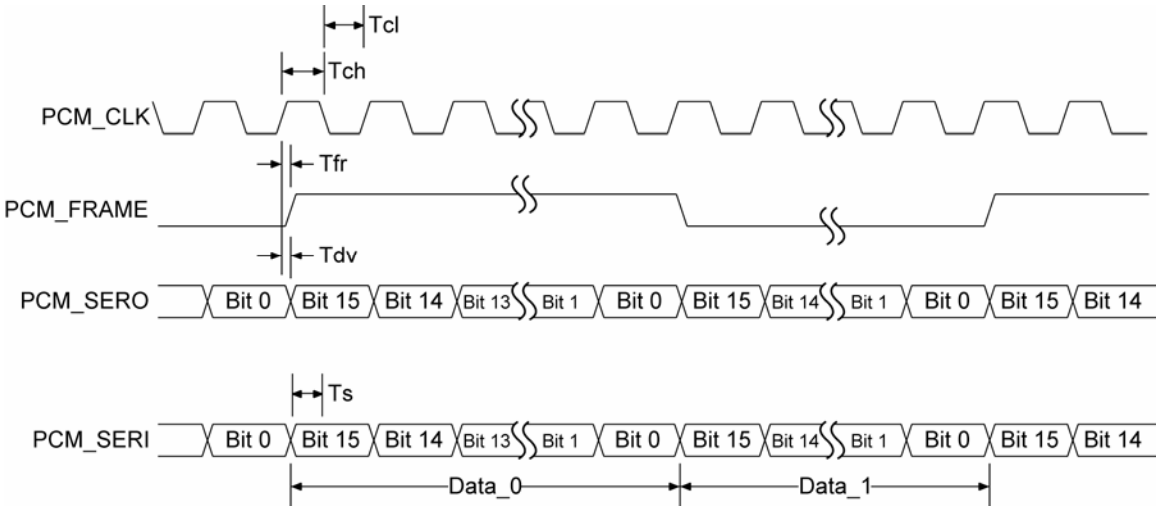


Figure 29: MSB Del Wide

Table 14: PCM Interface Descriptions

Parameter	Description	Min.	Max.	Unit
T_{dv}	PCM_CLK high to data valid		50	ns
T_s	Setup time before PCM_CLK high		10	ns
T_{fr}	PCM_CLK high to PCM_FRAME high		50	ns
T_{ch}	PCM_CLK high period (1.28MHz)		390	ns
T_{cl}	PCM_CLK low period (1.28MHz)		390	ns

12.2 GPIO Timing Diagram

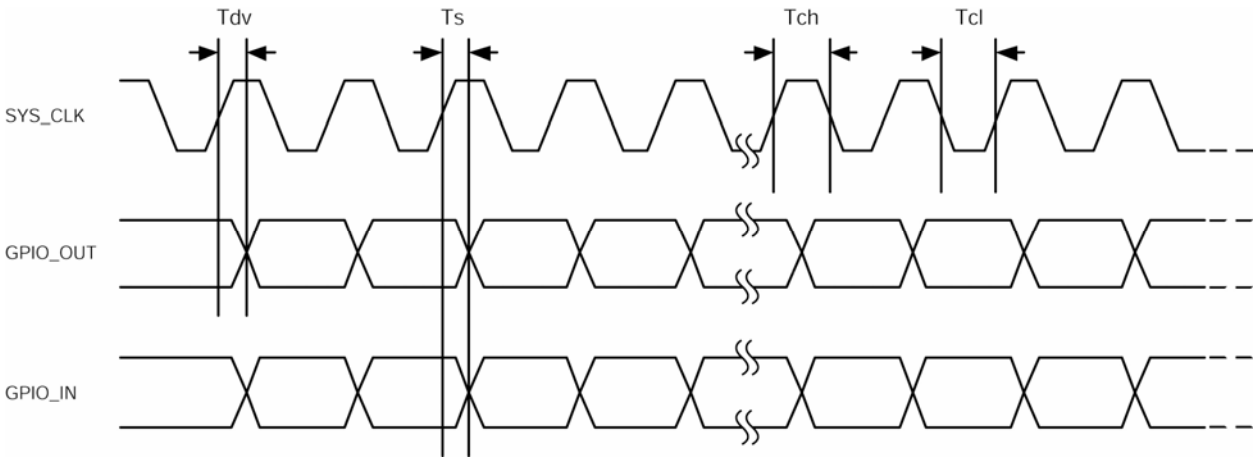


Figure 30: GPIO Timing Diagram

Table 15: GPIO Interface Descriptions

Parameter	Description	Min.	Max.	Unit
T_{dv}	SYS_CLK high to data valid		50	ns
T_s	Setup time before SYS_CLK high		10	ns
T_{ch}	SYS_CLK high period (1.28MHz)		390	ns
T_{cl}	SYS_CLK low period (1.28MHz)		390	ns

16.0 Ordering Information

Part Number	Package	Shipping Configuration	Temperature Range
0W344-004-XTP	8x8mm QFN	Tape & Reel (500 parts per reel)	-85 to 40 °C
0W344-005-XTP	8x8mm QFN	Tape & Reel (1000 parts per reel)	-85 to 40 °C
0W588-002-XUA	2.3x2.8mm WLCSP	Tape & Reel (5000 parts per reel)	-85 to 40 °C

17.0 Company or Product Inquiries

For more information about ON Semiconductor's products or services visit our Web site at http://onsemi.com.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855
Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative