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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	I²C, I²S, PCM, SPI, UART
Clock Rate	1.28MHz
Non-Volatile Memory	PRAM (24kB)
On-Chip RAM	16kB
Voltage - I/O	1.80V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-TFQFN Exposed Pad
Supplier Device Package	52-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/0w344-005-xtp

2.0 Key Features

2.1 System

- 16-bit programmable fixed-point DSP core
- Configurable WOLA filterbank coprocessor optimized for filterbank calculations
- 12-Kword program memory (PRAM)
- Two 4-Kword data memories (XRAM and YRAM)
- Two 384-word dual-port FIFO memories
- Two 128-word dual-port 18-bit memories dedicated to WOLA output results
- 576-word memory dedicated to WOLA gain values, WOLA windows and other configuration data
- Internal oscillator
- Operating voltage of 1.8V nominal
- Ultra-low power: less than 1mW @ 1.28MHz system clock frequency, 1.8V nominal operating voltage, both processors running
- Available in a QFN package; other packages available upon request

2.2 RCore DSP

- Dual-Harvard architecture, 16-bit programmable fixed-point DSP with three execution units
- Single-cycle multiply-accumulate (MAC) with 40-bit accumulator
- Highly parallel instruction set with powerful addressing modes
- Flexible address generation (including modulo addressing) for accessing program memory and data memories, plus control and configuration registers
- Separate system and user stacks with dedicated stack pointers
- Fast normalization and de-normalization operations optimized for signal level calculation and block-floating point calculations
- Supports time-domain pre- and post-processing of input data stream and frequency-domain processing of WOLA output
- Master processor for entire system

2.3 WOLA Filterbank Coprocessor

- Mono and stereo time-frequency transforms providing real or complex data results
- Standard library of overlap-add (OLA) and WOLA filterbank configurations
    - Configurable number of frequency bands
    - Configurable number of frequency bands
    - Configurable oversampling and decimation factors
    - Configurable windows
- Low group delay (< 4ms for 16 bands possible)
- Fast real and complex gain application for magnitude and phase processing
- Block floating-point calculations (4-bit exponent, 18-bit mantissa) to achieve high fidelity
- Maximum digital gain of 90dB possible
- High-fidelity time-frequency domain processing
- Low-overhead interaction with the RCore through shared memories, control registers and interrupts

2.4 Input Output Processor (IOP)

- Block-based DMA for all audio data provides automatic management of input and output FIFOs that reduces processor overhead
- Mono (one in, one out), simple stereo (two in, one out), full stereo (two in, two out) and digital mixed (two in, one out) operating modes
- Interacts with the RCore through interrupts and shared memories
- Normal and smart FIFO audio data accessing schemes available

digital pads of BelaSigna 200 itself. Analog ground returns associated with the audio output stage should connect back to the star point on separate individual traces.

For more information on the recommended ground design strategy, see Table 1.

In some designs, space constraints may make separate ground planes impractical. In this case a star configuration strategy should be used. Each analog ground return should connect to the star point with separate traces.

3.2 Internal Power Supplies

Power management circuitry in BelaSigna 200 generates separate digital (VDDC) and analog (VREG, VDBL) regulated supplies. Each supply requires an external decoupling capacitor, even if the supply is not used externally. Decoupling capacitors should be placed as close as possible to the power pads. Further details are provided in Table 1. Non-critical signals are outlined in Table 2.

Table 1: Critical Signal

Pin Name	Description	Routing Guideline
VBAT	Power supply	Place 1µF (min) decoupling capacitor close to pin. Connect negative terminal of capacitor to DGND plane.
VREG, VDBL	Internal regulator for analog sections	Place separate 1µF decoupling capacitors close to each pin. Connect negative capacitor terminal to AGND. Keep away from digital traces and output traces. VREG may be used to generate microphone bias. VDBL shall not be used to supply external circuitry.
AGND	Analog ground return	Connect to AGND plane.
VDDC	Internal regulator for digital sections	Place 10µF decoupling capacitor close to pin. Connect negative terminal of capacitor to DGND. Should be connected to VDDO pins and to EEPROM power.
GNDO, GNDC	Digital ground return (pads and core)	Connect to digital ground.
AI0, AI1 / LOUT, AI2, AI3	Microphone inputs	Keep as short as possible. Keep away from all digital traces and audio outputs. Avoid routing in parallel with other traces. Connect unused inputs to AGND.
AIR	Input stage reference voltage	Connect to AGND. If no analog ground plane, should share trace with microphone grounds to star point.
AO0, AO1	Analog audio output	Keep away from microphone inputs.
RCVR0+, RCVR0-, RCVR1+, RCVR1-	Direct digital audio output	Keep away from analog traces, particularly microphone inputs. Corresponding traces should be of approximately the same length.
AOR	Output stage reference voltage	Connect to star point. Share trace with power amplifier (if present).
RCVRGND	Output stage ground return	Connect to star point.
EXT_CLK	External clock input / internal clock output	Minimize trace length. Keep away from analog signals. If possible, surround with digital ground.
AI_RC	Infrared receiver input	If used, minimize trace length to photodiode.

Table 2: Non-Critical Signal

Pin Name	Description	Routing Guideline
CAP0, CAP1	Internal charge pump - capacitor connection	Place 100nF capacitor close to pins
DEBUG_TX, DEBUG_RX	Debug port	Not critical Connect to test points
TWSS_SDA, TWSS_CLK	TWSS port	Not critical
GPIO[14..0]	General-purpose I/O	Not critical
GPIO[15]	General-purpose I/O Determines voltage mode during boot. For 1.8V operation, should be connected to DGND	Not critical
UART_RX, UART_TX	General-purpose UART	Not critical
PCM_FRAME, PCM_CLK, PCM_OUT, PCM_IN	Pulse code modulation port	Not critical
I2S_INA, I2S_IND, I2S_FA, I2S_FD, I2S_OUTA, I2S_OUTD	Philips I²S compatible port	Not critical
DCLK	Programmable clock output	Not critical If used, keep away from analog inputs/outputs
LSAD[5..0]	Low-speed A/D converters	Not critical
SPI_CLK, SPI_CS, SPI_SERI, SPI_SERO	Serial peripheral interface port Connect to EEPROM	Not critical

3.3 Audio Inputs

The audio input traces should be as short as possible. The input impedance of each audio input pad (e.g., AI0, AI1, etc.,) is high (approximately 500kΩ); therefore a 10nF capacitor is sufficient to decouple the DC bias[1]. Keep audio input traces strictly away from output traces. Microphone ground terminals should be connected to the AGND plane (if present) or share a trace with the input ground reference voltage pin (AIR) to the star point.

Analog and digital outputs MUST be kept away from microphone inputs.

3.4 Audio Outputs

The audio output traces should be as short as possible. If the direct digital output is used, the trace length of RCVRx+ and RCVRx- should be approximately the same to provide matched impedances. If the analog audio output is used, the ground return for the external power amplifier should share a trace with the output ground reference voltage pin (AOR) to the star point.

[1] The capacitor and the internal resistance form a first-order analog high pass filter whose cutoff frequency can be calculated by f_{3dB} (Hz) = 1/(R·C·2π), which results with ~30Hz for 10nF capacitor.

4.0 Mechanical and Environmental Information

BelaSigna 200 is available in two packages:

- The QFN package measures 8x8mm, has easy-to-probe signals and all I/O available.
- The CSP package is the ultra-miniature option, measuring only 2.3x3.7mm; this package has reduced I/O and flexibility, but still meets a wide range of application needs.

4.1 QFN Package Option

4.1.1. QFN Mechanical Information

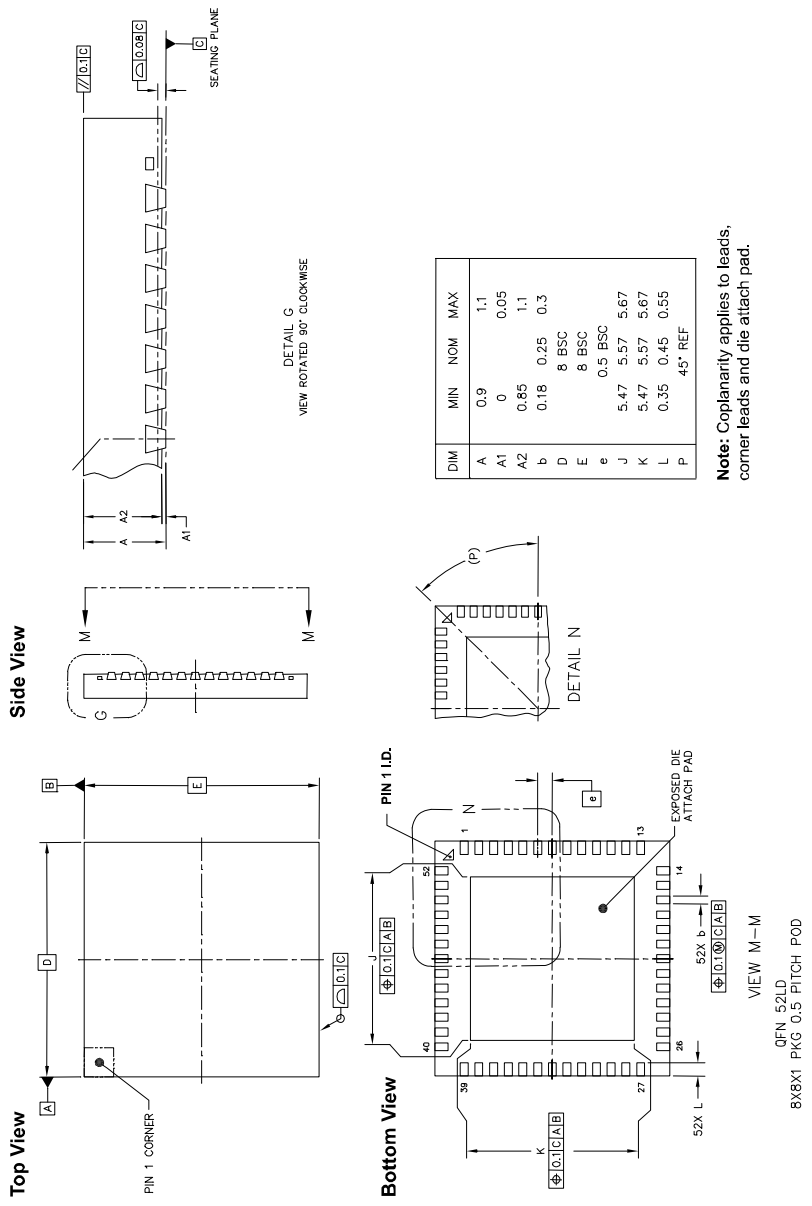


Figure 3: QFN Mechanical Drawings

4.1.3. QFN Environmental Characteristics

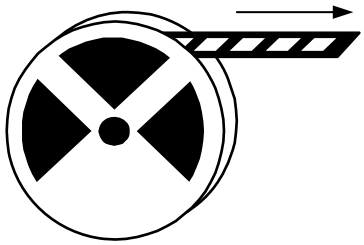
All parts supplied against this specification have been qualified as follows:

Table 3: Environmental Characteristics

Characteristics	
Packaging Level	
Moisture sensitivity level	JEDEC Level 3 30°C / 60% RH for 192 hours
Pressure cooker test (PCT)	121°C / 100% RH / 2 atm for 168 hours
Thermal cycling test (TCT)	-65°C to 150°C for 1000 cycles
Highly accelerated stress test (HAST)	130°C / 85% RH for 100 hours
High temperature stress test (HTST)	150°C for 1000 hours
Board Level	
Temperature	-40°C to 125°C for 2500 cycles with no failures
Drop	1m height with no failures
Bending	1mm deflection / 2Hz

4.1.4. QFN Carrier Information

ON Semiconductor offers tape and reel packing for BelaSigna 200 QFN packages. The packing consists of a pocketed carrier tape, a cover tape, and a molded anti-static polystyrene reel. The carrier and cover tape create an ESD safe environment, protecting the QFNs from physical and electro-static damage during shipping and handling.



Reel Diameter: 13 inches
Quantity Per Reel: 500 pieces
Date Codes: Max. of two date codes can be combined into one reel

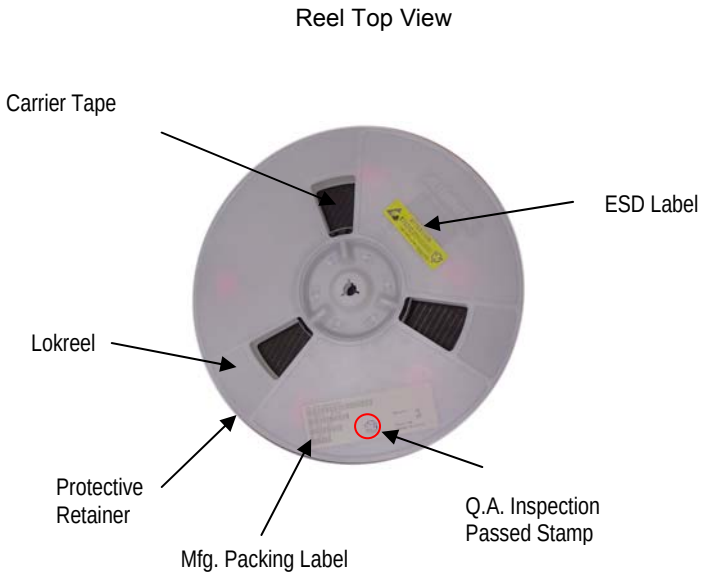


Figure 4: QFN Reel Format

4.2.2. CSP Pad Out

Table 4: Pad Out (Advance Information)

Pad Index	Pad Name	Pad Function	I/O	U/D
B2	CAP0	Charge pump capacitor pin 0	N/A	N/A
A2	CAP1	Charge pump capacitor pin 1	N/A	N/A
A1	VDBL	Double voltage	O	N/A
C3	VREG	Regulated voltage for microphone bias	O	N/A
B3	A|0	Audio signal input to ADC0	I	N/A
B1	A|1/LOUT	Audio signal input to ADC0/line level output signal from preamp 0	I/O	N/A
C2	A|2	Audio signal input to ADC1	I	N/A
C1	A|3	Audio signal input to ADC1	I	N/A
B4	A|R	Reference voltage for microphone	N/A	N/A
C4	AGND	Analog ground	N/A	N/A
D1	AOR	Reference voltage for DAC	N/A	N/A
E1	AO1/RCVR1-	Audio signal output from DAC1/output from direct digital drive 1-	O	N/A
D2	AO0/RCVR1+	Audio signal output from DAC0/output from direct digital drive 1+	O	N/A
D3	RCVR0-	Output from direct digital drive 0	O	N/A
E3	RCVR0+	Output from direct digital drive 0	O	N/A
D4	RCVRGND	Receiver return current	N/A	N/A
E2	VBAT	Positive power supply	I	N/A
E5	VDD	Core logic, EEPROM and pad supply	I	N/A
A6	GNDO	Digital pads ground	N/A	N/A
E6	GNDC	Core logic and pads ground	N/A	N/A
D6	EXT_CLK	External clock input/internal clock output	I/O	U
E7	DEBUG_RX	Debug port receive	I	U
D7	DEBUG_TX	Debut port transmit	O	U
E8	TWSS_SDA	TWSS data	I/O	U
D8	TWSS_CLK	TWSS clock	I	U
C8	SPI_SERO	Serial peripheral interface serial data out	I/O	D
C7	SPI_SERI	Serial peripheral interface serial data in	I	U
B8	SPI_CS	Serial peripheral interface chip select	I/O	D
C6	SPI_CLK	Serial peripheral interface clock	I/O	N/A
A8	GPIO[14]/PCM_FRAME	General-purpose I/O/PCM interface frame	I/O	U
B7	GPIO[13]/PCM_OUT	General-purpose I/O/PCM interface output	I/O	U
A7	GPIO[12]/PCM_IN	General-purpose I/O/PCM interface input	I/O	U
B6	GPIO[11]/PCM_CLK	General-purpose I/O/PCM interface clock	I/O	U
A5	GPIO[10]/DCLK	General-purpose I/O/class D receiver clock	I/O	U
B5	LSAD[5]/GPIO[9]/UART_RX	Low-speed A/D/general-purpose I/O/general-purpose UART receive	I/O	U
A4	LSAD[4]/GPIO[8]/UART_TX	Low-speed A/D input/general-purpose I/O/general-purpose UART transmit	I/O	U
C5	LSAD[3]/GPIO[7]	Low-speed A/D input/general purpose I/P	I/O	U
A3	LSAD[1]/GPIO[5]/I2S_OUT A	Low-speed A/D inputs/general-purpose I/O/I2S interface analog blocks output	I/O	U
D5	LSAD[0]/GPIO[4]/I2S_OUT D	Low-speed A/D inputs/general-purpose I/O/I2S interface analog blocks output	I/O	U
E4	GPIO[3]/ NCLK_DIV_RESET/I2S_FA	General-purpose I/O/clock divider reset/I2S interface analog blocks frame output	I/O	U

4.2.3. CSP Environmental Characteristics

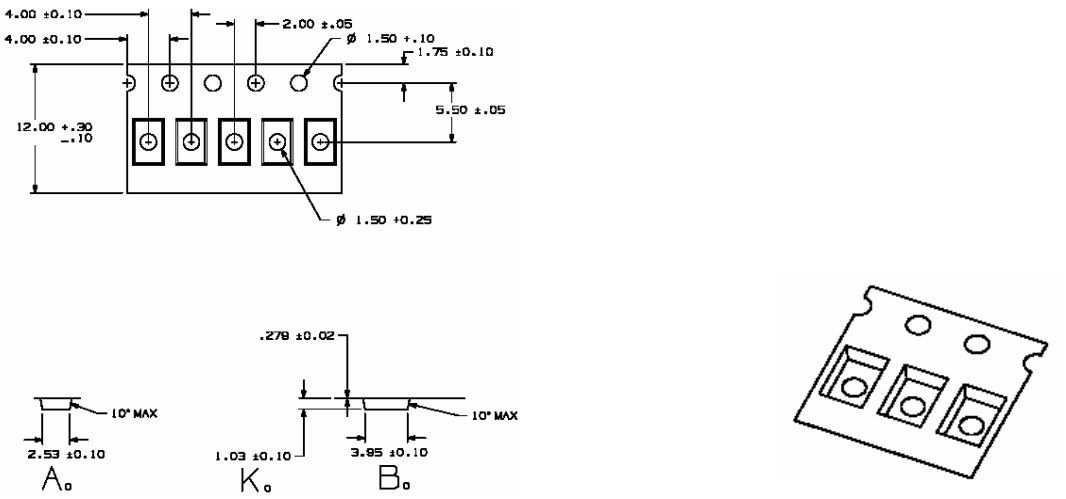
All parts supplied against this specification have been qualified as follows:

Table 5:

Packaging Level	
Moisture sensitivity level (MSL)	JEDEC Level 3 30°C / 60% RH for 192 hours
Pressure cooker test (PCT)	121°C / 100% RH / 2 atm for 168 hours
Thermal cycling test (TCT)	-65°C to 150°C for 1000 cycles
Highly accelerated stress test (HAST)	130°C / 85% RH for 100 hours
High temperature stress test (HTST)	150°C for 1000 hours
Board Level	
Temperature	-40°C to 125°C for 1000 cycles with no failures (for board thickness <40mils and underfilled CSP)
Drop	1m height with no failures

4.2.4. CSP Carrier Information

The devices will be provided in standard 7” Tape & Reel carrier with 5,000 parts per reel.



Note: all dimensions in millimeters

Figure 8: CSP Tape Dimensions

4.2.5. CSP Design Considerations

In order to achieve the highest level of miniaturization, the CSP package is constrained in ways that will factor into design decisions. The CSP will only operate in HV mode, and therefore requires a 1.8V operating voltage. The number of pins is reduced to 40 (compared to 49 active pins on the QFN). This reduction eliminates access to GPIOs (0,1,2,6,15), LSAD 2, the I2S interface, and the IR remote receiver.

For PCB manufacture with BelaSigna 200 CSP, ON Semiconductor recommends Solder-on-Pad (SoP) surface finish. With SoP, the solder mask opening should be solder mask-defined and copper pad geometry will be dictated by the PCB vendor’s design requirements.

6.0 Architecture Overview

6.1 RCore DSP

The RCore is a 16-bit fixed-point, dual-Harvard-architecture DSP. It includes efficient normalize and de-normalize instructions, plus support for double-precision operations to provide the additional dynamic range needed for many applications. All memory locations in the system are accessible by the RCore using several addressing modes including indirect and circular modes. The RCore generally assumes master functionality of the system.

6.1.1. RCore DSP Architecture

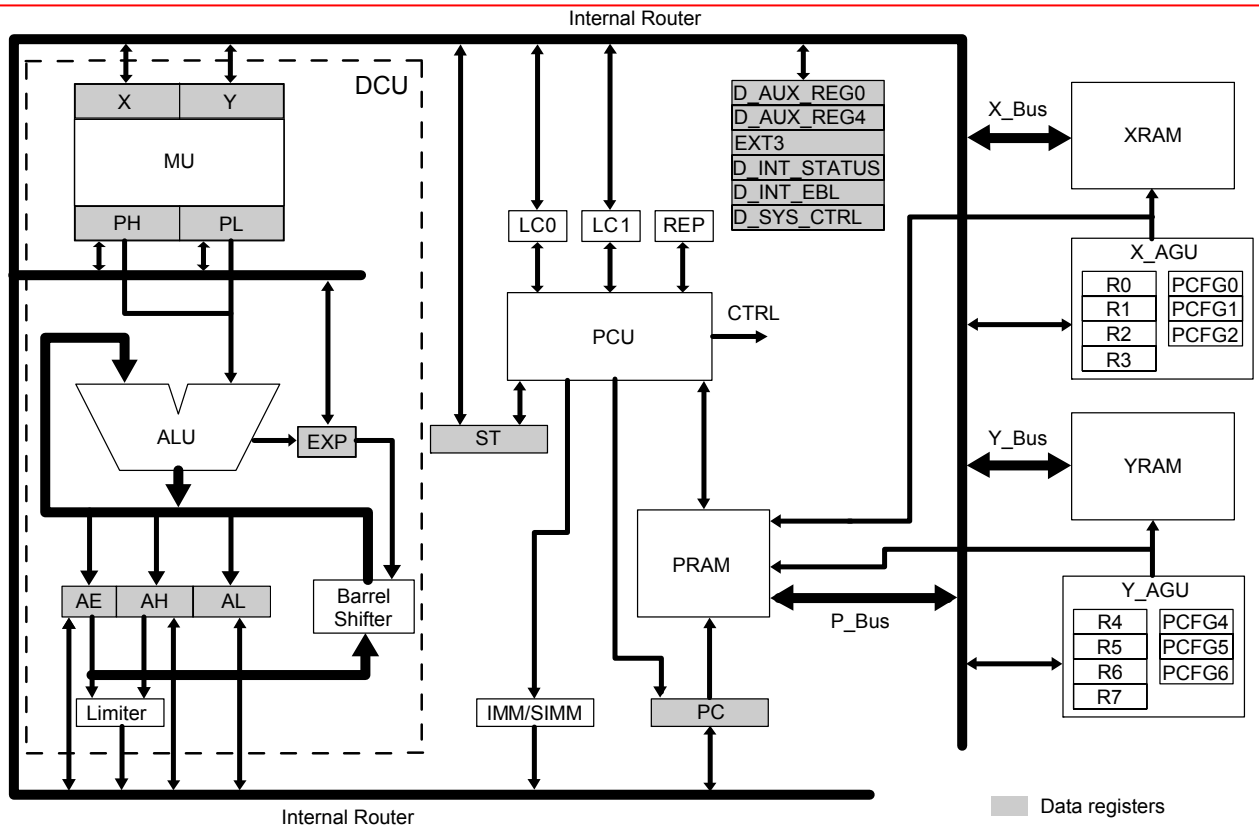


Figure 9: RCore Programming Model

The RCore is a single-cycle pipelined multiply-accumulate (MAC) architecture that feeds into a 40-bit accumulator complete with barrel shifter for fast normalization and de-normalization operations. Program execution is controlled by a sequencer that employs a three-stage pipeline (FETCH, DECODE, EXECUTE). Furthermore, the RCore incorporates pointer configuration registers for low cycle-count address generation when accessing the three memories: program memory (PRAM), X data memory (XRAM) and Y data memory (YRAM).

6.1.2. Instruction Set

The RCore instruction set can be divided into the following three classes:

1. Arithmetic and Logic Instructions

The RCore uses two's complement fractional as a native data format. Thus, the range of valid numbers is [-1; 1), which is represented by 0x8000 to 0x7FFF. Other formats can be utilized by applying appropriate shifts to the data.

The multiplier takes 16-bit values and performs a multiplication every time an operand is loaded into either the X or Y register. A number of instructions that allow loading of X and Y simultaneously and addition of the new product to the previous product (a MAC operation), are available. Single-cycle MAC with data pointer update and fetch is supported.

The arithmetic logic unit (ALU) receives its input from either the accumpulator (AE|AH|AL) or the product register (PH|PL). Although the RCORE is a 16-bit system, 32-bit additions or subtractions are also supported. Bit manipulation is also available on the accumulator as well as operations to perform arithmetic or logic shifts, toggling of specific bits, limiting, and other functions.

2. Data Movement Instructions

Data movement instructions transfer data between RAM, control registers and the RCore’s internal registers (accumulator, PH, PL, etc).

Two address generators are available to simultaneously generate two addresses in a single cycle. The address pointers R0..2 and R4..6 can be configured to support increment, decrement, add-by-offset, and two types of modulo-N circular buffer operations. Single-cycle access to low X memory or low Y memory as well as two-cycle instructions for immediate access to any address are also available.

3. Program Flow Control Instructions

The RCore supports repeating of both single-word instructions and larger segments of code using dedicated repeat instructions or hardware loop counters. Furthermore, instructions to manipulate the program counter (PC) register such as calls to subroutines, conditional branches and unconditional branches are also provided.

7.1 Weighted Overlap-Add (WOLA) Filterbank Coprocessor

The WOLA coprocessor performs low-delay, high-fidelity filterbank processing to provide efficient time-frequency processing. The coprocessor stores intermediate data values, program code and window coefficients in its own memory space. Audio data are accessed directly from the input and output FIFOs where they are automatically managed by the IOP.

The WOLA coprocessor can be configured to handle different sizes and types of transforms, such as mono, simple stereo or full stereo configurations. The number of bands, the stacking mode (even or odd), the oversampling factor, and the shape of the analysis and synthesis windows used are all configurable. The selected set of parameters affects both the frequency resolution, the group delay through the WOLA coprocessor and the number of cycles needed for complete execution.

The WOLA coprocessor can generate both real and complex data. Either real or complex gains can be applied. The RCore always has access to these values through shared memories. All parameters are configurable with microcode, which is used to control the WOLA during execution.

The RCore initiates all WOLA functions (analysis, gain applications, synthesis) through dedicated control registers. A dedicated interrupt is used to signal completion of a WOLA function.

Many standard WOLA microcode configurations are delivered with the EDK. These configurations have been specially designed for low group delay and high fidelity.

7.2 Input Output Processor (IOP)

The IOP is an audio-optimized configurable DMA unit for audio data samples. It manages the collection of data from the A/D converters to the input FIFO and feeds digital data to the audio output stage from the output FIFO. The IOP can be configured to access data in the FIFOs in four different ways:

- **Mono mode:** Input samples are stored sequentially in the input FIFO. Output samples are stored sequentially in the output FIFO.
- **Simple stereo mode:** Input samples from the two channels are stored interleaved in the input FIFO. Output samples for the single output channel are stored in the lower part of the output FIFO.
- **Digital mixed mode:** Input samples from the two channels are stored in each half of the input FIFO. Output samples for the single output channel are stored in the lower half of the output FIFO.
- **Full stereo mode:** Input samples from the two channels are stored interleaved in the input FIFO. Output samples for the two output channels are stored interleaved in the output FIFO. (Note: A one-in, two-out configuration can be achieved in this mode by leaving the second input unused).

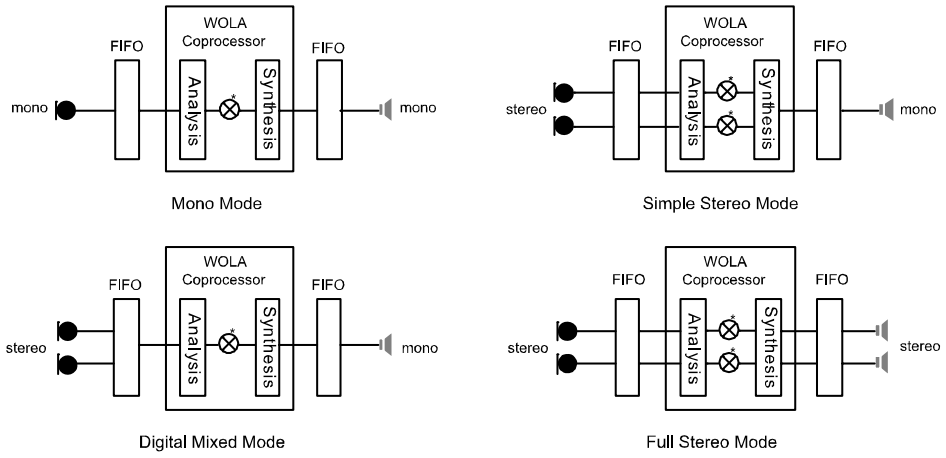


Figure 10: Four Audio Modes

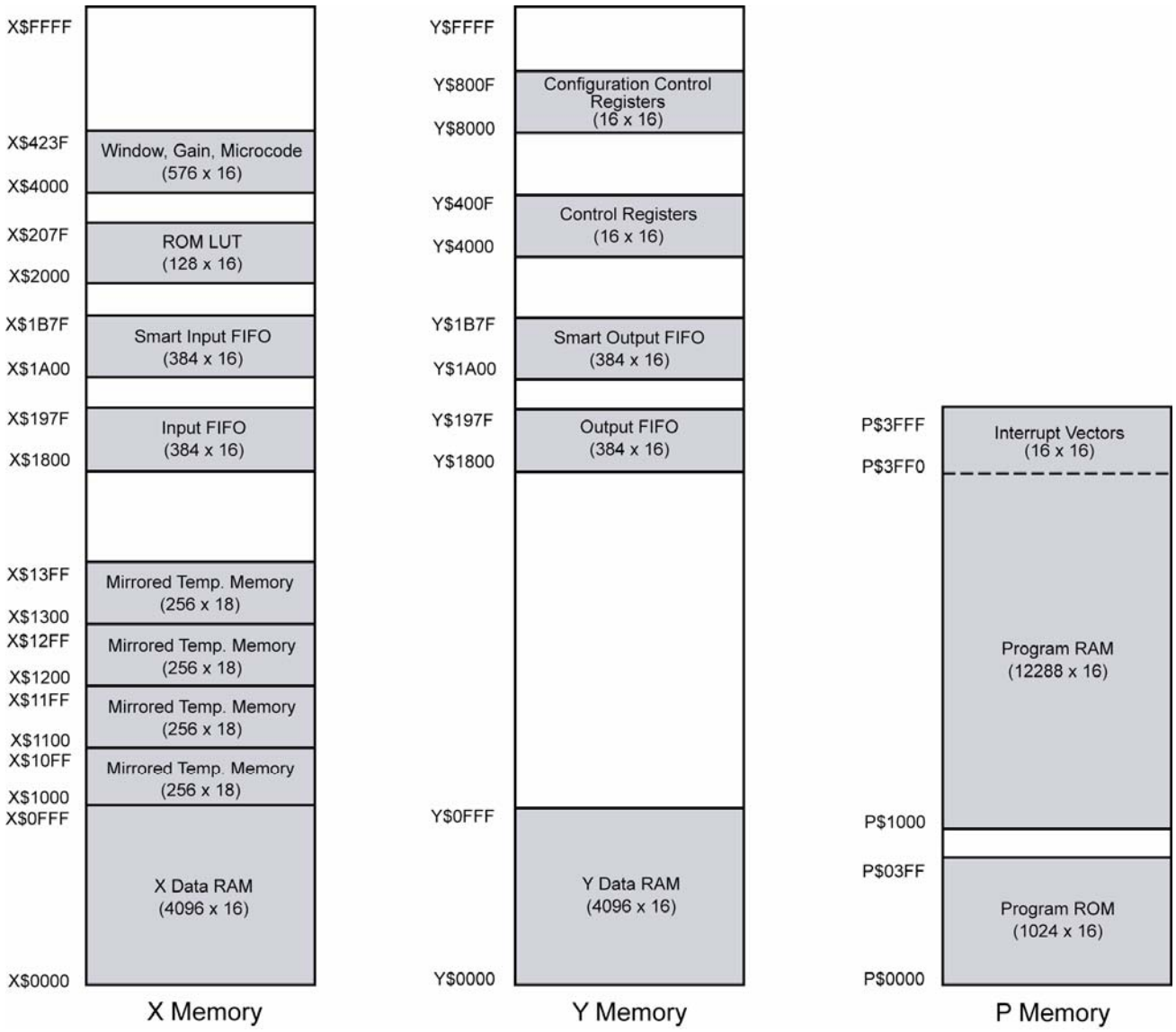


Figure 11: Memory Maps

7.6 Interrupts

The RCore DSP has a single interrupt channel that serves eleven interrupt sources in a prioritized manner. The interrupt controller also handles interrupt acknowledge flags. Every interrupt source has its own interrupt vector. Furthermore, the priority scheme of the interrupt sources can be modified. Refer to Table 9 for a description of all the interrupts.

8.0 Description of Analog Blocks

8.1 Input Stage

The analog audio input stage is comprised of two individual channels. For each channel, one of two possible inputs is routed to the input of the programmable preamplifier that can be configured for bypass or gain values of 12 to 30dB (3-dB steps).

The analog signal is filtered to remove frequencies above 10kHz before it is passed into the high-fidelity 16-bit oversampling ΣΔ A/D converter. Subsequently, any necessary sample rate decimation is performed to downsample the signal to the desired sampling rate. During decimation the level of the signal can be adjusted digitally for optimal gain matching between the two input channels. Any undesired DC component can be removed by a configurable DC-removal filter that is part of the decimation circuitry. The DC removal filter can be bypassed or configured for cut-off frequencies at 5, 10 and 20Hz.

A built-in feature allows a sampling delay to be configured between channel zero and channel one. This is useful in beam-forming applications.

For power consumption savings either of the input channels can be disabled via software.

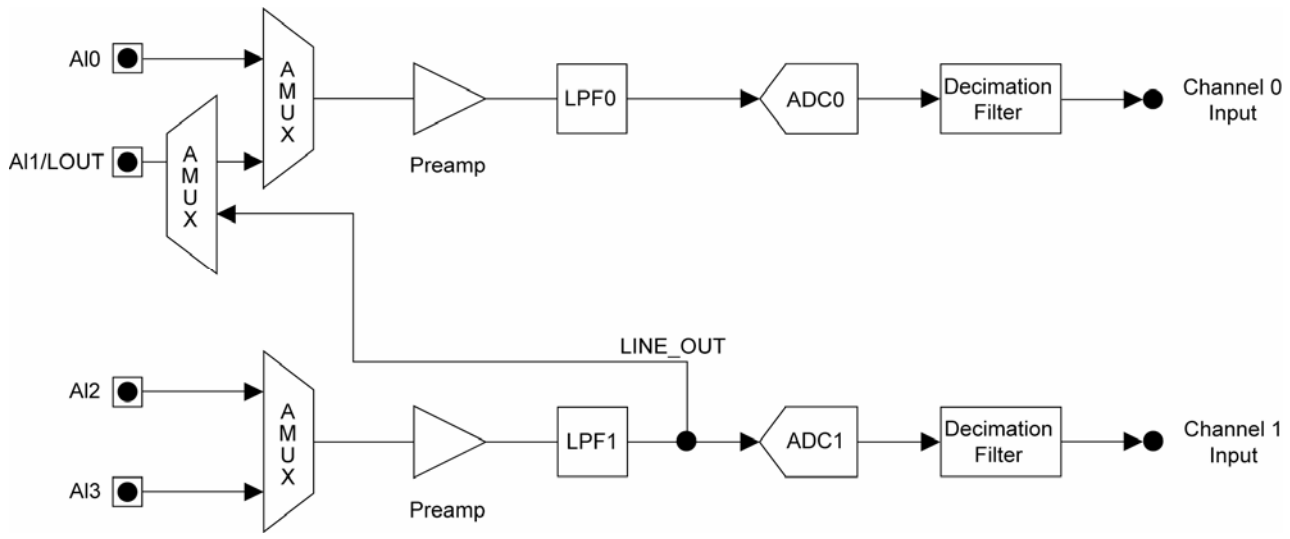


Figure 12: Input Stage

8.2 Output Stage

The analog audio output stage is composed of two individual channels. The first part of the output stage interpolates the signal for highly oversampled D/A conversion and automatically configures itself for the desired oversampling rate. Here, the signal is routed to both the ΣΔ D/A converter and the direct digital outputs. The D/A converter translates the signal into a high-fidelity analog signal and passes it into a reconstruction filter to smooth out the effects of sampling. The reconstruction filter has a fixed cut-off frequency at 10kHz.

From the reconstruction filter, the signal passes through the programmable output attenuator, which can adjust the signal for various line-level outputs or mute the signal altogether. The attenuator can be bypassed or configured to a value in the interval -12 to -30dB (3-dB steps).

The direct digital output provides a bridge driven by a pulse-density modulated output that can be used to directly drive an output transducer without the need for an external power amplifier.

9.2 External Analog Interfaces

9.2.1. Low-Speed A/D Converters (LSAD)

Six LSAD inputs are available on BelaSigna 200. Combined with two internal LSAD inputs (supply and ground) this gives a total of eight multiplexed inputs to the LSAD converter. The multiplexed inputs are sampled sequentially at 1.6kHz per channel. The native data format for the LSAD is 10-bit two's complement. However, a total of eight operation modes are provided that allow a configurable input dynamic range in cases where certain minimum and maximum values for the converted inputs are desired; such as in the case of a volume control where only input values up to a certain magnitude are allowed.

11.3 Analog Characteristics

Conditions: Temperature = 25°C, f_{SYS_CLK} = 1.28MHz (internal), f_{MCLK} = 1.28MHz, f_{SAMP} = 16kHz, V_{bat} = 1.8V

Table 12: Analog Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Stage						
Input voltage	Vin	AI0, AI1, AI2, AI3 inputs 0dB preamp gain	-1		1	Vp
Input impedance[5]	Rin	Preamplifier gain 12, 15, 18, 21, 24, 27, 30dB	385	550	715	kΩ
Input referred noise	IRN	Unweighted, 20Hz to 8kHz BW, 30dB preamp gain		3		µVrms
Input dynamic range		Unweighted, 20Hz to 8kHz BW, 0dB preamp gain		85		dB
Input THD+N		Unweighted, 20Hz to 8kHz BW, 0dB preamp gain, input at 1 kHz		-60		dB
Preamplifier gain tolerance (0, 12, 15, 18, 21, 24, 27, 30dB)		50% re. FS input at 1kHz	-1.5		1.5	dB
Output Stage						
Line out output level	Vlo	AI1	-1		1	Vp
Line out output impedance	Rlo	AI1		5		kΩ
Output impedance[6]	Rao	AO0. Attenuator = 12, 15, 18, 21, 24, 27, 30dB	8.9	12.8	16.6	kΩ
Output dynamic range		Unweighted, 100Hz to 22kHz BW, 0dB output attenuation		75		dB
Output THD+N		Unweighted, 100Hz to 22kHz BW, 0dB output attenuation, input at 1kHz		-60		dB
Output attenuator tolerance (0,12,15,18,21,24,27,30dB)		50% re. FS input at 1kHz	-2		2	dB
Low-Speed A/D						
Input voltage		Peak input voltage, HV mode	-0.3		2.1	V
Sampling frequency		All channels sequentially MCLK = 1.28MHz		12.8		kHz
Channel frequency		8 channels		1.6		kHz
Anti-Aliasing Filters (Input and Output)						
Cut-off frequencies			7	10	13	kHz
Passband flatness			-1		1	dB
Stopband attenuation				80		dB

[5] Depends slightly on the preamp gain
[6] Depends strongly on the attenuator

12.1.2. 32-bit

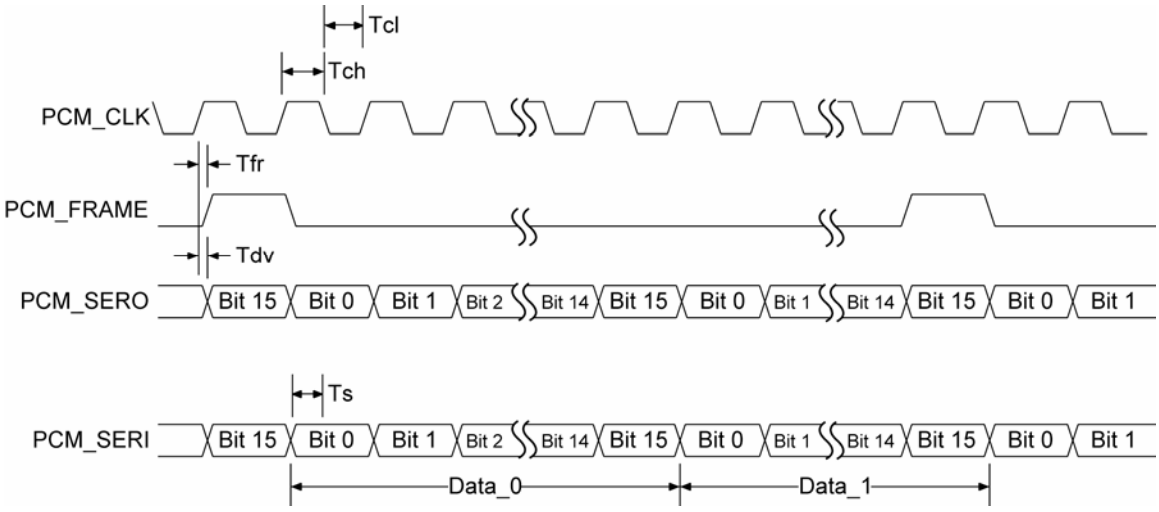


Figure 22: LSB Advanced Short

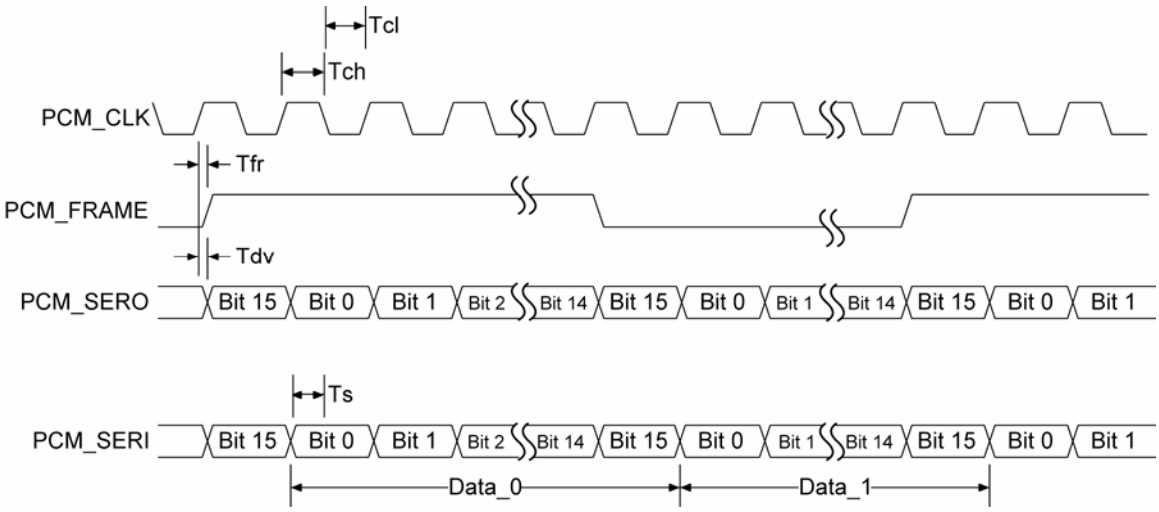


Figure 23: LSB Advanced Wide

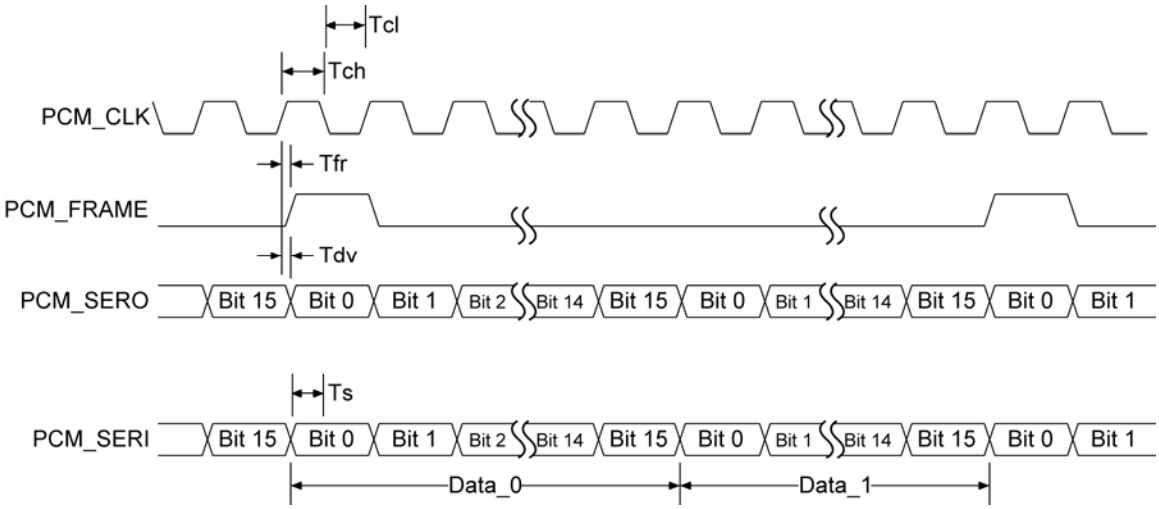


Figure 24: LSB Del Short

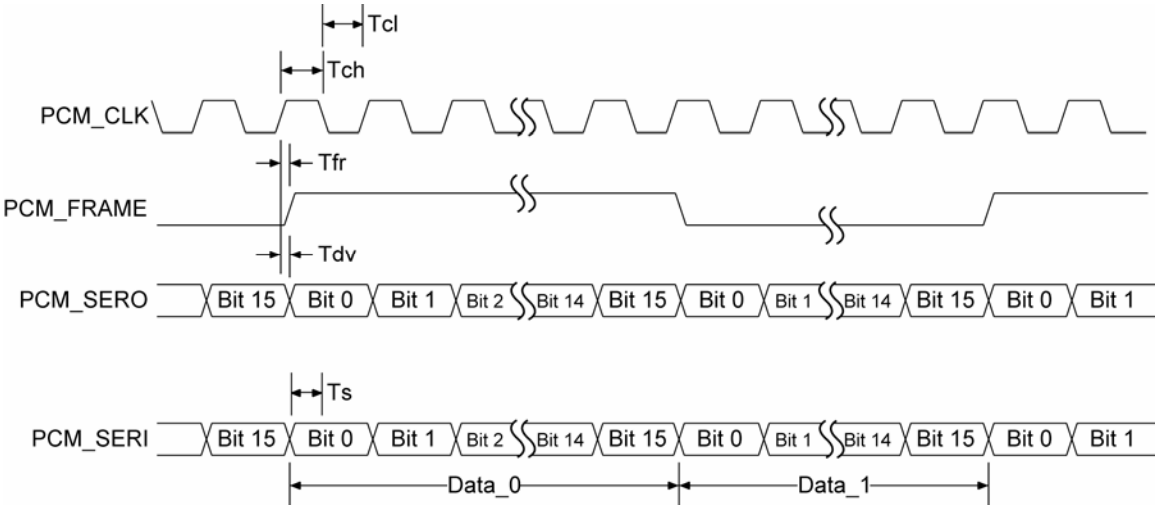


Figure 25: LSB Del Wide

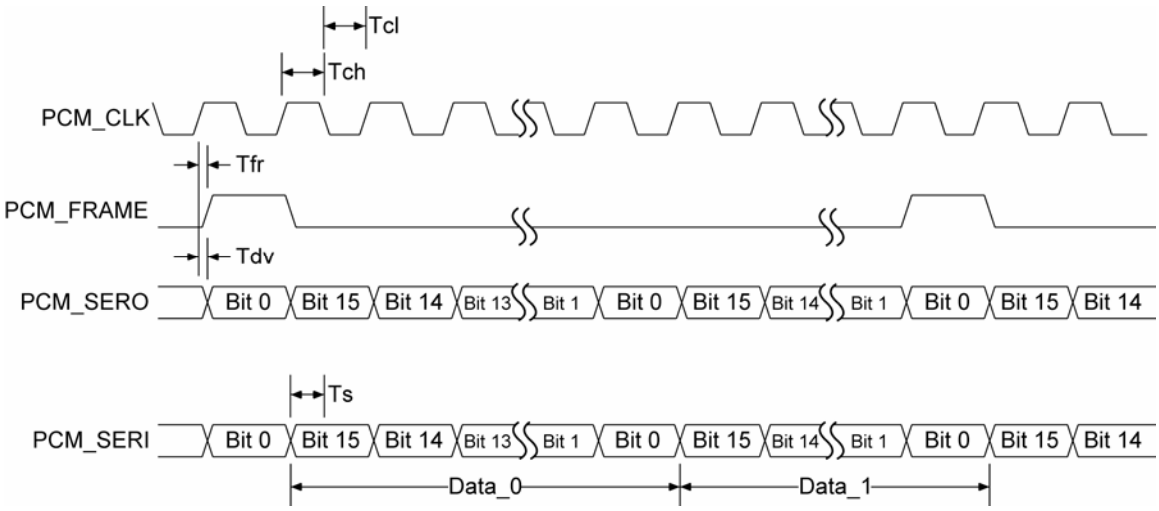


Figure 26: MSB Advanced Short

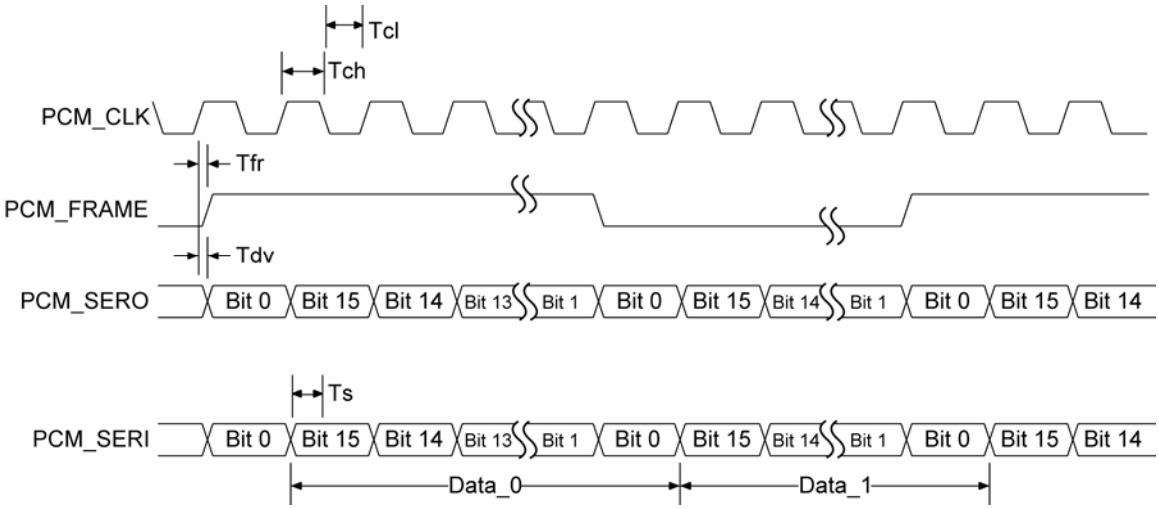


Figure 27: MSB Advanced Wide

12.2 GPIO Timing Diagram

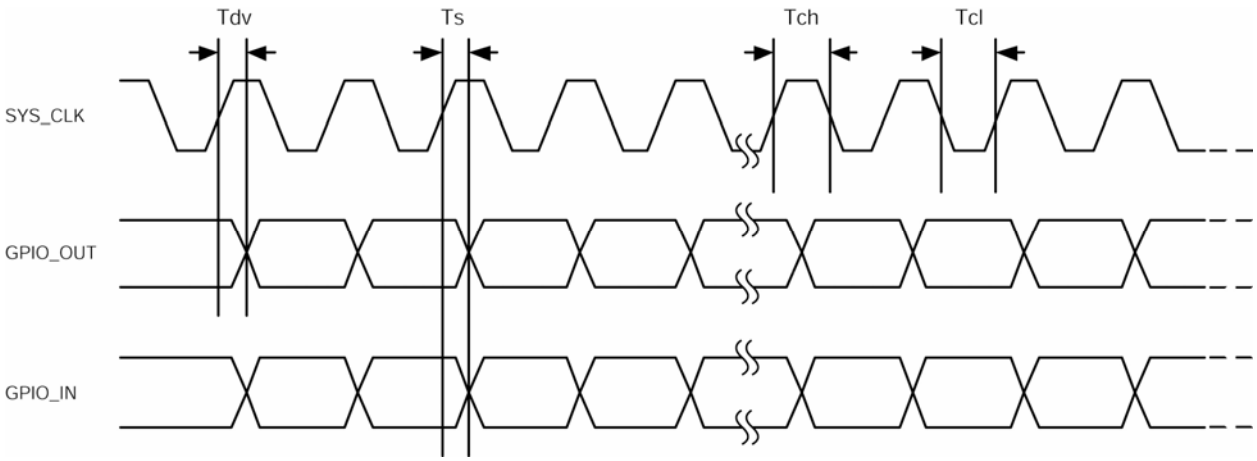


Figure 30: GPIO Timing Diagram

Table 15: GPIO Interface Descriptions

Parameter	Description	Min.	Max.	Unit
T_{dv}	SYS_CLK high to data valid		50	ns
T_s	Setup time before SYS_CLK high		10	ns
T_{ch}	SYS_CLK high period (1.28MHz)		390	ns
T_{cl}	SYS_CLK low period (1.28MHz)		390	ns

12.3 SPI Port Timing Diagram

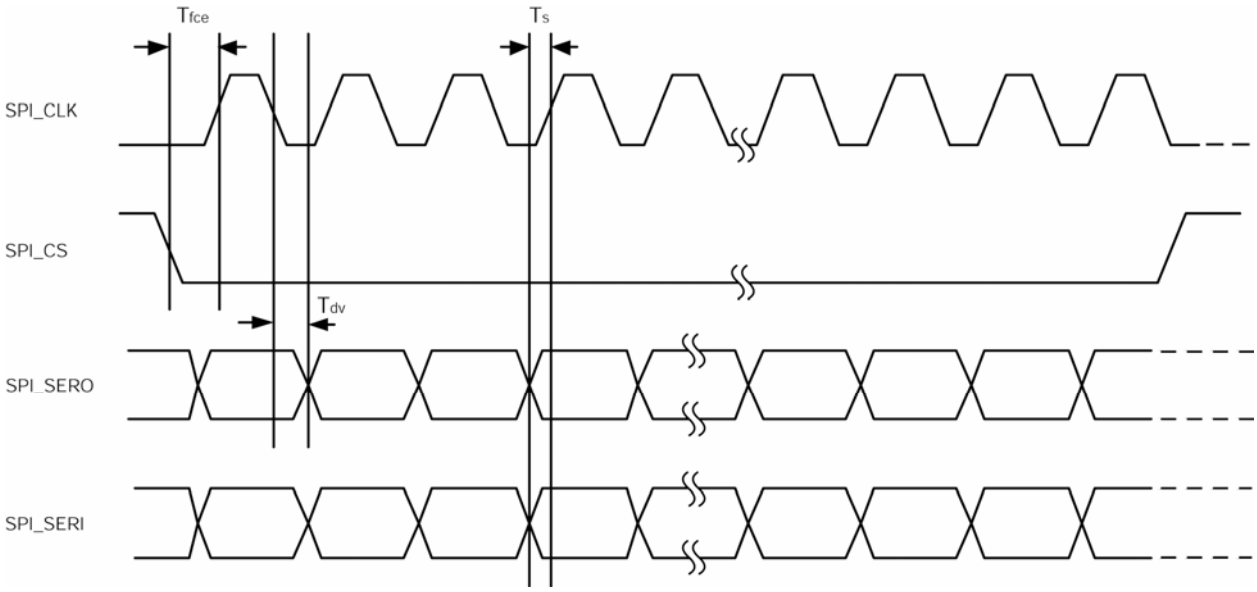


Figure 31: SPI Port Timing Diagram

Table 16: SPI Interface Descriptions

Parameter	Description	Min.	Max.	Unit
T_{dv}	SPI_CLK high to output data valid		50	ns
T_s	Setup time before SPI_CLK high		10	ns
T_{fce}	SPI_CS low to first SPI_CLK high			ns

16.0 Ordering Information

Part Number	Package	Shipping Configuration	Temperature Range
0W344-004-XTP	8x8mm QFN	Tape & Reel (500 parts per reel)	-85 to 40 °C
0W344-005-XTP	8x8mm QFN	Tape & Reel (1000 parts per reel)	-85 to 40 °C
0W588-002-XUA	2.3x2.8mm WLCSP	Tape & Reel (5000 parts per reel)	-85 to 40 °C

17.0 Company or Product Inquiries

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