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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	8-Bit
Speed	18MHz
Connectivity	SIO, UART/USART
Peripherals	LCD, PWM, WDT
Number of I/O	29
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP/QIP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc87f7np6avuej-2h

Function Details

■Ports

- Normal withstand voltage I/O ports
  Ports whose I/O direction can be designated in 1 bit units: 29 (P0n, P1n, P70 to P73, P8n, XT2)
- Normal withstand voltage input port: 1 (XT1)
- LCD ports
  - Segment output: 54 (S00 to S53)
  - Common output: 4 (COM0 to COM3)
  - Bias power sources for LCD driver: 3 (V1 to V3)

  Other functions
  - Input/output ports: 54 (P3n, PAn, PBn, PCn, PDn, PEn, PFn)
  - Input ports: 7 (PLn)
- Dedicated oscillator ports: 2 (CF1, CF2)
- Reset pins: 1 ($\overline{\text{RES}}$)
- Power pins: 6 ($V_{SS}1$ to $V_{SS}3$, $V_{DD}1$ to $V_{DD}3$)

■LCD Controller

1) Seven display modes are available (static, 1/2, 1/3, 1/4 duty × 1/2, 1/3 bias)
2) Segment output and common output can be switched to general-purpose input/output ports

■Small Signal Detection (MIC signals etc.)

1) Counts pulses with a level which is greater than a preset value
2) 2-bit counter

■Timers

- Timer 0: 16-bit timer/counter with two capture registers.
  - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels
  - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit counter (with two 8-bit capture registers)
  - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)
  - Mode 3: 16-bit counter (with two 16-bit capture registers)
- Timer1: 16-bit counter timer that supports PWM/toggle outputs
  - Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer counter with an 8-bit prescaler (with toggle outputs)
  - Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  - Mode 2: 16-bit counter timer with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8 bits)
  - Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM.)
- Timer4: 8-bit timer with a 6-bit prescaler
- Timer5: 8-bit timer with a 6-bit prescaler
- Timer6: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer7: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer8: 16-bit timer
  - Mode 0: 8-bit timer with an 8-bit prescaler × 2 channels
  - Mode 1: 16-bit timer with an 8-bit prescaler
- Base Timer
  1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts programmable in 5 different time schemes
- Day and time counter
  1) Used with a base timer, the day and time counter can be used as a 65000 day + minute + second counter.

■High-speed Clock Counter
1) Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
2) Can generate output real-time.

■ Serial Interfaces
- SIO0: 8-bit synchronous serial interface
  1) LSB first/MSB first made selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3tCYC)
  3) Automatic continuous data transmission (1 to 256 bits specifiable in 1-bit units, suspension and resumption of data transmission possible in 1-byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■UART1
- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2 bits in continuous data transmission)
- Built-in baudrate generator

■UART2
- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2 bits in continuous data transmission)
- Built-in baudrate generator

■AD Converter : 12 bits × 15 channels

■PWM : Multi frequency 12-bit PWM × 2 channels

■ Infrared Remote Control Receiver Circuit1
1) Noise reduction function (Time constant of noise reduction filter: approx. 120μs, when selecting a 32.768kHz crystal oscillator as a reference clock)
2) Supporting reception formats with a guide-pulse of half-clock/clock/none.
3) Determines a end of reception by detecting a no-signal periods (No carrier).
(Supports same reception format with a different bit length.)
4) X'tal HOLD mode cancellation function

■Infrared Remote Control Receiver Circuit2
1) Noise reduction function
(Time constant of noise reduction filter: approx. 120μs, when selecting a 32.768kHz crystal oscillator as a reference clock.)
2) Supporting reception formats with a guide-pulse of half-clock/clock/none.
3) Determines a end of reception by detecting a no-signal periods (No carrier).
(Supports same reception format with a different bit length.)
4) X'tal HOLD mode cancellation function

■Watchdog Timer
1) External RC watchdog timer
2) Interrupt and reset signals selectable

■Clock Output Function
1) Can output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 as a system clock.
2) Can output the source oscillation clock for the sub clock.

■ Interrupt Source Flags

- 31 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4/remote control receiver1
4	0001BH	H or L	INT3/base timer/INT5/ remote control receiver2
5	00023H	H or L	T0H/INT6
6	0002BH	H or L	T1L/T1H/INT7
7	00033H	H or L	SIO0/UART1 receive/ UART2 receive/T8L/T8H
8	0003BH	H or L	SIO1/UART1 transmit/ UART2 transmit
9	00043H	H or L	ADC/MIC/T6/T7/PWM4/PWM5
10	0004BH	H or L	Port 0/T4/T5

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

- IFLG (List of interrupt source flag function)
  1) Shows a list of interrupt source flags that caused a branching to a particular vector address.

■Subroutine Stack Levels

- 4096/2048 levels maximum (The stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits

- RC oscillation circuit (internal): For system clock
- CF oscillation circuit: For system clock, with internal Rf and external Rd
- Crystal oscillation circuit: For low-speed system clock, with internal Rf and external Rd
- Multifrequency RC oscillation circuit (internal): For system clock
  1) Adjustable in ±4% (typ) increments from the selected center frequency.
  2) Measures the frequency of the source oscillation clock using the input signal from XT1 as the reference.

■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (at a main clock rate of 10MHz).

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation (Some parts of the serial transfer function stop operation) .
  1) Oscillation is not stopped automatically.
  2) Canceled by a system reset or occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, RC, X'tal, and multifrequency RC oscillators automatically stop operation.
  2) There are three ways of resetting the HOLD mode.
     (1) Setting the reset pin to the low level
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
     (3) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer and infrared remote controller circuit.
  1) The CF, RC, and multifrequency RC oscillators automatically stop operation.
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are five ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an interrupt source established in the base timer circuit
     (5) Having an interrupt source established in the infrared remote control receiver circuit

■On-chip Debugger Function

- Supports software debugging with the IC mounted on the target board.

■Package Form

- QIP100E(14×20) : Pb-Free/Halogen Free type
- TQFP100(14×14) : Pb-Free/Halogen Free type [Under Development]

■Development Tools

- On-chip Debugger: TCB87 TypeB +LC87F7Nxx A or TCB87 TypeC (3Lines Cable) +LC87F7NxxA

■Flash ROM Programming boards

Package	Programming Boards
QIP100E(14×20)	W87FQ100
TQFP100(14×14)	W87FSQ100

■Flash ROM Programmer

Maker		Model	Supported Version	Device
Flash Support Group, Inc (FSG)	Single Programmer	AF9709C	(Note 2)	LC87F7NP6A LC87F7NJ2A LC87F7NC8A
	Gang Programmer	AF9723/AF9723B(main unit) (including models manufactured by Ando Electric Co., Ltd.)	(Note 2)	LC87F7NP6A LC87F7NJ2A LC87F7NC8A
		AF9833(unit) (including models manufactured by Ando Electric Co., Ltd.)	(Note 2)	
Flash Support Group, Inc (FSG) +Our company (Note 1)	In-circuit Single/Gang Programmer	AF9101/AF9103(main unit) (manufactured by FSG)	(Note 2)	LC87F7NP6A LC87F7NJ2A LC87F7NC8A
		SIB87 Type C (Interface Driver) (Our company model)		
Our company	Single/Gang Programmer	SKK Type B / Type C (SanyoFWS)	Application Version 1.08or later Chip Data Version 2.44 later	LC87F7NP6A LC87F7NJ2A LC87F7NC8A
	In-circuit Single/Gang Programmer	SKK-DBG Type B /Type C (SanyoFWS)		

Contact information about the AF series:

Flash Support Group Company (TOA ELECTRONICS, Inc.)
Phone: 81-53-428-8380
E-mail: sales@j-fsg.co.jp

Note1: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from our company (SIB87) together can give a PC-less, standalone on-board-programming capabilities.

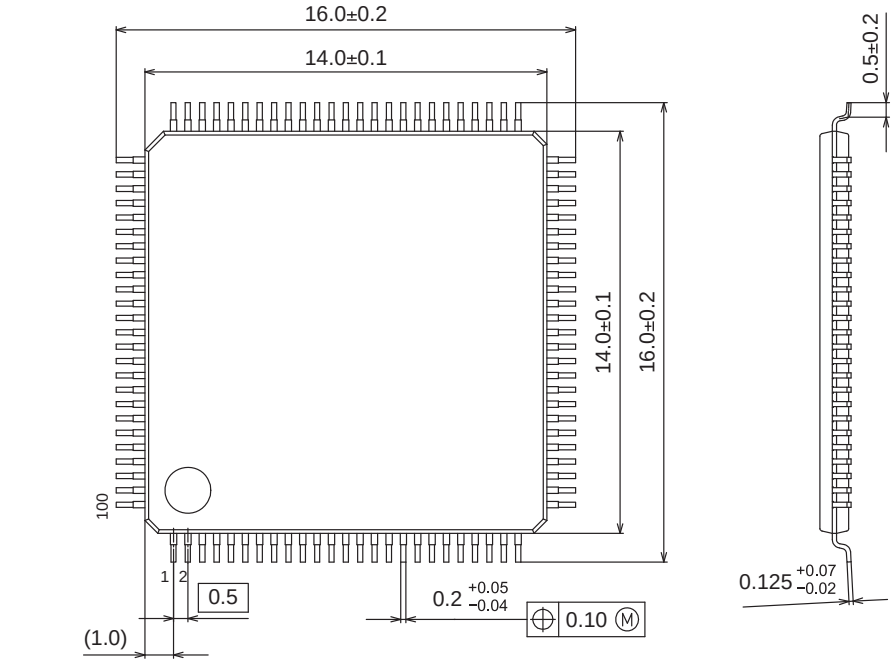
Note2: It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or our company for the information.

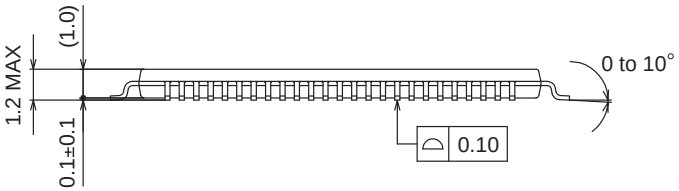
Package Dimensions

unit : mm

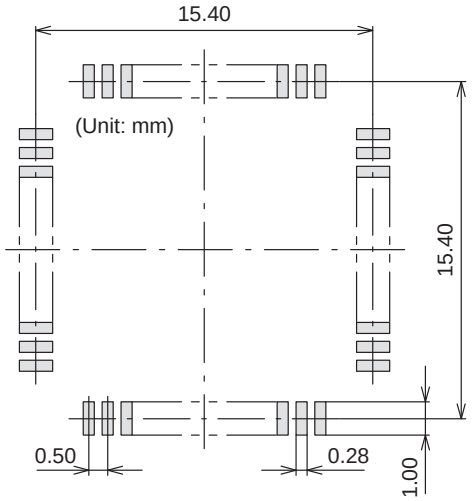
*Package TQFP100(14×14) type is Under Development.

TQFP100 14x14 / TQFP100
CASE 932AY
ISSUE A

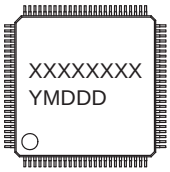




SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

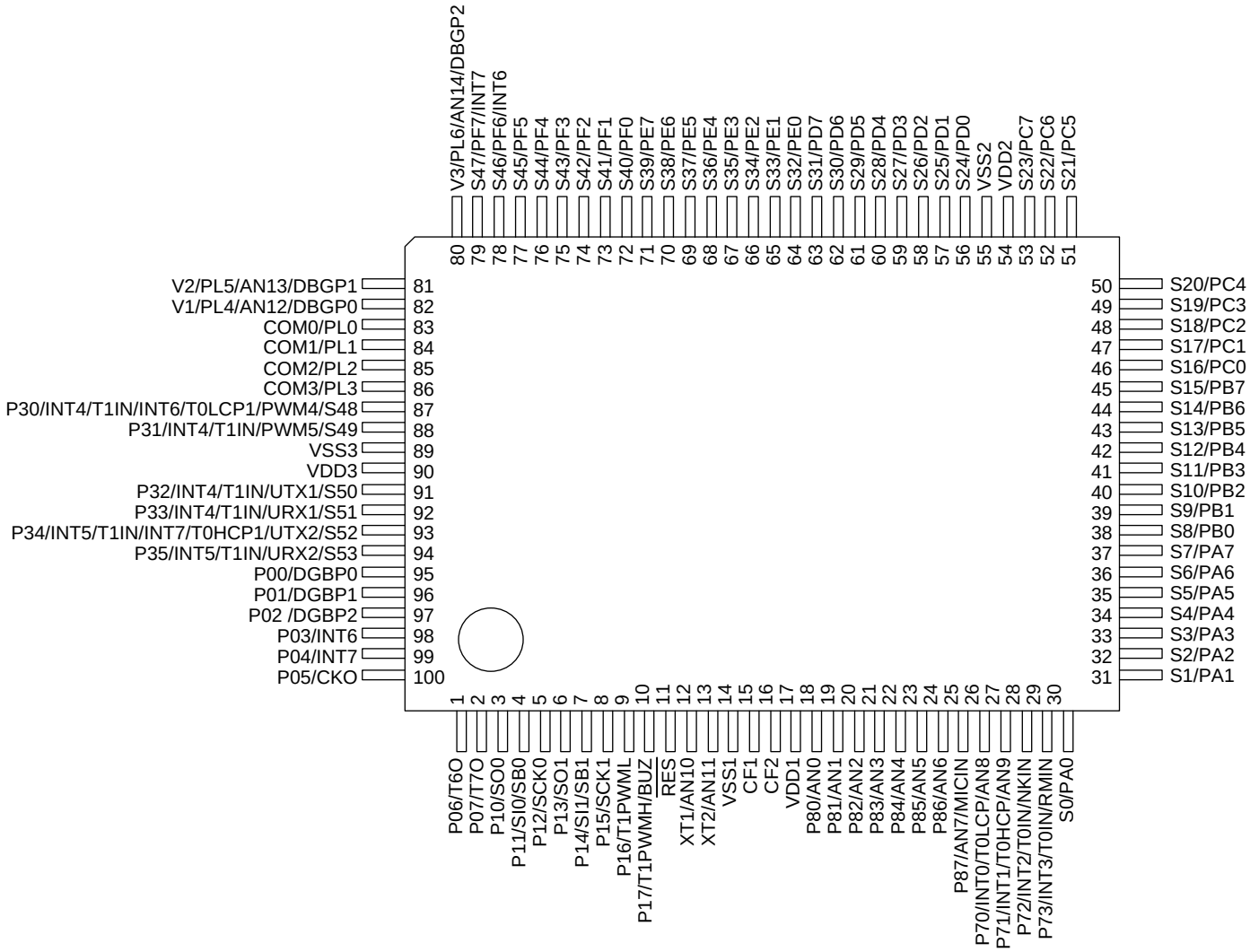
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

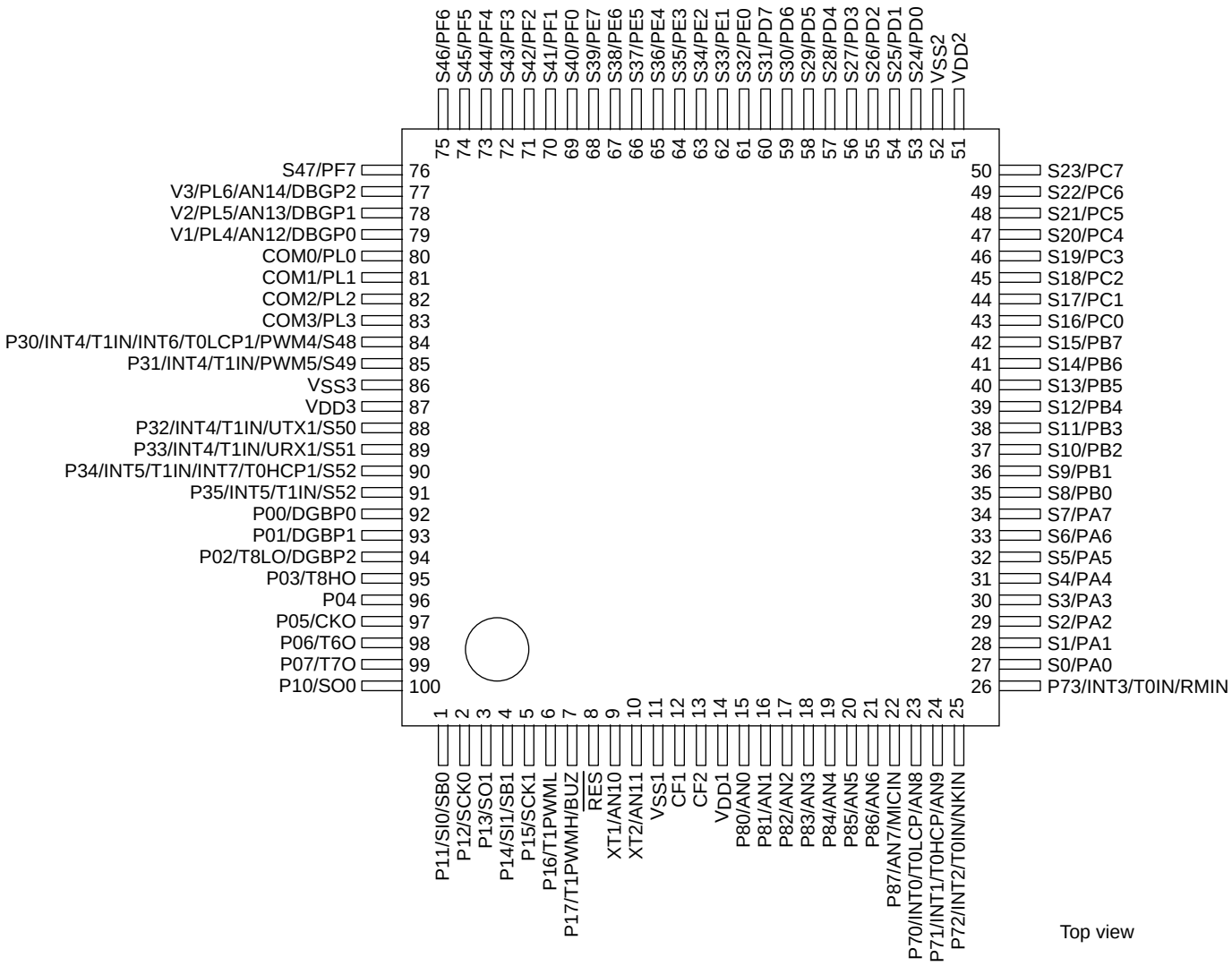
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin Assignment

QIP100E(14×20), Pb-Free/Halogen Free type



TQFIP100(14×14), Pb-Free/Halogen Free type [Under Development]



Top view

Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$
$V_{SS}2$
$V_{SS}3$</td><td>-</td><td>- power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}1$
$V_{DD}2$
$V_{DD}3$</td><td>-</td><td>+ power supply pin</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Input for HOLD release
• Input for port 0 interrupt
• Shared pins
P03: INT6 input
P04: INT7 input
P05: Clock output (system clock/can selected from sub clock)
P06: Timer 6 toggle output
P07: Timer 7 toggle output
On chip debugger pins: DBGP0 to DBGP2(P00 to P02)</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Shared pins
P10: SIO0 data output
P11: SIO0 data input/bus I/O
P12: SIO0 clock I/O
P13: SIO1 data output
P14: SIO1 data input/bus I/O
P15: SIO1 clock I/O
P16: Timer 1PWML output
P17: Timer 1PWMH output/beeper output</td><td>Yes</td></tr>
<tr><td>Port 3
P30 to P35</td><td>I/O</td><td>• 6-bit I/O port
• Segment output for LCD
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Shared pins
P30 to P33: INT4 input/HOLD release input/timer 1 event input/timer 0L capture input/ timer 0H capture input
P34 to P35: INT5 input/HOLD release input/timer 1 event input/timer 0L capture input/ timer 0H capture input
P30: PWM4 output/INT6 input/timer 0L capture 1 input
P31: PWM5 output
P32: UART1 transmit
P33: UART1 receive
P34: UART2 transmit/INT7 input/timer 0H capture 1 input
P35: UART2 receive
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT6</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT7</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
</table>

Continued on next page.

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<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Shared pins
P70: INT0 input/HOLD release input/timer 0L capture input/watchdog timer output
P71: INT1 input/HOLD release input/timer 0H capture input
P72: INT2 input/HOLD release input/timer 0 event input/timer 0L capture input/
high speed clock counter input
P73: INT3 input (with noise filter)/timer 0 event input/timer 0H capture input/
remote control receiver input
AD converter input ports: AN8 (P70), AN9 (P71)
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>Port 8
P80 to P87</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Shared pins
AD converter input ports: AN0 to AN7
Small signal detector input port: MICIN (P87)</td><td>No</td></tr>
<tr><td>S0/PA0 to
S7/PA7</td><td>I/O</td><td>• Segment output for LCD
• Can be used as general-purpose I/O port (PA)</td><td>No</td></tr>
<tr><td>S8/PB0 to
S15/PB7</td><td>I/O</td><td>• Segment output for LCD
• Can be used as general-purpose I/O port (PB)</td><td>No</td></tr>
<tr><td>S16/PC0 to
S23/PC7</td><td>I/O</td><td>• Segment output for LCD
• Can be used as general-purpose I/O port (PC)</td><td>No</td></tr>
<tr><td>S24/PD0 to
S31/PD7</td><td>I/O</td><td>• Segment output for LCD
• Can be used as general-purpose I/O port (PD)</td><td>No</td></tr>
<tr><td>S32/PE0 to
S39/PE7</td><td>I/O</td><td>• Segment output for LCD
• Can be used as general-purpose I/O port (PE)</td><td>No</td></tr>
<tr><td>S40/PF0 to
S47/PF7</td><td>I/O</td><td>• Segment output for LCD
• Can be used as general-purpose I/O port (PF)
PF6: INT6 input
PF7: INT7 input</td><td>No</td></tr>
<tr><td>COM0/PL0 to
COM3/PL3</td><td>I/O</td><td>• Common output for LCD
• Can be used as general-purpose input port (PL)</td><td>No</td></tr>
<tr><td>V1/PL4 to
V3/PL6</td><td>I/O</td><td>• LCD output bias power supply
• Can be used as general-purpose input port (PL)
• Shared pins
AD converter input ports: AN12 (V1) to AN14 (V3)
On-chip debugger pins: DBGP0 (V1) to DBGP2 (V3)</td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>Input</td><td>Reset pin</td><td>No</td></tr>
<tr><td>XT1</td><td>Input</td><td>• 32.768kHz crystal oscillator input pin
• Shared pins
General-purpose input port
Must be connected to $V_{DD}1$ if not to be used.
AD converter input port: AN10</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>• 32.768kHz crystal oscillator output pin
• Shared pins
General-purpose I/O port
Must be set for oscillation and kept open if not to be used.
AD converter input port: AN11</td><td>No</td></tr>
<tr><td>CF1</td><td>Input</td><td>Ceramic resonator input pin</td><td>No</td></tr>
<tr><td>CF2</td><td>Output</td><td>Ceramic resonator output pin</td><td>No</td></tr>
</table>

Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions	Specification				
					V_{DD} [V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	$V_{DD}1=V_{DD}2=V_{DD}3$		−0.3		+4.6	V
supply voltage for LCD		VLCD	V1/PL4, V2/PL5, V3/PL6	$V_{DD}1=V_{DD}2=V_{DD}3$		−0.3		V_{DD}	
Input voltage		V_I(1)	Port L XT1, CF1, $\overline{RES}$			−0.3		V_{DD}+0.3	
		V_I(2)	$V_{DD}2$, $V_{DD}3$			V_{SS}		V_{DD}+0.1	
Input/output voltage		V_{IO}(1)	Ports 0, 1, 3, 7, 8 Ports A, B, C, D, E, F, XT2			−0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 32 to 35	• CMOS output selected • Current at each pin		−10			mA
		IOPH(2)	Ports 30, 31	• CMOS output selected • Current at each pin		−20			
		IOPH(3)	Ports 71 to 73	Current at each pin		−5			
		IOPH(4)	Ports A, B, C, D, E, F	Current at each pin		−5			
	Mean output current (Note 1-1)	IOMH(1)	Ports 0, 1, 32 to 35	• CMOS output selected • Current at each pin		−7.5			
		IOMH(2)	Ports 30, 31	• CMOS output selected • Current at each pin		−15			
		IOMH(3)	Ports 71 to 73	Current at each pin		−3			
		IOMH(4)	Ports A, B, C, D, E, F	Current at each pin		−3			
	Total output current	ΣIOAH(1)	Ports 0, 1, 32 to 35	Total of all pins		−25			
		ΣIOAH(2)	Ports 30, 31	Total of all pins		−25			
		ΣIOAH(3)	Ports 0, 1, 3	Total of all pins		−45			
		ΣIOAH(4)	Ports 71 to 73	Total of all pins		−5			
		ΣIOAH(5)	Ports A, B, C	Total of all pins		−25			
		ΣIOAH(6)	Ports D, E, F	Total of all pins		−25			
		ΣIOAH(7)	Ports A, B, C, D, E, F	Total of all pins		−45			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 32 to 35	Current at each pin				20	
		IOPL(2)	Ports 30, 31	Current at each pin				30	
		IOPL(3)	Ports 7, 8 XT2	Current at each pin				10	
		IOPL(4)	Ports A, B, C, D, E, F	Current at each pin				10	
	Mean output current (Note 1-1)	IOML(1)	Ports 0, 1, 32 to 35	Current at each pin				15	
		IOML(2)	Ports 30, 31	Current at each pin				20	
		IOML(3)	Ports 7, 8 XT2	Current at each pin				7.5	
		IOML(4)	Ports A, B, C, D, E, F	Current at each pin				7.5	
	Total output current	ΣOAL(1)	Ports 0,1,32 to 35	Total of all pins				45	
		ΣIOAL(2)	Ports 30, 31	Total of all pins				45	
		ΣIOAL(3)	Ports 0, 1, 3	Total of all pins				80	
		ΣIOAL(4)	Ports 7, 8 XT2	Total of all pins				20	
		ΣIOAL(5)	Ports A, B, C	Total of all pins				45	
		ΣIOAL(6)	Ports D, E, F	Total of all pins				45	
		ΣIOAL(7)	Ports A, B, C, D, E, F	Total of all pins				80	
Maximum power dissipation		Pd max	QIP100E(14×20)	Ta=-40 to +85°C				215	mW
			TQFP100(14×14)	Ta=-40 to +85°C				TBD	
Operating ambient temperature		Topr				−40		+85	°C
Storage ambient temperature		Tstg				−55		+125	

Note 1-1: The mean output current is a mean value measured over 100ms.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Range at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	$V_{DD}(1)$	$V_{DD}1=V_{DD}2=V_{DD}3$	0.167μs≤tCYC≤200μs		2.7		3.6	V
			0.356μs≤tCYC≤200μs		2.5		3.6	
Memory sustaining supply voltage	VHD	$V_{DD}1$	RAM and register contents sustained in HOLD mode.		2.0		3.6	
High level input voltage	$V_{IH}(1)$	Ports 0, 3, 8 Ports A, B, C, D, E, F Port L	Output disabled	2.5 to 3.6	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	Port 1 Ports 71 to 73 P70 port input/ interrupt side	• Output disabled • When INT1VTSL=0 (P71 only)	2.5 to 3.6	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(3)$	P71 interrupt side	• Output disabled • When INT1VTSL=1	2.5 to 3.6	$0.85V_{DD}$		V_{DD}	
	$V_{IH}(4)$	P87 small signal input side	Output disabled	2.5 to 3.6	$0.75V_{DD}$		V_{DD}	
	$V_{IH}(5)$	P70 watchdog timer side	Output disabled	2.5 to 3.6	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(6)$	XT1, XT2, CF1, $\overline{RES}$		2.5 to 3.6	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 0, 3, 8 Ports A, B, C, D, E, F Port L	Output disabled	2.5 to 3.6	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(2)$	Port 1 Ports 71 to 73 P70 port input/ interrupt side	• Output disabled • When INT1VTSL=0 (P71 only)	2.5 to 3.6	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	P71 interrupt side	• Output disabled • When INT1VTSL=1	2.5 to 3.6	V_{SS}		$0.45V_{DD}$	
	$V_{IL}(4)$	P87 small signal input side	Output disabled	2.5 to 3.6	V_{SS}		$0.25V_{DD}$	
	$V_{IL}(5)$	P70 watchdog timer side	Output disabled	2.5 to 3.6	V_{SS}		$0.8V_{DD}$ –1.0	
	$V_{IL}(6)$	XT1, XT2, CF1, $\overline{RES}$		2.5 to 3.6	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-2)	tCYC			2.7 to 3.6	0.167		200	μs
				2.5 to 3.6	0.356		200	
External system clock frequency	FEXCF(1)	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty=50±5%	2.5 to 3.6	0.1		18	MHz
			• CF2 pin open • System clock frequency division ratio=1/2	2.5 to 3.6	0.2		36	

Note 2-1: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

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Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
High level output voltage	V_{OH}(1)	Ports 0, 1, 32 to 35	I_{OH}=−0.4mA	2.5 to 3.6	V_{DD}−0.4			V
	V_{OH}(2)	Ports 30, 31	I_{OH}=−1.6mA	2.5 to 3.6	V_{DD}−0.4			
	V_{OH}(3)	Ports 71 to 73	I_{OH}=−0.4mA	2.5 to 3.6	V_{DD}−0.4			
	V_{OH}(4)	Ports A, B, C Ports D, E, F	I_{OH}=−0.4mA	2.5 to 3.6	V_{DD}−0.4			
Low level output voltage	V_{OL}(1)	Ports 0, 1, 32 to 35 Ports 30, 31 (PWM function output mode)	I_{OL}=1.6mA	2.5 to 3.6			0.4	
	V_{OL}(2)	Ports 30, 31 (Port function output mode)	I_{OL}=5mA	2.5 to 3.6			0.4	
	V_{OL}(3)	Ports 7, 8 XT2	I_{OL}=1.6mA	2.5 to 3.6			0.4	
	V_{OL}(4)	Ports A, B, C Ports D, E, F	I_{OL}=1.6mA	2.5 to 3.6			0.4	
LCD output voltage regulation	VODLS	S0 to S53	• I_O=0mA • VLCD, 2/3VLCD, 1/3VLCD level output • See Fig. 8.	2.5 to 3.6	0		±0.2	
	VODLC	COM0 to COM3	• IO=0mA • VLCD, 2/3VLCD, 1/2VLCD, 1/3VLCD level output • See Fig. 8.	2.5 to 3.6	0		±0.2	
LCD bias resistor	RLCD(1)	Resistance per one bias resister	See Fig. 8.	2.5 to 3.6		60		kΩ
	RLCD(2)	Resistance per one bias resister 1/2R mode	See Fig. 8.	2.5 to 3.6		30		
Resistance of pull-up MOS Tr.	Rpu(1)	Ports 0, 1, 3, 7 Ports A, B, C, D, E, F	V_{OH}=0.9V_{DD}	2.5 to 3.6	18	50	50	
Hysterisis voltage	VHYS(1)	Ports 1, 7 $\overline{RES}$		2.5 to 3.6		0.1V_{DD}		V
	VHYS(2)	P87 small signal input side		2.5 to 3.6		0.1V_{DD}		
Pin capacitance	CP	All pins	• For pins other than that under test: V_{IN}=V_{SS} • f=1MHz • Ta=25°C	2.5 to 3.6		10		pF
Input sensitivity	Vsen	P87 small signal input side		2.5 to 3.6	0.12V_{DD}			Vpp

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Serial I/O Characteristics at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3$ = 0V, 0.190µs ≤ tCYC ≤ 200µs

SIO0 Serial I/O Characteristics (Note 4-1-1) at V_{DD} = 2.7 V to 3.6V, 0.190µs ≤ tCYC ≤ 200µs

Parameter			Symbol	Pin/Remarks	Conditions	Specification				
						V_{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.	2.5 to 3.6	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)		• Continuous data transmission/reception mode • See Fig. 6. (Note 4-1-2)		4			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 6.	2.5 to 3.6	4/3			
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2)		• Continuous data transmission/reception mode • CMOS output selected • See Fig. 6.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.5 to 3.6	0.03			µs
	Data hold time		thDI(1)				0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode (Note 4-1-3)	2.5 to 3.6			(1/3)tCYC +0.05	
			tdD0(2)		• Synchronous 8-bit mode (Note 4-1-3)				1tCYC +0.05	
	Output clock		tdD0(3)		(Note 4-1-3)				(1/3)tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

AD Converter Characteristics at $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

<12bits AD Converter Mode at Ta =–30 to +70°C>

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN7(P87), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2)		2.5 to 3.6		12		bit
Absolute accuracy	ET		(Note 6-1)	2.5 to 3.6			±16	LSB
Conversion time	tCAD		• See Conversion time calculation formulas. (Note 6-2)	3.0 to 3.6	64		115	µs
				2.7 to 3.6	128		230	
				2.5 to 3.6	256		460	
Analog input voltage range	VAIN				V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	2.5 to 3.6			1	µA
	IAINL		VAIN=V_{SS}	2.5 to 3.6	–1			

<8bits AD Converter Mode at Ta =–30 to +70°C>

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN7(P87), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2)		2.5 to 3.6		8		bit
Absolute accuracy	ET		(Note 6-1)	2.5 to 3.6			±1.5	LSB
Conversion time	TCAD		• See Conversion time calculation formulas. (Note 6-2)	3.0 to 3.6	39		71	µs
				2.7 to 3.6	79		140	
				2.5 to 3.6	157		280	
Analog input voltage range	VAIN				V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	2.5 to 3.6			1	µA
	IAINL		VAIN=V_{SS}	2.5 to 3.6	–1			

<Conversion time calculation formulas>

12bits AD Converter Mode: tCAD(Conversion time)=((52/(division ratio)) + 2) × (1/3) ×tCYC
8bits AD Converter Mode: tCAD(Conversion time)=((32/(division ratio)) + 2) × (1/3) ×tCYC

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.
The conversion time is 2 times the normal-time conversion time when:
- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

Consumption Current Characteristics at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	$V_{DD}1 = V_{DD}2 = V_{DD}3$	• FmCF=18MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 3.6		6.1	15.6	mA
	IDDOP(2)		• FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.5 to 3.6		3.9	8.8	
	IDDOP(3)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	2.5 to 3.6		0.4	1.7	
	IDDOP(4)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 10MHz with frequency variable RC oscillation • 1/1 frequency division ratio	2.5 to 3.6		4.3	12.0	
	IDDOP(5)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 4MHz with frequency variable RC oscillation • 1/1 frequency division ratio	2.5 to 3.6		2.1	6.6	
	IDDOP(6)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	2.5 to 3.6		19.3	73	μA

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued on next page.

F-ROM Write Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

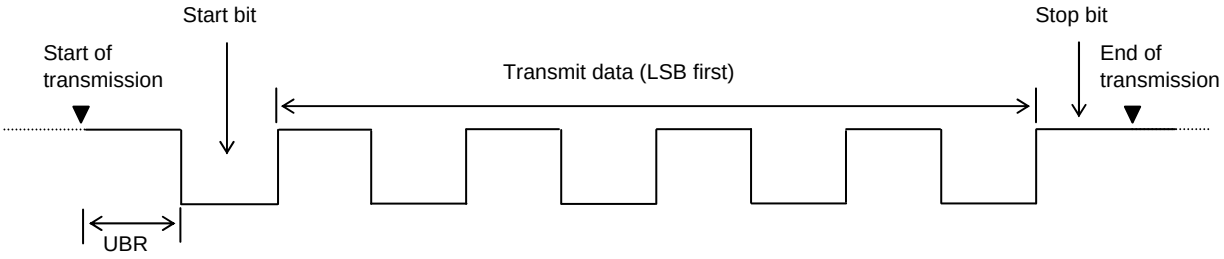
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Without CPU current	3.0 to 3.6		7	11	mA
Programming time	tFW(1)		• 2K-byte erase operation	3.0 to 3.6		12	15	ms
	tFW(2)		• 2K-byte writing operation	3.0 to 3.6		35	45	µs

UART (Full Duplex) Operating Conditions at Ta = +40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

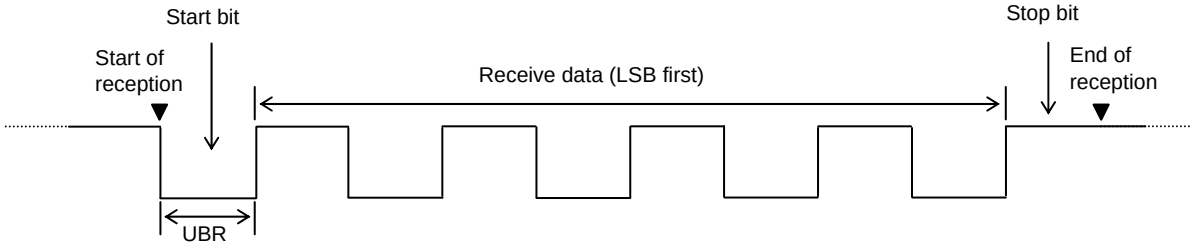
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
Transfer rate	UBR	UTX(S32), URX(S33)		2.5 to 3.6	16/3		8192/3	tCYC

Data length: 7/8/9 bits (LSB first)
Stop bits: 1 bit (2-bit in continuous data transmission)
Parity bits: None

Example of 8-bit Data Transmission Mode Processing (Transmit Data=55H)



Example of 8-bit Data Reception Mode Processing (Receive Data=55H)



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
18MHz	MURATA	CSTCE18M0V51-R0	(5)	(5)	OPEN	150	2.7 to 3.6	0.05	0.15	Values shown in parentheses are capacitance included in the oscillator
		CSTLS18M0X51-B0	(5)	(5)	OPEN	0	2.7 to 3.6	0.11	0.33	
10MHz	MURATA	CSTCE10M00G52-R0	(10)	(10)	OPEN	680	2.5 to 3.6	0.05	0.15	Values shown in parentheses are capacitance included in the oscillator
		CSTLS10M00G53-B0	(15)	(15)	OPEN	1.5k	2.5 to 3.6	0.05	0.15	
8MHz	MURATA	CSTCE8M00G52-R0	(10)	(10)	OPEN	680	2.5 to 3.6	0.05	0.15	Values shown in parentheses are capacitance included in the oscillator
		CSTLS8M00G53-B0	(15)	(15)	OPEN	1.5k	2.5 to 3.6	0.05	0.15	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillation Circuit with a Crystal Oscillation

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	9	9	Open	330k	2.5 to 3.6	1.0	3.0	CL=7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Fig. 4).

Caution: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

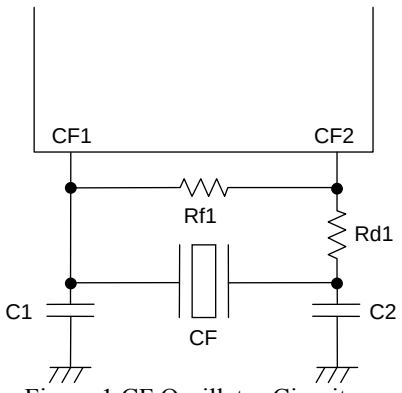


Figure 1 CF Oscillator Circuit

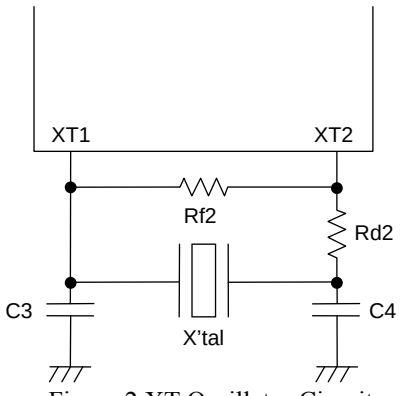


Figure 2 XT Oscillator Circuit

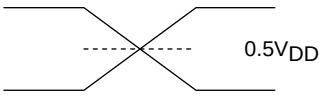
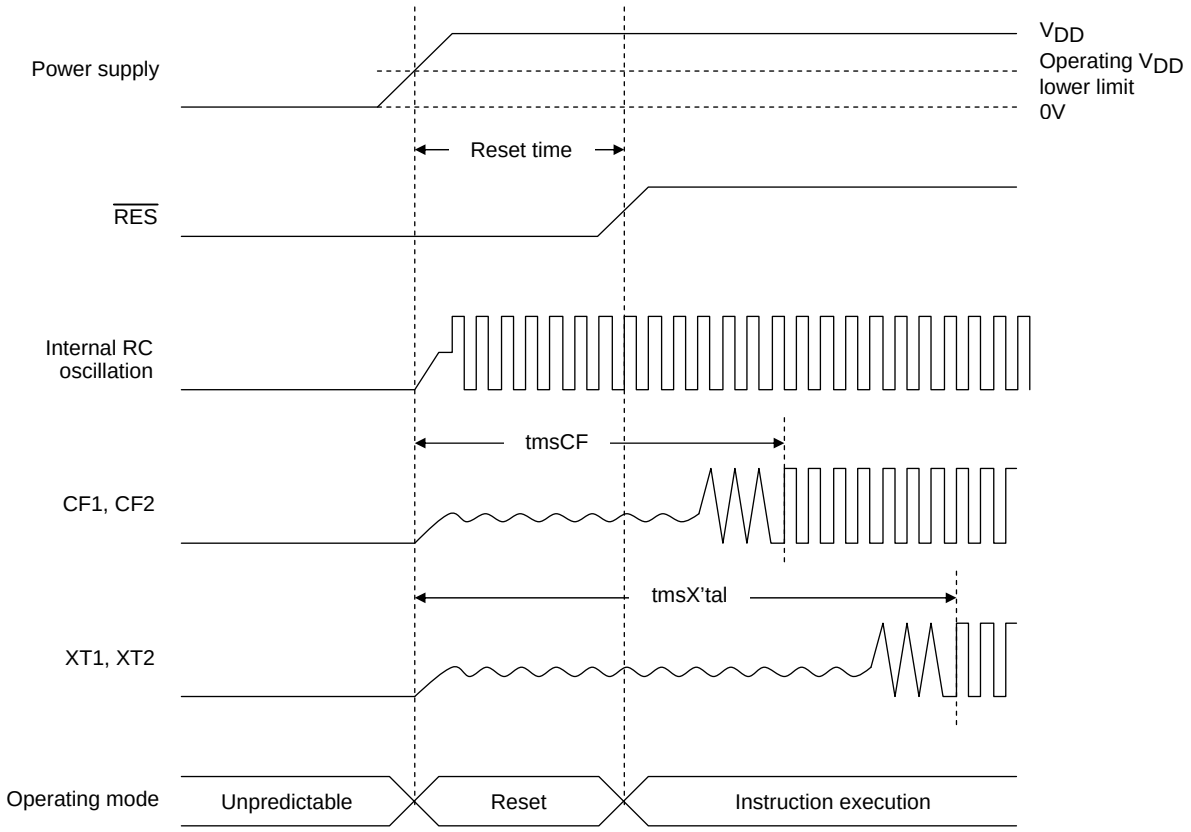
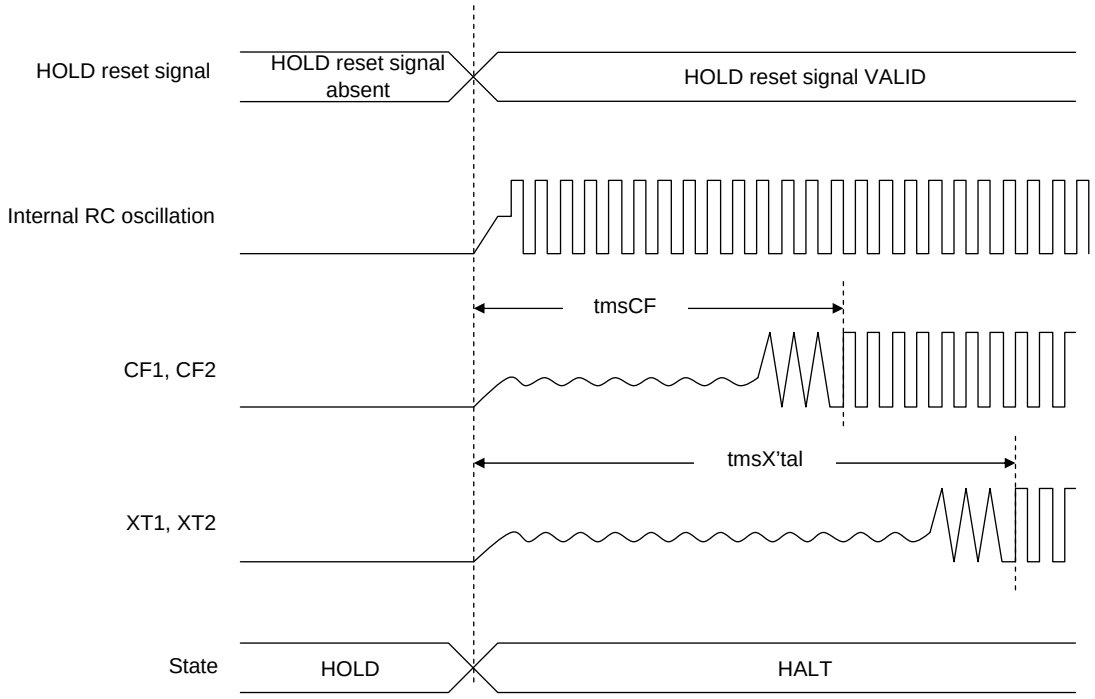


Figure 3 AC Timing Measurement Point



Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times

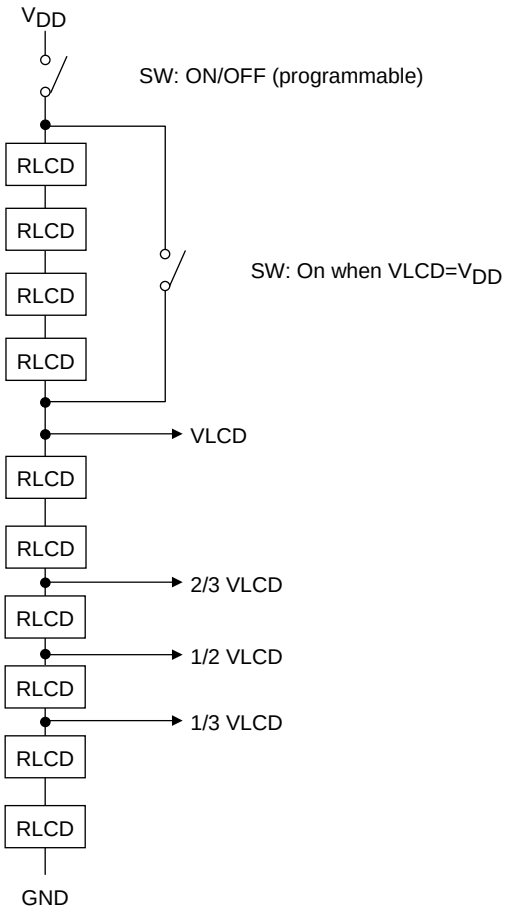


Figure 8 LCD bias resistor

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC87F7NC8AUEJ-2H	QIP100E(14×20) (Pb-Free / Halogen Free)	50 / Tray Foam
LC87F7NC8AVUEJ-2H	QIP100E(14×20) (Pb-Free / Halogen Free)	50 / Tray Foam