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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21e16l-mnt

32-bit ARM-Based Microcontrollers

- Up to four compare channels with optional complementary output
 - Generation of synchronized pulse width modulation (PWM) pattern across port pins
 - Deterministic fault protection, fast decay and configurable dead-time between complementary output
 - Dithering that increase resolution with up to 5 bit and reduce quantization error
- 32-bit Real Time Counter (RTC) with clock/calendar function
- Watchdog Timer (WDT)
- CRC-32 generator
- Up to six Serial Communication Interfaces (SERCOM), each configurable to operate as either:
 - USART with full-duplex and single-wire half-duplex configuration
 - I²C up to 3.4MHz
 - SPI
 - LIN slave
- One 12-bit, 350ksps Analog-to-Digital Converter (ADC) with up to 18 channels
 - Differential and single-ended input
 - 1/2x to 16x programmable gain stage
 - Automatic offset and gain error compensation
 - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
- 10-bit, 350ksps Digital-to-Analog Converter (DAC)
- Four Analog Comparators (AC) with window compare function
- I/O
 - Up to 38 programmable I/O pins
- Packages
 - 48-pin TQFP, QFN
 - 32-pin QFN
- Operating Voltage
 - 1.62V – 3.63V

Table of Contents

Introduction.....	1
Features.....	1
1. Description.....	5
2. Configuration Summary.....	6
3. Ordering Information.....	7
3.1. SAM D21ExL.....	7
3.2. SAM D21GxL.....	7
3.3. Device Identification.....	7
4. Block Diagram.....	9
5. Pinout.....	10
5.1. SAM D21GxL.....	10
5.2. SAM D21ExL.....	11
6. Product Mapping.....	12
7. Processor And Architecture.....	13
7.1. Cortex M0+ Processor.....	13
7.2. Nested Vector Interrupt Controller.....	14
7.3. Micro Trace Buffer.....	16
7.4. High-Speed Bus System.....	17
7.5. AHB-APB Bridge.....	18
7.6. PAC - Peripheral Access Controller.....	19
8. Packaging Information.....	29
8.1. Thermal Considerations.....	29
8.2. Package Drawings.....	30
8.3. Soldering Profile.....	34
The Microchip Web Site.....	35
Customer Change Notification Service.....	35
Customer Support.....	35
Product Identification System.....	35
Microchip Devices Code Protection Feature.....	36
Legal Notice.....	36
Trademarks.....	37

32-bit ARM-Based Microcontrollers

Quality Management System Certified by DNV.....	37
Worldwide Sales and Service.....	38

1. Description

The SAM D21L is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and offered in 32- and 48-pin packages with up to 64KB Flash and 8KB of SRAM. The SAM D21L operate at a maximum frequency of 48MHz and reach 2.46 CoreMark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The SAM D21L microcontrollers provide the following features: In-system programmable Flash, twelve-channel direct memory access (DMA) controller, 12 channel Event System, programmable interrupt controller, up to 52 programmable I/O pins, 32-bit real-time clock and calendar, up to five 16-bit Timer/Counters (TC) and three 24-bit Timer/Counters for Control (TCC), where each TC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and three timer/counters have extended functions optimized for motor, lighting and other control applications. The series provide up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I²C up to 3.4MHz, SMBus, PMBus, and LIN slave; up to eighteen-channel 350ksps 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, one 10-bit 350ksps DAC, four analog comparators with window mode; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

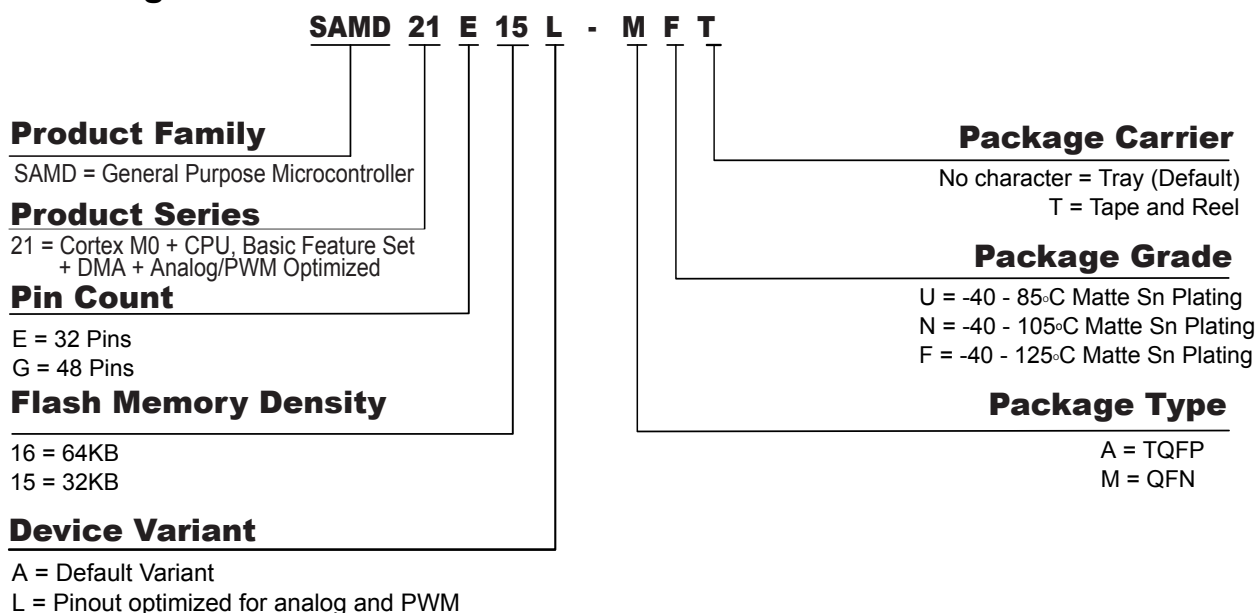
All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM D21L microcontrollers have two software-selectable sleep modes, idle and standby. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped except those selected to continue running. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The SAM D21L microcontrollers are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

3. Ordering Information



3.1 SAM D21ExL

Ordering Code	FLASH (bytes)	SRAM (bytes)	Temperature Range	Package	Carrier Type
ATSAMD21E15L-MNT	32K	4K	105°C	QFN32	Tape & Reel
ATSAMD21E15L-MFT	32K	4K	125°C	QFN32	Tape & Reel
ATSAMD21E15L-AFT	32K	4K	125°C	TQFP32	Tape & Reel
ATSAMD21E16L-MNT	64K	8K	105°C	QFN32	Tape & Reel
ATSAMD21E16L-MFT	64K	8K	125°C	QFN32	Tape & Reel
ATSAMD21E16L-AFT	64K	8K	125°C	TQFP32	Tape & Reel

3.2 SAM D21GxL

Ordering Code	FLASH (bytes)	SRAM (bytes)	Temperature Range	Package	Carrier Type
ATSAMD21G16L-MUT	64K	8K	85°C	QFN48	Tape & Reel
ATSAMD21G16L-MNT	64K	8K	105°C	QFN48	Tape & Reel

3.3 Device Identification

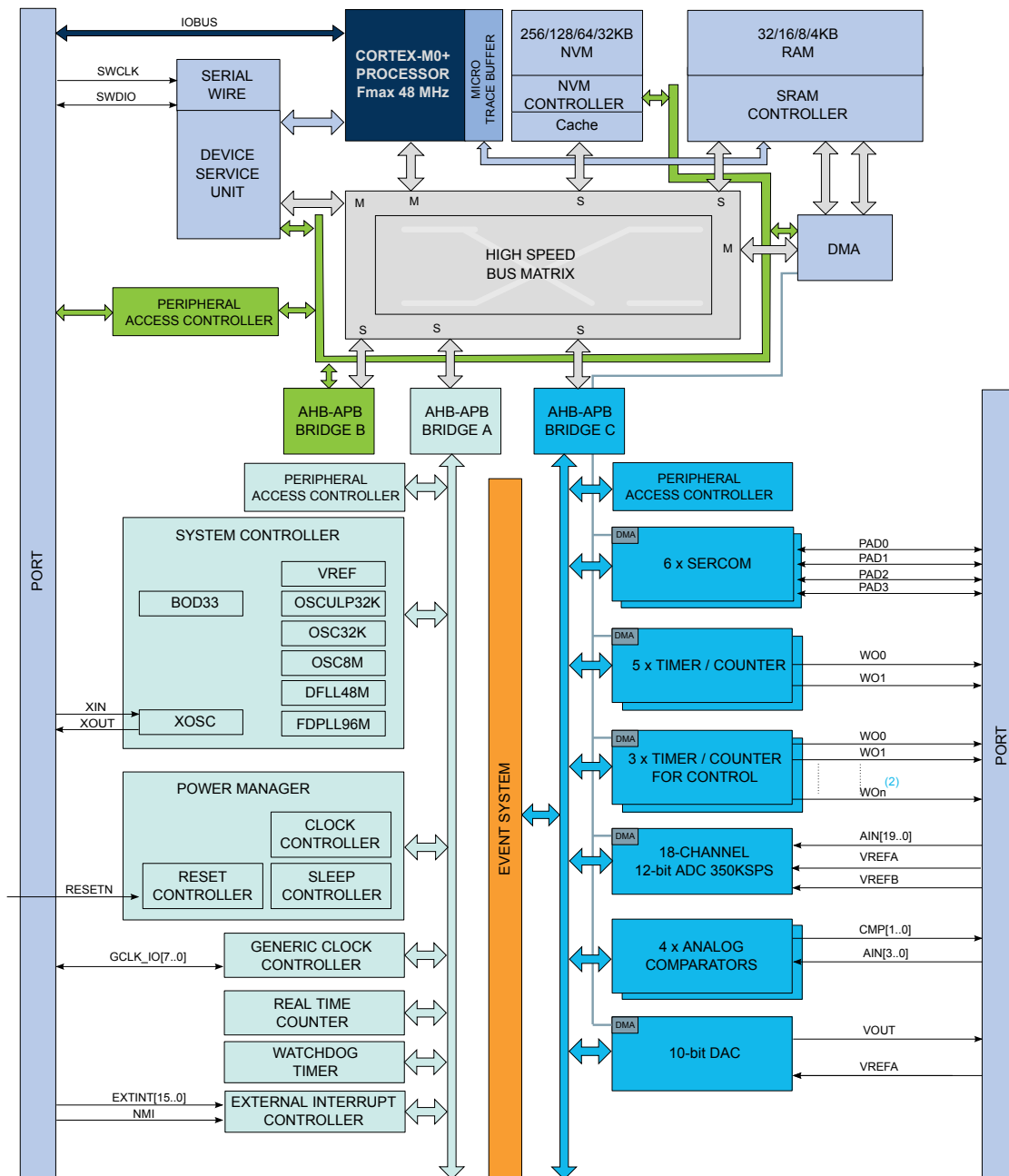
The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM D21L variants have a reset value of DID=0x1001drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

Table 3-1. SAM D21L Device Identification Values

Device Variant	DID.DEVSEL	Device ID (DID)
Reserved	0x00 - 0x61	
SAMD21E16L	0x62	0x1001143E
SAMD21E15L	0x63	0x1001143F
Reserved	0x64 - 0x86	
SAMD21G16L	0x87	0x10011457
Reserved	0x88 - 0xFF	

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die. The device variant denotes functional differences, whereas the die revision marks evolution of the die.

4. Block Diagram



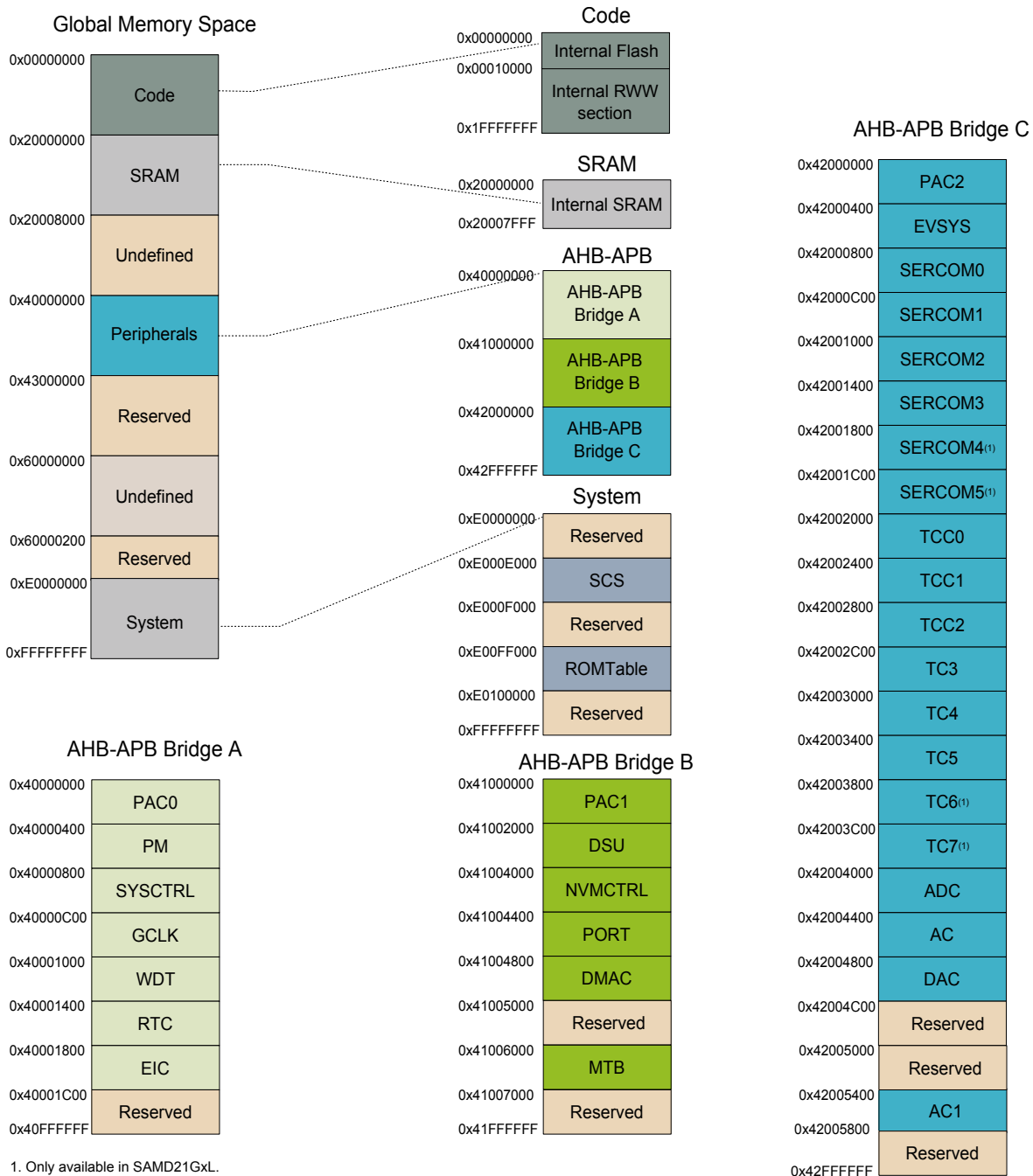
1. Some products have different number of SERCOM instances, Timer/Counter instances and ADC signals. Refer to the Configuration Summary.
2. The three TCC instances have different configurations, including the number of Waveform Output (WO) lines. Refer to the TCC Configurations for details.

Related Links

Configuration Summary

6. Product Mapping

Figure 6-1. SAM D21L Product Mapping



This figure represents the full configuration of the SAM D21L with maximum flash and SRAM capabilities and a full set of peripherals. Refer to the configuration summary for details.

7. Processor And Architecture

7.1 Cortex M0+ Processor

The SAM D21L implements the ARM® Cortex®-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The ARM Cortex-M0+ implemented is revision r0p1. For more information refer to <http://www.arm.com>.

7.1.1 Cortex M0+ Configuration

Table 7-1. Cortex M0+ Configuration

Features	Configurable option	Device configuration
Interrupts	External interrupts 0-32	28
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Absent ⁽¹⁾
Memory Protection Unit	Not present or 8-region	Not present
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

Note:

1. All software run in privileged mode only.

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory, which includes flash and RAM.
- Single 32-bit I/O port bus interfacing to the PORT with 1-cycle loads and stores.

7.1.2 Cortex-M0+ Peripherals

- System Control Space (SCS)
 - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- System Timer (SysTick)

7.4 High-Speed Bus System

7.4.1 Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

7.4.2 Configuration

Table 7-4. Bus Matrix Masters

Bus Matrix Masters	Master ID
CM0+ - Cortex M0+ Processor	0
DSU - Device Service Unit	1

Table 7-5. Bus Matrix Slaves

Bus Matrix Slaves	Slave ID
Internal Flash Memory	0
AHB-APB Bridge A	1
AHB-APB Bridge B	2
AHB-APB Bridge C	3

7.4.3 SRAM Quality of Service

To ensure that masters with latency requirements get sufficient priority when accessing RAM, the different masters can be configured to have a given priority for different type of access.

The Quality of Service (QoS) level is independently selected for each master accessing the RAM. For any access to the RAM the RAM also receives the QoS level. The QoS levels and their corresponding bit values for the QoS level configuration is shown in Table. Quality of Service.

Table 7-6. Quality of Service

Value	Name	Description
00	DISABLE	Background (no sensitive operation)
01	LOW	Sensitive Bandwidth
10	MEDIUM	Sensitive Latency
11	HIGH	Critical Latency

If a master is configured with QoS level 0x00 or 0x01 there will be minimum one cycle latency for the RAM access.

The priority order for concurrent accesses are decided by two factors. First the QoS level for the master and then a static priority given by table nn-mm (table: SRAM port connection) where the lowest port ID has the highest static priority.

The MTB has fixed QoS level 3 and the DSU has fixed QoS level 1.

The CPU QoS level can be written/read at address 0x41007110, bits [1:0]. Its reset value is 0x0.

Refer to different master QOSCTRL registers for configuring QoS for the other master (DMAC).

7.5 AHB-APB Bridge

The AHB-APB bridge is an AHB slave, providing an interface between the high-speed AHB domain and the low-power APB domain. It is used to provide access to the programmable control registers of peripherals.

AHB-APB bridge is based on AMBA APB Protocol Specification V2.0 (ref. as APB4) including:

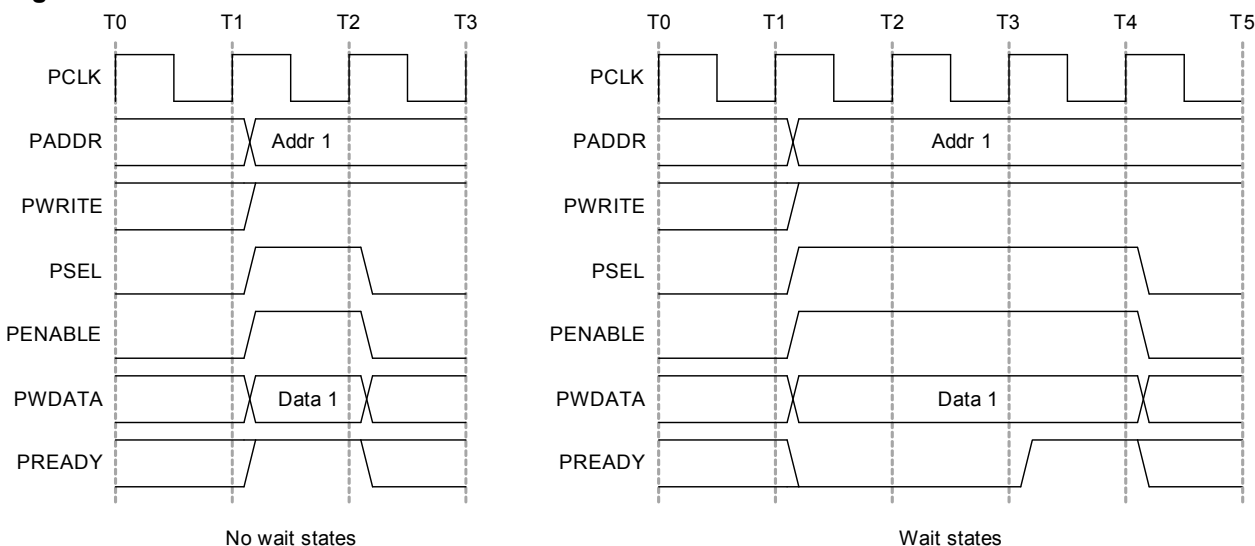
- Wait state support
- Error reporting
- Transaction protection
- Sparse data transfer (byte, half-word and word)

Additional enhancements:

- Address and data cycles merged into a single cycle
- Sparse data transfer also apply to read access

to operate the AHB-APB bridge, the clock (CLK_HPxBx_AHB) must be enabled. See *PM – Power Manager* for details.

Figure 7-1. APB Write Access.



32-bit ARM-Based Microcontrollers

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access		EIC	RTC	WDT	GCLK	SYSCTRL	PM	
Reset		0	0	0	0	0	0	

Bit 6 – EIC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 5 – RTC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 4 – WDT:

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – GCLK

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – SYSCTRL

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

32-bit ARM-Based Microcontrollers

Bit	15	14	13	12	11	10	9	8
	TC7	TC4	TC5	TC4	TC3	TCC2	TCC1	TCC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
							EVSYS	
Access							R/W	
Reset							0	

Bit 18 – DAC:

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 17 – AC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 16 – ADC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 11, 12, 13, 14, 15 – TC3, TC4, TC5, TC4, TC7

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 8, 9, 10 – TCCn

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

32-bit ARM-Based Microcontrollers

Bit 1 – EVSYS

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 0:1, 2:3, 4:5, 6:7, 8:9, 10:11 – SERCOMn

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Write Protect Set

Name: WPSET

Offset: 0x04

Reset: 0x00800000

Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
						DAC	AC	ADC
Access						R/W	R/W	R/W
Reset						0	0	0
Bit	15	14	13	12	11	10	9	8
	TC7	TC6	TC5	TC4	TC3	TCC2	TCC1	TCC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	SERCOM5	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0	EVSYS	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit 18 – DAC:

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 17 – AC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 16 – ADC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 11, 12, 13, 14, 15 – TC3, TC4, TC5, TC6, TC7

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 8, 9, 10 – TCCn

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 2, 3, 4, 5, 6, 7 – SERCOMn

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – EVSYS

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

32-bit ARM-Based Microcontrollers

Table 8-5. Device and Package Maximum Weight

100	mg
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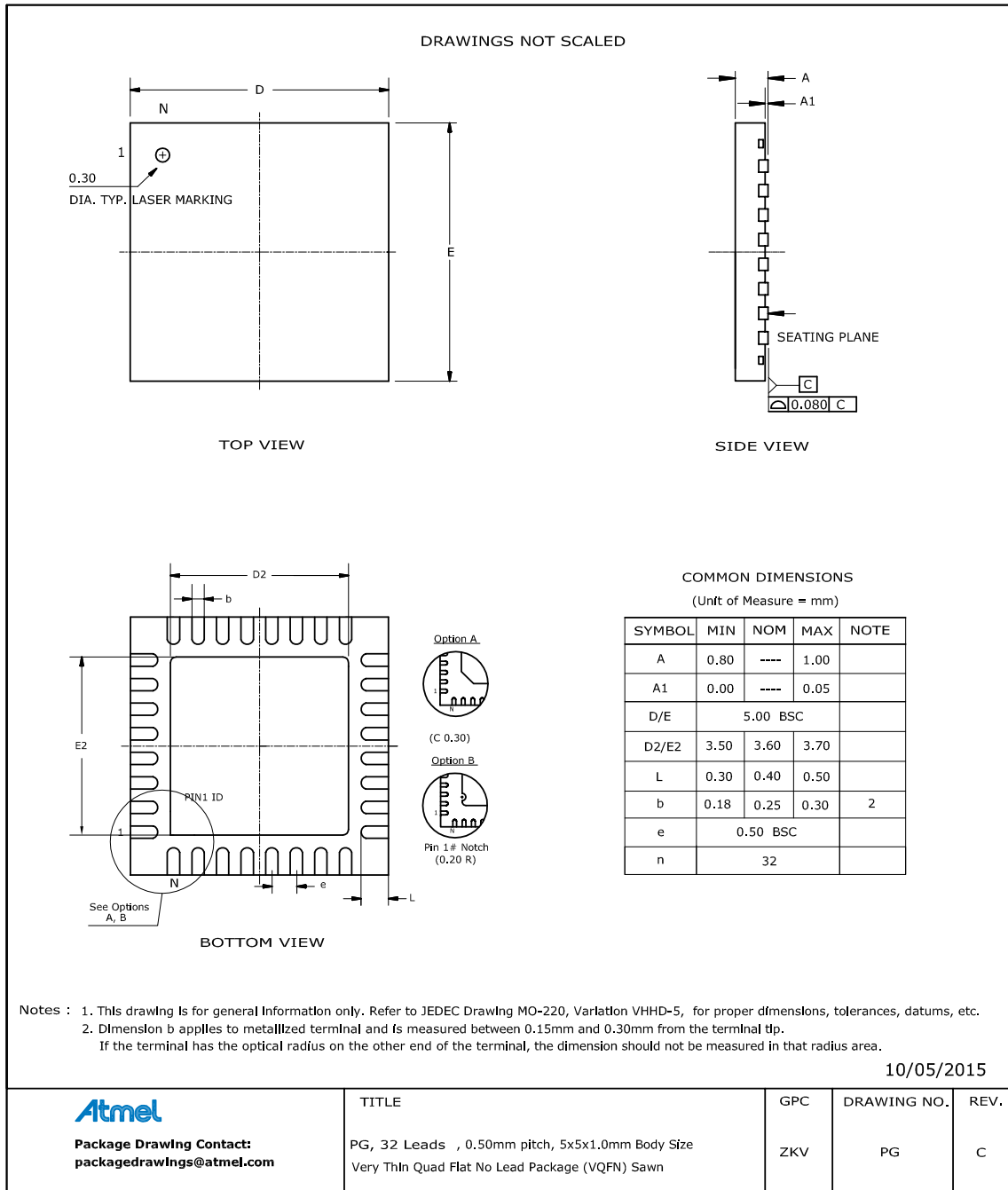
Table 8-6. Package Characteristics

Moisture Sensitivity Level	MSL3
----------------------------	------

Table 8-7. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.3 32 pin QFN



Note: The exposed die attach pad is connected inside the device to GND and GNDANA.

Table 8-8. Device and Package Maximum Weight

90	mg
----	----

Table 8-9. Package Characteristics

Moisture Sensitivity Level	MSL3
----------------------------	------

Table 8-10. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.3 Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Table 8-11.

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max.
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max.
Time 25°C to Peak Temperature	8 minutes max.

A maximum of three reflow passes is allowed per component.

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