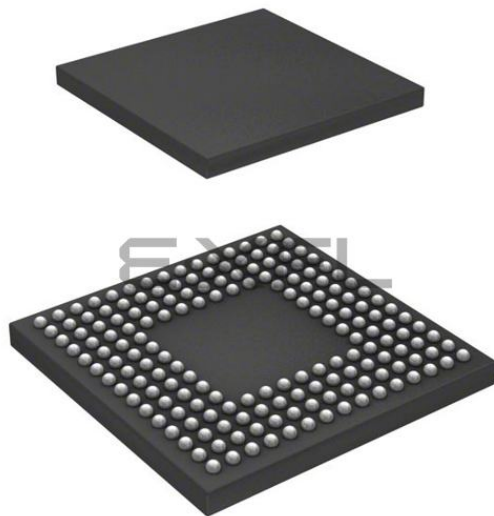




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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56316ddbg-u0

Table 1.1 Outline of Specifications (4/6)

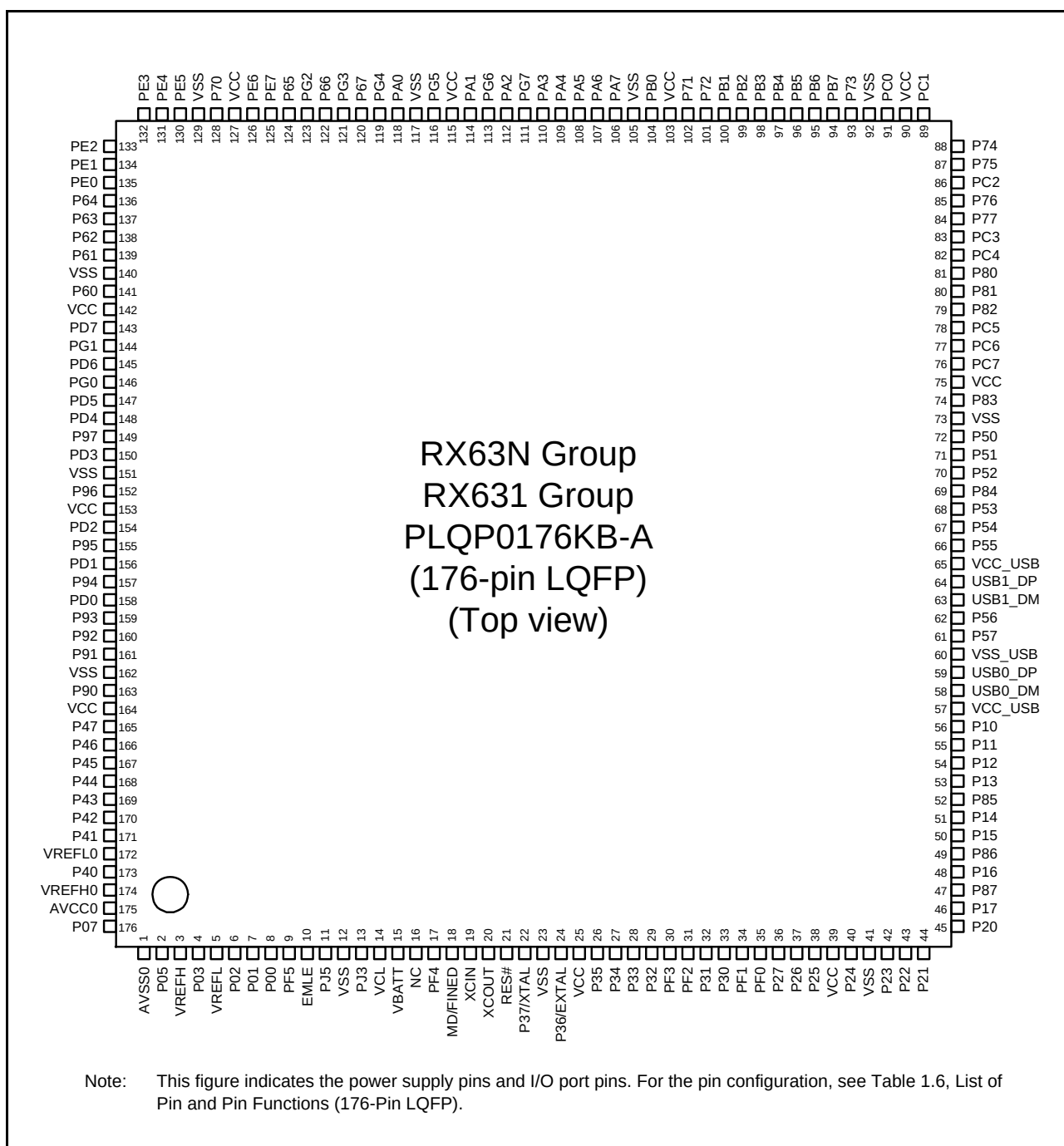
Classification	Module/Function	Description
Timers	16-bit timer pulse unit (TPUa)	• (16 bits x 6 channels) x 2 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Buffered operation and phase-counting mode (two phase encoder input) depending on the channel • Support for cascade-connected operation (32 bits x 2 channels) • PPG output trigger can be generated • Capable of generating conversion start triggers for the A/D converters • Signals from the input capture pins are input via a digital filter • Clock frequency measuring method
	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits x 6 channels) x 1 unit • Time bases for the 6 x 16-bit timer channels can be provided via up to sixteen pulse-input/output lines and three pulse-input lines • Select from among eight counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Generation of triggers for A/D converter conversion • Digital filter • Signals from the input capture pins are input via a digital filter • PPG output trigger can be generated • Clock frequency measuring function
	Frequency measuring method (MCK)	The MTU or unit 0 TPU module can be used to monitor the main clock, subclock, HOCO clock, LOCO clock, and PLL clock for abnormal frequencies.
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Programmable pulse generator (PPG)	• (4 bits x 4 groups) x 2 units • Pulse output with the MTU2 or TPU output as a trigger • Maximum of 32 pulse-output possible
	8-bit timers (TMR)	• (8 bits x 2 channels) x 2 units • Select from among seven internal clock signals (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12
	Compare match timer (CMT)	• (16 bits x 2 channels) x 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Realtime clock (RTCa)	• Clock sources: Main clock, subclock • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values
	Watchdog timer (WDTa)	• 14 bits x 1 channel • Select from among 6 counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Independent watchdog timer (IWDTa)	• 14 bits x 1 channel • Counter-input clock: IWDt-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX63N (D version)	R5F563NECDLC	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDLC	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDLC	PTLG0177KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDL	PTLG0177KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDLC	PTLG0177KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDL	PTLG0177KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDLC	PTLG0177KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDLC	PTLG0177KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDBG	PLBG0176GA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDBG	PLBG0176GA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDBG	PLBG0176GA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDBG	PLBG0176GA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDBG	PLBG0176GA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDBG	PLBG0176GA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDBG	PLBG0176GA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDBG	PLBG0176GA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFHDFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFDDFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKHDFC	PLQP0176KB-A*1	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKDDFC	PLQP0176KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDFC	PLQP0176KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDFC	PLQP0176KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJHDFC	PLQP0176KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJDDFC	PLQP0176KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGHDFC	PLQP0176KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGDDFC	PLQP0176KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDFC	PLQP0176KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDFC	PLQP0176KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYHDFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYDDFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWHDFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWDDFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWGDFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWCDFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDFC	PLQP0176KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDFC	PLQP0176KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDFC	PLQP0176KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDFC	PLQP0176KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDLK	PTLG0145KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDLK	PTLG0145KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

**Figure 1.5 Pin Assignment (176-Pin LQFP)**

RX63N Group, RX631 Group
PTLG0100JA-A (100-pin TFLGA)
(Top view)

	A	B	C	D	E	F	G	H	J	K	
10	PE2	PE3	PE4	PA0	PA3	VSS	VCC	PB7	PC1	PC2	10
9	PE1	PD7	PE5	PA1	PA5	PA7	PB1	PB6	PC0	PC3	9
8	PE0	PD6	PD5	PE7	PA4	PB0	PB4	PC6	PC4	PC5	8
7	PD4	PD3	PD2	PE6	PA6	PB2	PB5	PC7	P50	P51	7
6	PD0	PD1	P47	P46	PA2	PB3	P52	P54	VCC_ USB	USB0_ DP	6
5	P43	P44	P42	P45	P41	P12	P53	P55	VSS_ USB	USB0_ DM	5
4	VREFL0	P40	VREFH0	VBATT	P34	P32	P27	P15	P13	P14	4
3	P07	AVCC0	PJ3	MD/ FINED	RES#	P35	P30	P16	P17	P20	3
2	VREFH	AVSS0	VREFL	XCOUT	VSS	VCC	P31	P25	P21	P22	2
1	P05	EMLE	VCL	XCIN	XTAL	EXTAL	P33	P26	P24	P23	1
	A	B	C	D	E	F	G	H	J	K	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pins and Pin Functions (100-Pin LQFP).

Figure 1.8 Pin Assignment (100-Pin TFLGA)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
H3	RES#						
H4		P35				NMI	
H12		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	ET_MDC/TXD5/SMOSI5/ SSDA5/SSLA0	IRQ5-DS	
H13		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	ET_MDIO/RXD5/SMISO5/ SSCL5	IRQ6-DS	
H14		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
H15	TRDATA3	PG7	D31				
J1	EXTAL	P36					
J2	VCC						
J3		P34		MTIOC0A/TMCI3/PO12/ POE2#	SCK6/SCK0/ USB_DPRPD	IRQ4	
J4	TMS	PF3					
J12		PA5	A5	TIOC0B1/PO21	ET_LINKSTA/RSPCKA		
J13	VSS						
J14		PA7	A7	TIOC0B2/PO23	ET_WOL/MISOA		
J15		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	ET_EXOUT/CTS5#/ RTS5#SS5#MOSIA		
K1		P33		MTIOC0D/TIOC0D/ TMRI3/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0/PCKO	IRQ3-DS	
K2		P32		MTIOC0C/TIOC0C/TMO3/ PO10/RTCOU/RTIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC	IRQ2-DS	
K3	TDI	PF2			RXD1/SMISO1/SSCL1		
K4	TCK/FINEC	PF1			SCK1		
K12		PB2	A10	TIOC0C3/TCLKC/PO26	ET_RX_CLK/REF50CK/ CTS4#RTS4#CTS6#/ RTS6#SS4#SS6#		
K13		P71	CS1#		ET_MDIO		
K14	VCC						
K15		PB0	A8	MTIC5W/TIOCA3/PO24	ET_ERXD1/RMII_RXD1/ RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA	IRQ12	
L1		P31		MTIOC4D/TMCI2/PO9/ RTIC1	CTS1#RTS1#SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
L2		P30		MTIOC4B/TMRI3/PO8/ RTIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
L3	TDO	PF0			TXD1/SMOSI1/SSDA1		
L4		P25	CS5#/EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3/ USB_DPRPD/HSYNC		ADTRG0#
L12		PB6	A14	MTIOC3D/TIOCA5/PO30	ET_ETXD1/RMII_TXD1/ RXD9/SMISO9/SSCL9		
L13		PB3	A11	MTIOC0A/MTIOC4A/ TIOC0D/TCLKD/TMO0/ PO27/POE3#	ET_RX_ER/RMII_RX_ER/ SCK4/SCK6		
L14		PB1	A9	MTIOC0C/MTIOC4C/ TIOC0B3/TMCI0/PO25	ET_ERXD0/RMII_RXD0/ TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6	IRQ4-DS	
L15		P72	CS2#		ET_MDC		
M1		P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
M2		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
M3		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/USB0_VBUSEN/ PIXCLK		
M4		P86		TIOCA0	PIXD1		
M5		P13		MTIOC0B/TIOCA5/TMO3/ PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
M6		P56	WR2#/BC2#/ EDACK1	MTIOC3C/TIOCA1			
M7		P54	ALE/EDACK0	MTIOC4B/TMCI1	ET_LINKSTA/CTS2#/ RTS2#/SS2#/CTX1		
M8		P53*2	BCLK				
M9		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
M10		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	ET_ETXD2/SCK8/ RSPCKA		
M11		P81	EDACK0	MTIOC3D/PO27	ET_ETXD0/RMII_TXD0/ RXD10/SMISO10/SSCL10		
M12		P77	CS7#	PO23	ET_RX_ER/RMII_RX_ER/ TXD11/SMOSI11/SSDA11		
M13		PB7	A15	MTIOC3B/TIOCB5/PO31	ET_CRS/RMII_CRS_DV/ TXD9/SMOSI9/SSDA9		
M14		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	ET_ETXD0/RMII_TXD0/ SCK9		
M15		PB4	A12	TIOCA4/PO28	ET_TX_EN/ RMII_TXD_EN/CTS9#/ RTS9#/SS9#		
N1	VCC						
N2		P23	EDACK0	MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7		
N3		P22	EDREQ0	MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0/USB0_DRPD/ PIXD6		
N4		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ USB1_DPUPE/PIXD0	IRQ5	
N5		P12		MTIC5U/TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
N6		P57	WAIT#/WR3#/ BC3#/EDREQ1				
N7		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	ET_EXOUT/CRX1	IRQ10	
N8	VCC_USB						
N9		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
N10		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	ET_COL/TXD8/SMOSI8/ SSDA8/MISOA	IRQ14	
N11		P82	EDREQ1	MTIOC4A/PO28	ET_ETXD1/RMII_TXD1/ TXD10/SMOSI10/SSDA10		
N12		PC3	A19	MTIOC4D/TCLKB/PO24	ET_TX_ER/TXD5/ SMOSI5/SSDA5/IETXD		
N13		PC0	A16	MTIOC3C/TCLKC/PO17	ET_ERXD3/CTS5#/ RTS5#/SS5#/SSLA1/ SCL3	IRQ14	
N14		P73	CS3#	PO16	ET_WOL		
N15	VSS						

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (1/5)

Pin No.	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
A1	AVSS0						
A2		P07				IRQ15	ADTRG0#
A3		P40				IRQ8-DS	AN000
A4		P42				IRQ10-DS	AN002
A5		P45				IRQ13-DS	AN005
A6		P90	A16		TXD7/SMOSI7/SSDA7		AN014
A7		P92	A18		RXD7/SMISO7/SSCL7		AN016
A8		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
A9		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
A10	VSS						
A11		P62	CS2#/RAS#				
A12		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/ PO18	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB		ANEX1
A13		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/ PO26/POE8#	CTS12#/RTS12#/SS12#/ MISOB/ET_ERXD3		AN1
B1	VREFH						
B2	AVCC0						
B3		P05				IRQ13	DA1
B4	VREFL0						
B5		P43				IRQ11-DS	AN003
B6		P47				IRQ15-DS	AN007
B7		P91	A17		SCK7		AN015
B8		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
B9		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
B10	VCC						
B11		P61	CS1#/SDCS#				
B12		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/ PO23	RXD12/SMISO12/SSCL12/ RXDX12/SSLB3/MOSIB	IRQ7-DS	AN0
B13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0/ET_ERXD2		AN2
C1	VREFL						
C2		P02		TMC11	SCK6	IRQ10	AN020
C3	VREFH0						
C4		P41				IRQ9-DS	AN001
C5		P46				IRQ14-DS	AN006
C6	VSS						
C7		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
C8		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
C9		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
C10		P63	CS3#/CAS#				
C11		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
C12	SDCLK	P70					
C13	VSS						
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
D2		PF5				IRQ4	
D3		P03				IRQ11	DA0
D4		P01		TMC10	RXD6/SMISO6/SSCL6	IRQ9	AN019

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (4/4)

Pin No. 100-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
94	VREFL0						
95		P40				IRQ8-DS	AN000
96	VREFH0						
97	AVCC0						
98		P07				IRQ15	ADTRG0#
99	AVSS0						
100		P05				IRQ13	DA1

Note 1. Enabled only for the ROM capacity of 768 Kbytes or more

Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.11 List of Pins and Pin Functions (64-Pin TFLGA) (1/2)

Pin No. 64-pin TFLGA	Power Supply Clock System Control	I/O Port	Timers (MTU2a, TPUa, TMR, PPG, RTCa, POE2a)	Communications (SClC, SClD, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
A1		P05			IRQ13	DA1
A2	AVCC0					
A3	VREFH0					
A4	VREFL0					
A5	VREFH					
A6	VREFL					
A7		PE2	MTIOC4A/PO23	RXD12/SMISO12/SSCL12/ RXDX12/SSLB3/MOSIB	IRQ7-DS	AN010
A8		PE3	MTIOC4B/PO26/POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN011
B1	VCL					
B2	AVSS0					
B3		P40			IRQ8-DS	AN000
B4		P42			IRQ10-DS	AN002
B5		P44			IRQ12-DS	AN004
B6		P46			IRQ14-DS	AN006
B7		PE1	MTIOC4C/PO18	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB		AN009
B8		PE4	MTIOC4D/MTIOC1A/PO28	SSLB0		AN012
C1	XCIN					
C2	MD/FINED					
C3	EMLE					
C4		P41			IRQ9-DS	AN001
C5		P43			IRQ11-DS	AN003
C6		PE0		SCK12/SSLB1		AN008
C7		PE5	MTIOC4C/MTIOC2B	RSPCKB	IRQ5	AN013
C8		PA0	MTIOC4A/TIOCA0/PO16	SSLA1		
D1	XCOUT					
D2	RES#					
D3	TCK FINEC	P27	MTIOC2B/TMCI3	SCK1/RSPCKB		
D4		P14	MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2	CTS1#/RTS1#/SS1#/CTX1/ USB0_DPUPE/ USB0_OVRCURA	IRQ4	
D5		PA6	MTIC5V/MTCLKB/TIOCA2/ TMCI3/PO22/POE2#	CTS5#/RTS5#/SS5#/ MOSIA		
D6		PA4	MTIC5U/MTCLKA/TIOCA1/ TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS	
D7		PA1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2/SCL2	IRQ11	
D8		PA3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/SSCL5/ SDA2	IRQ6-DS	
E1	VSS					
E2	VBATT					
E3	TDI	P30	MTIOC4B/TMRI3/POE8#/ RTIC0	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	

Table 4.1 List of I/O Registers (Address Order) (23/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 8800h	MTU2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	MTU2a
0008 8801h	MTU2	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8802h	MTU2	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8804h	MTU2	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8805h	MTU2	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8806h	MTU2	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8808h	MTU2	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 880Ah	MTU2	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8880h	MTU5	Timer counter U	TCNTU	16	16	2, 3 PCLKB	2 ICLK	
0008 8882h	MTU5	Timer general register U	TGRU	16	16	2, 3 PCLKB	2 ICLK	
0008 8884h	MTU5	Timer control register U	TCRU	8	8	2, 3 PCLKB	2 ICLK	
0008 8886h	MTU5	Timer I/O control register U	TIORU	8	8	2, 3 PCLKB	2 ICLK	
0008 8890h	MTU5	Timer counter V	TCNTV	16	16	2, 3 PCLKB	2 ICLK	
0008 8892h	MTU5	Timer general register V	TGRV	16	16	2, 3 PCLKB	2 ICLK	
0008 8894h	MTU5	Timer control register V	TCRV	8	8	2, 3 PCLKB	2 ICLK	
0008 8896h	MTU5	Timer I/O control register V	TIORV	8	8	2, 3 PCLKB	2 ICLK	
0008 88A0h	MTU5	Timer counter W	TCNTW	16	16	2, 3 PCLKB	2 ICLK	
0008 88A2h	MTU5	Timer general register W	TGRW	16	16	2, 3 PCLKB	2 ICLK	
0008 88A4h	MTU5	Timer control register W	TCRW	8	8	2, 3 PCLKB	2 ICLK	
0008 88A6h	MTU5	Timer I/O control register W	TIORW	8	8	2, 3 PCLKB	2 ICLK	
0008 88B2h	MTU5	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 88B4h	MTU5	Timer start register	TSTR	8	8	2, 3 PCLKB	2 ICLK	
0008 88B6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	2, 3 PCLKB	2 ICLK	
0008 8900h	POE	Input level control/status register 1	ICSR1	16	16	2, 3 PCLKB	2 ICLK	POE2a
0008 8902h	POE	Output level control/status register 1	OCSR1	16	16	2, 3 PCLKB	2 ICLK	
0008 8908h	POE	Input level control/status register 2	ICSR2	16	16	2, 3 PCLKB	2 ICLK	
0008 890Ah	POE	Software port output enable register	SPOER	8	8	2, 3 PCLKB	2 ICLK	
0008 890Bh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK	
0008 890Ch	POE	Port output enable control register 2	POECR2	8	8	2, 3 PCLKB	2 ICLK	
0008 890Eh	POE	Input level control/status register 3	ICSR3	16	16	2, 3 PCLKB	2 ICLK	
0008 9000h	S12AD	A/D control register	ADCSR	8	8	2, 3 PCLKB	2 ICLK	S12ADa
0008 9004h	S12AD	A/D channel select register 0	ADANS0	16	16	2, 3 PCLKB	2 ICLK	
0008 9006h	S12AD	A/D channel select register 1	ADANS1	16	16	2, 3 PCLKB	2 ICLK	
0008 9008h	S12AD	A/D-converted value addition mode select register 0	ADADS0	16	16	2, 3 PCLKB	2 ICLK	
0008 900Ah	S12AD	A/D-converted value addition mode select register 1	ADADS1	16	16	2, 3 PCLKB	2 ICLK	
0008 900Ch	S12AD	A/D-converted value addition count select register	ADADC	8	8	2, 3 PCLKB	2 ICLK	
0008 900Eh	S12AD	A/D control extended register	ADCER	16	16	2, 3 PCLKB	2 ICLK	
0008 9010h	S12AD	A/D start trigger select register	ADSTRGR	8	8	2, 3 PCLKB	2 ICLK	
0008 9012h	S12AD	A/D conversion extended input control register	ADEXICR	16	16	2, 3 PCLKB	2 ICLK	
0008 901Ah	S12AD	A/D temperature sensor data register	ADTSR	16	16	2, 3 PCLKB	2 ICLK	
0008 901Ch	S12AD	A/D internal reference voltage data register	ADOCDR	16	16	2, 3 PCLKB	2 ICLK	
0008 9020h	S12AD	A/D data register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK	
0008 9022h	S12AD	A/D data register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK	
0008 9024h	S12AD	A/D data register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK	
0008 9026h	S12AD	A/D data register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK	
0008 9028h	S12AD	A/D data register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK	
0008 902Ah	S12AD	A/D data register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK	
0008 902Ch	S12AD	A/D data register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK	
0008 902Eh	S12AD	A/D data register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK	
0008 9030h	S12AD	A/D data register 8	ADDR8	16	16	2, 3 PCLKB	2 ICLK	
0008 9032h	S12AD	A/D data register 9	ADDR9	16	16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (33/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C178h	MPC	P70 pin function control register	P70PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C179h	MPC	P71 pin function control register	P71PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Ah	MPC	P72 pin function control register	P72PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Bh	MPC	P73 pin function control register	P73PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Ch	MPC	P74 pin function control register	P74PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Dh	MPC	P75 pin function control register	P75PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Eh	MPC	P76 pin function control register	P76PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Fh	MPC	P77 pin function control register	P77PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C180h	MPC	P80 pin function control register	P80PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C181h	MPC	P81 pin function control register	P81PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C182h	MPC	P82 pin function control register	P82PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C183h	MPC	P83 pin function control register	P83PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C186h	MPC	P86 pin function control register	P86PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C187h	MPC	P87 pin function control register	P87PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C188h	MPC	P90 pin function control register	P90PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C189h	MPC	P91 pin function control register	P91PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C18Ah	MPC	P92 pin function control register	P92PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C18Bh	MPC	P93 pin function control register	P93PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C190h	MPC	PA0 pin function control register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C191h	MPC	PA1 pin function control register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C192h	MPC	PA2 pin function control register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C193h	MPC	PA3 pin function control register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C194h	MPC	PA4 pin function control register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C195h	MPC	PA5 pin function control register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C196h	MPC	PA6 pin function control register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C197h	MPC	PA7 pin function control register	PA7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C198h	MPC	PB0 pin function control register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C199h	MPC	PB1 pin function control register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Ah	MPC	PB2 pin function control register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Bh	MPC	PB3 pin function control register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Ch	MPC	PB4 pin function control register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Dh	MPC	PB5 pin function control register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Eh	MPC	PB6 pin function control register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Fh	MPC	PB7 pin function control register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A0h	MPC	PC0 pin function control register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A1h	MPC	PC1 pin function control register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A2h	MPC	PC2 pin function control register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A3h	MPC	PC3 pin function control register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A4h	MPC	PC4 pin function control register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A5h	MPC	PC5 pin function control register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A6h	MPC	PC6 pin function control register	PC6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A7h	MPC	PC7 pin function control register	PC7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A8h	MPC	PD0 pin function control register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A9h	MPC	PD1 pin function control register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1AAh	MPC	PD2 pin function control register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1ABh	MPC	PD3 pin function control register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1ACh	MPC	PD4 pin function control register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1ADh	MPC	PD5 pin function control register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1AEh	MPC	PD6 pin function control register	PD6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1AFh	MPC	PD7 pin function control register	PD7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B0h	MPC	PE0 pin function control register	PE0PFS	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (48/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 02A0h	USB1	Pipe 5 transaction counter enable register	PIPE5TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 02A2h	USB1	Pipe 5 transaction counter register	PIPE5TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0400h	USB	Deep standby USB transceiver control/pin monitor register	DPUSR0R	32	32	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0404h	USB	Deep standby USB suspend/resume interrupt register	DPUSR1R	32	32	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0500h	PDC	PDC Control Register 0	PCCR0	32	32	2, 3PCLKA	2 ICLK	PDC
000A 0504h	PDC	PDC Control Register 1	PCCR1	32	32	2, 3PCLKA	2 ICLK	
000A 0508h	PDC	PDC Status Register	PCSR	32	32	2, 3PCLKA	2 ICLK	
000A 050Ch	PDC	PDC Pin Monitor Register	PCMONR	32	32	2, 3PCLKA	2 ICLK	
000A 0510h	PDC	PDC Receive Data Register	PCDR	32	32	2, 3PCLKA	2 ICLK	
000A 0514h	PDC	Vertical Capture Register	VCR	32	32	2, 3PCLKA	2 ICLK	
000A 0518h	PDC	Horizontal Capture Register	HCR	32	32	2, 3PCLKA	2 ICLK	
000C 0000h	EDMAC	EDMAC mode register	EDMR	32	32	5, 6 PCLKA	—	EDMAC
000C 0008h	EDMAC	EDMAC transmit request register	EDTRR	32	32	5, 6 PCLKA	—	
000C 0010h	EDMAC	EDMAC receive request register	EDRRR	32	32	5, 6 PCLKA	—	
000C 0018h	EDMAC	Transmit descriptor list start address register	TDLAR	32	32	5, 6 PCLKA	—	
000C 0020h	EDMAC	Receive descriptor list start address register	RDLAR	32	32	5, 6 PCLKA	—	
000C 0028h	EDMAC	ETHERC/EDMAC status register	EESR	32	32	5, 6 PCLKA	—	
000C 0030h	EDMAC	ETHERC/EDMAC status interrupt permission register	EESIPR	32	32	5, 6 PCLKA	—	
000C 0038h	EDMAC	Transmit/receive status copy enable register	TRSCER	32	32	5, 6 PCLKA	—	
000C 0040h	EDMAC	Receive missed-frame counter register	RMFCR	32	32	5, 6 PCLKA	—	
000C 0048h	EDMAC	Transmit FIFO threshold register	TFTR	32	32	5, 6 PCLKA	—	
000C 0050h	EDMAC	FIFO depth register	FDR	32	32	5, 6 PCLKA	—	
000C 0058h	EDMAC	Receiving method control register	RMCR	32	32	5, 6 PCLKA	—	
000C 0064h	EDMAC	Transmit FIFO underrun counter	TFUCR	32	32	5, 6 PCLKA	—	
000C 0068h	EDMAC	Receive FIFO overflow counter	RFOCR	32	32	5, 6 PCLKA	—	
000C 006Ch	EDMAC	Independent output signal setting register	IOSR	32	32	5, 6 PCLKA	—	
000C 0070h	EDMAC	Flow control start FIFO threshold setting register	FCFTR	32	32	5, 6 PCLKA	—	
000C 0078h	EDMAC	Receive data padding insert register	RPADIR	32	32	5, 6 PCLKA	—	
000C 007Ch	EDMAC	Transmit interrupt setting register	TRIMD	32	32	5, 6 PCLKA	—	
000C 00C8h	EDMAC	Receive buffer write address register	RBWAR	32	32	5, 6 PCLKA	—	
000C 00CCh	EDMAC	Receive descriptor fetch address register	RDFAR	32	32	5, 6 PCLKA	—	
000C 00D4h	EDMAC	Transmit buffer read address register	TBRAR	32	32	5, 6 PCLKA	—	
000C 00D8h	EDMAC	Transmit descriptor fetch address register	TDFAR	32	32	5, 6 PCLKA	—	

Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Supply current*1	High-speed operating mode	Max.*2		I _{CC} *3	—	—	100	mA	ICLK = 100 MHz PCLKA = 100MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 100MHz	
		Normal*4	Peripheral function: clock signal supplied*4		—	52	—			
			Peripheral function: clock signal stopped*4		—	40	—			
		Sleep mode			—	25	65			
		All-module-clock-stop mode (reference value)			—	20	38			
		Increased by BGO operation*5			—	15	—			
	Low-speed operating mode 1*6				—	4	—			ICLK = 1 MHz
	Low-speed operating mode 2				—	1	—			
	Software standby mode				—	0.2	6			
	Deep software standby mode	Power supplied to RAM and USB resume detecting unit			—	22	200			μA
		Power not supplied to RAM and USB resume detecting unit	Power-on reset circuit and low-power consumption function disabled	—	21	60				
			Power-on reset circuit and low-power	—	6.2	28				
		Increase when the RTC is operating	When a crystal oscillator for low clock loads is in use	—	1.0	—				
			When a crystal oscillator for standard clock loads is in use	—	3.0	—				
		RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)	When a crystal oscillator for low clock loads is in use	—	0.9	—	V _{BATT} = 2.0 V, VCC = 0V			
				—	1.6	—	V _{BATT} = 3.3 V, VCC = 0V			
			When a crystal oscillator for standard clock loads is in use	—	1.7	—	V _{BATT} = 2.0 V (for products with 100 pins or more), V _{BATT} = 2.3 V (for the 64-pin product), VCC = 0V			
				—	3.3	—	V _{BATT} = 3.3 V, VCC = 0V			
	Analog power supply current*7	During 12-bit A/D conversion (including temperature sensor)			I _{AVCC0}	—	2.3	3.2	mA	
		During 10-bit A/D conversion			I _{VREFH} *9	—	1.0	1.65		mA
During D/A conversion (per unit)			—	0.7		1.0	mA			
Waiting for A/D, D/A conversion (all units)*10			—	—	25	35		μA		
A/D, D/A converter in standby mode (all units)*10				—	0.1	4.0	μA			
Reference power supply current	During 12-bit A/D conversion			I _{VREFH0}	—	0.6		0.7	mA	
	Waiting for 12-bit A/D conversion (per unit)				—	0.5	0.6	mA		
	12-bit A/D converter in standby mode (per unit)				—	0.1	2.0			μA

5.3.2 Clock Timing

Table 5.12 Clock Timing (Except for Sub-Clock Related)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	Packages with 177 to 144 pins	t _{Bcyc}	20	—	—	ns	Figure 5.3
	Packages with 100 pins or less		40	—	—	ns	
BCLK pin output high pulse width		t _{CH}	5	—	—	ns	
BCLK pin output low pulse width		t _{CL}	5	—	—	ns	
BCLK pin output rising time		t _{Cr}	—	—	5	ns	
BCLK pin output falling time		t _{Cf}	—	—	5	ns	
SDCLK pin output cycle time	only 177 to 144 pin	t _{Bcyc}	20	—	—	ns	
SDCLK pin output high pulse width		t _{CH}	5	—	—	ns	
SDCLK pin output low pulse width		t _{CH}	5	—	—	ns	
SDCLK pin output rising time		t _{CH}	—	—	5	ns	
SDCLK pin output falling time		t _{CH}	—	—	5	ns	
EXTAL external clock input cycle time		t _{EXcyc}	50	—	—	ns	Figure 5.4
EXTAL external clock input high pulse width		t _{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t _{EXL}	20	—	—	ns	
EXTAL external clock rising time		t _{EXr}	—	—	5	ns	
EXTAL external clock falling time		t _{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t _{EXWT}	1	—	—	ms	
Main clock frequency		f _{MAIN}	4	—	16	MHz	
Main clock oscillator start-up time		t _{MAINOSC}	—	—	—*3	ms	Figure 5.5
Main clock oscillation stabilization wait time		t _{MAINOSCWT}	—	—	—*4	ms	
LOCO and IWDTCCLK clock cycle time		t _{cyc}	6.96	8	9.4	μs	
LOCO and IWDTCCLK clock oscillation frequency		f _{LOCO}	106.25	125	143.75	kHz	
LOCO and IWDTCCLK clock oscillation stabilization wait time		t _{LOCOWT}	—	—	20	μs	Figure 5.6
HOCO clock oscillator oscillation frequency		f _{HOCO}	45	50	55	MHz	
HOCO clock oscillation stabilization wait time 1*2		t _{HOCOWT1}	—	—	1.8	ms	Figure 5.7
HOCO clock oscillation stabilization wait time 2		t _{HOCOWT2}	—	—	2.0	ms	Figure 5.8
HOCO clock power supply settling time		t _{HOCOP}	—	—	1	ms	Figure 5.9
PLL clock frequency		f _{PLL}	104	—	200	MHz	
PLL lock time	PLL operation started after main clock oscillation has settled	t _{PLL1}	—	—	500	μs	Figure 5.10
PLL clock oscillation stabilization wait time		t _{PLLWT1}	—	—	—*5	ms	
PLL lock time	PLL operation started before main clock oscillation has settled	t _{PLL2}	—	—	t _{MAINOSC} + t _{PLL1}	ms	Figure 5.11
PLL clock oscillation stabilization wait time		t _{PLLWT2}	—	—	—*5	ms	

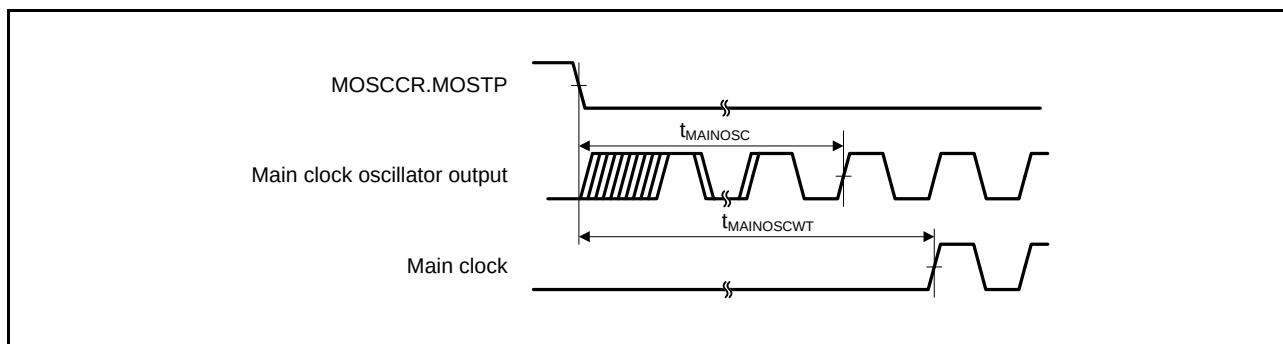


Figure 5.5 Main Clock Oscillation Start Timing

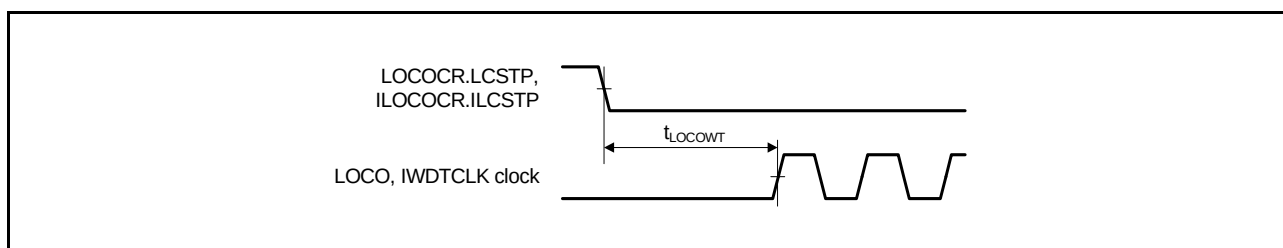


Figure 5.6 LOCO, IWDTCCLK Oscillation Start Timing

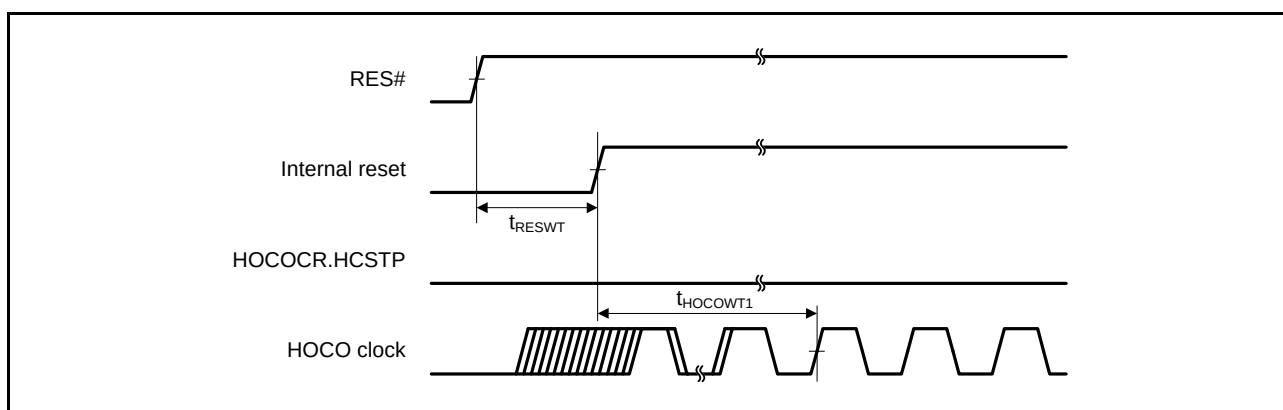


Figure 5.7 HOCO Oscillation Start Timing (After Reset is Canceled by Setting the OFS1.HOCOEN Bit to 0)

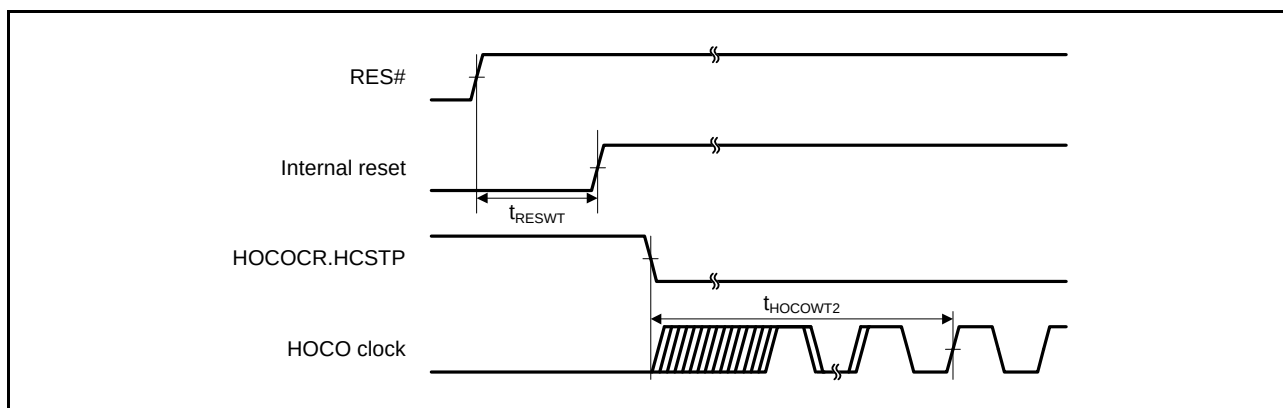


Figure 5.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

5.9 Oscillation Stop Detection Timing

Table 5.34 Oscillation Stop Detection Circuit Characteristics

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.67

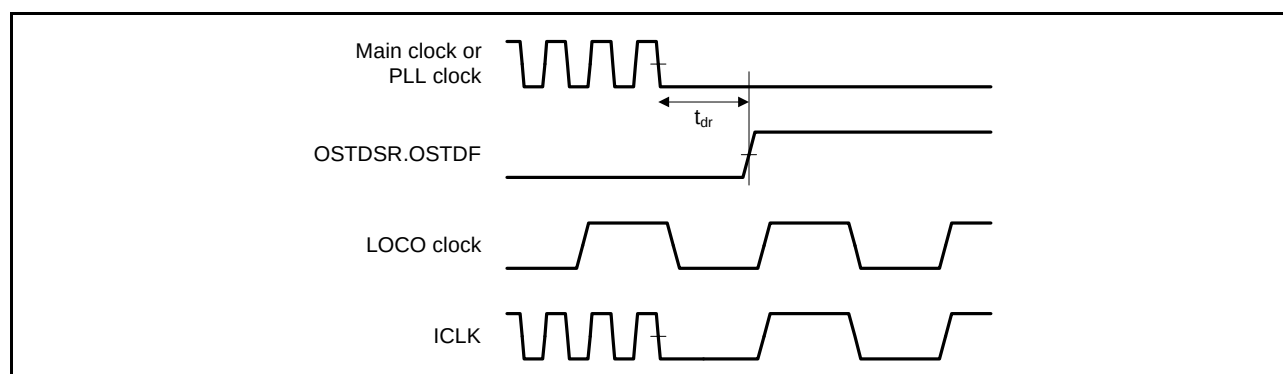


Figure 5.67 Oscillation Stop Detection Timing

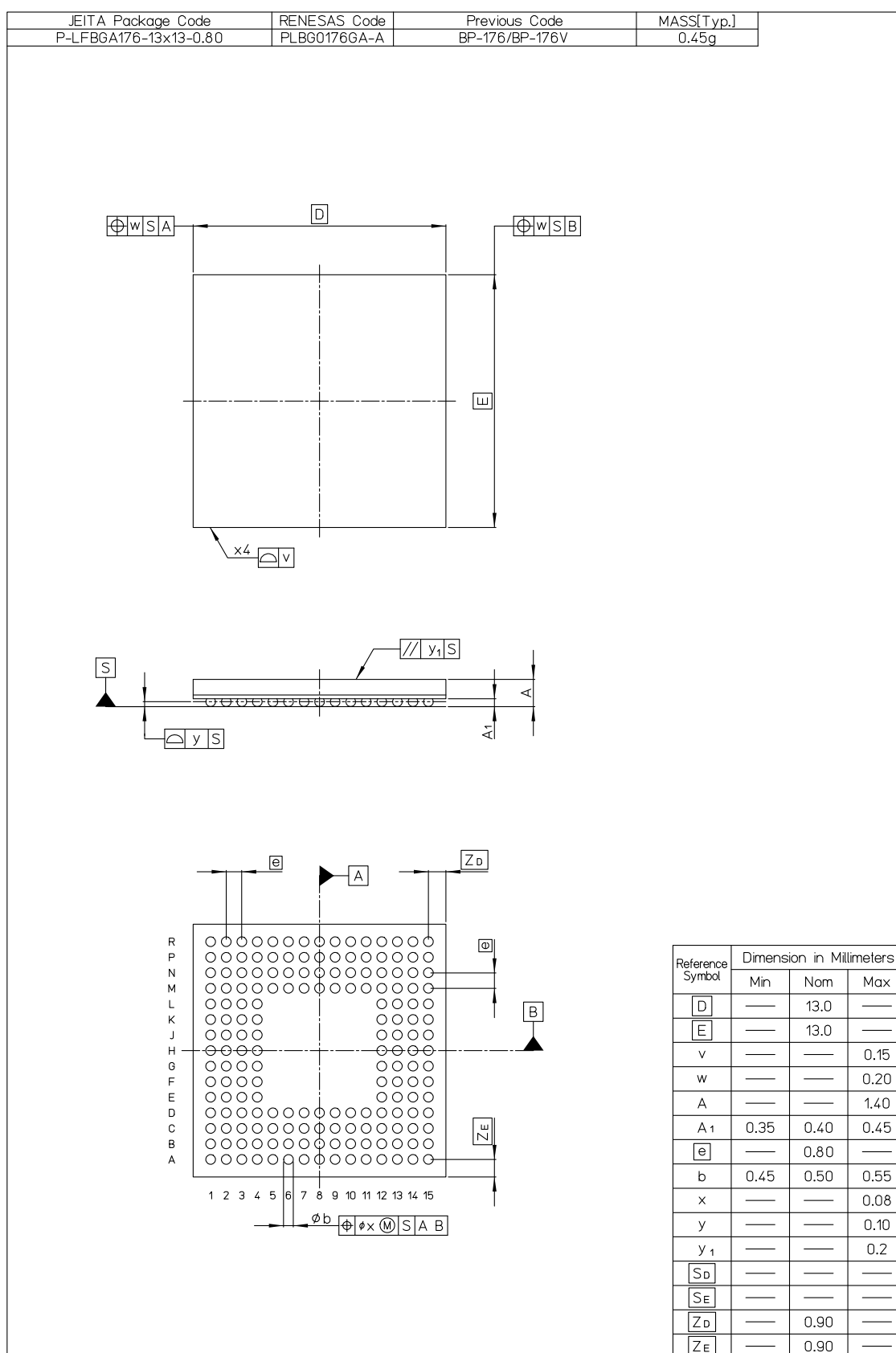


Figure B 176-pin LFBGA (PLBG0176GA-A)

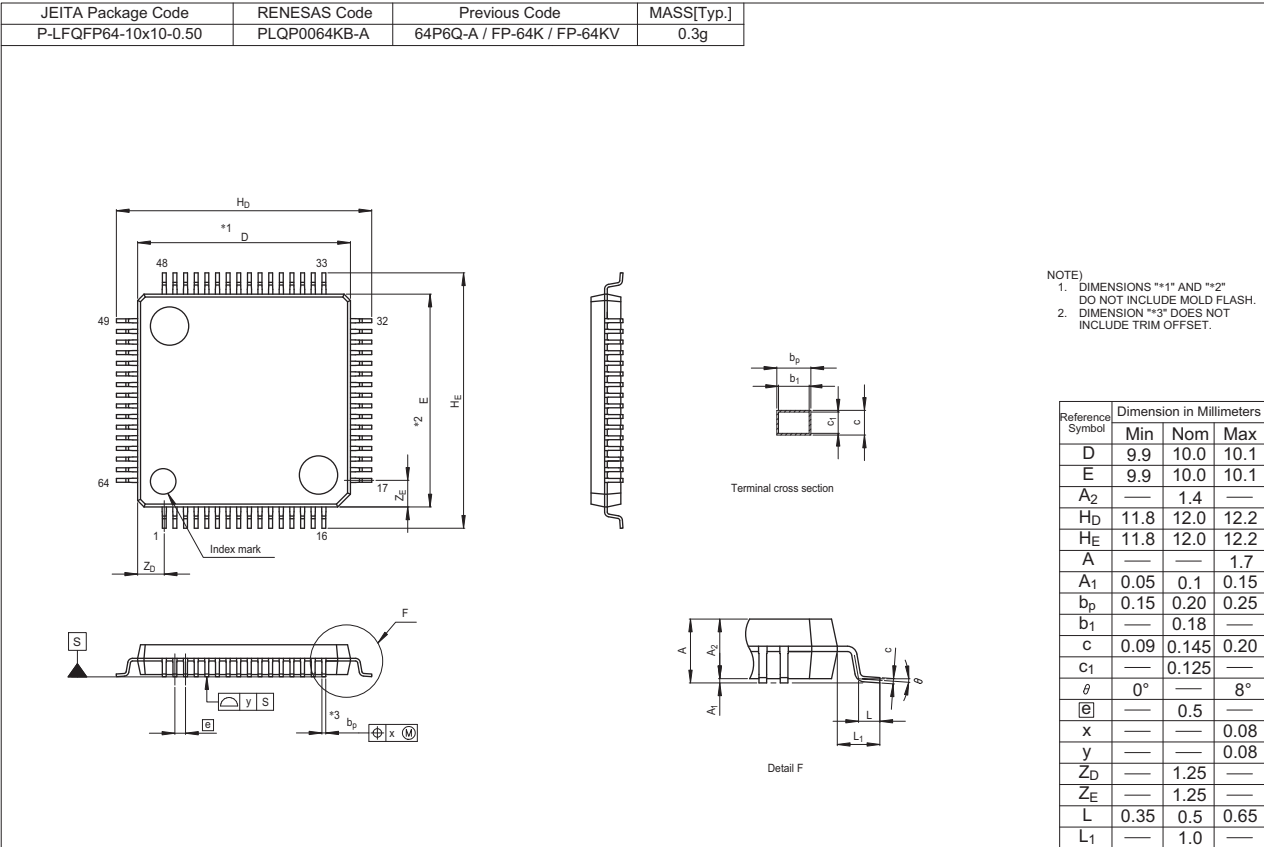


Figure I 64-pin LQFP (PLQP0064KB-A)

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification	
		Page	Summary		
1.80	May 13. 2014	Features			
		1	Operating temp. range chaged, Unique ID added		
		1. Overview			
		2 to 7	Table 1.1 Outline of Specifications: Operating temperature changed, Unique ID and Note 2, added		
		8	Table 1.2 Comparison of Functions for Different Packages: Unique ID, added		
		9 to 16	Table 1.3 List of Products, changed and Note 2, added		TN-RX*-A092A/J
		17	Figure 1.1 How to Read the Product Part Number: Operating temperature range, changed		
		19, 23	Table 1.4 Pin Functions: VBATT and USB power pins, changed		
		3. Address Space			
		76	Figure 3.1 Memory Map in Each Operating Mode, changed		TN-RX*-A081A/E
		77	Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode), changed		TN-RX*-A081A/E
		5. Electrical Characteristics			
		130	Table 5.1 Absolute Maximum Ratings: Operating temperature, changed		
		131	Table 5.2 DC Characteristics (1): Note 1, chaged		
		133 to 134	Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C)): Title		
		135 to 136	Table 5.5 DC Characteristics (4) (for G Version (-85 < Ta ≤ +105°C)), added		
		1921	Table 5.12 Clock Timing (Except for Sub-Clock Related): LOCO changed to LOCO and IWDTCCLKB		
		144	Figure 5.6 LOCO, IWDTCCLK Clock Oscillation Start Timing, added		TN-RX*-A097A/J
		189	Figure 5.68 Battery Backup Function Characteristics changed		

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