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Details

Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56316ddfp-v0

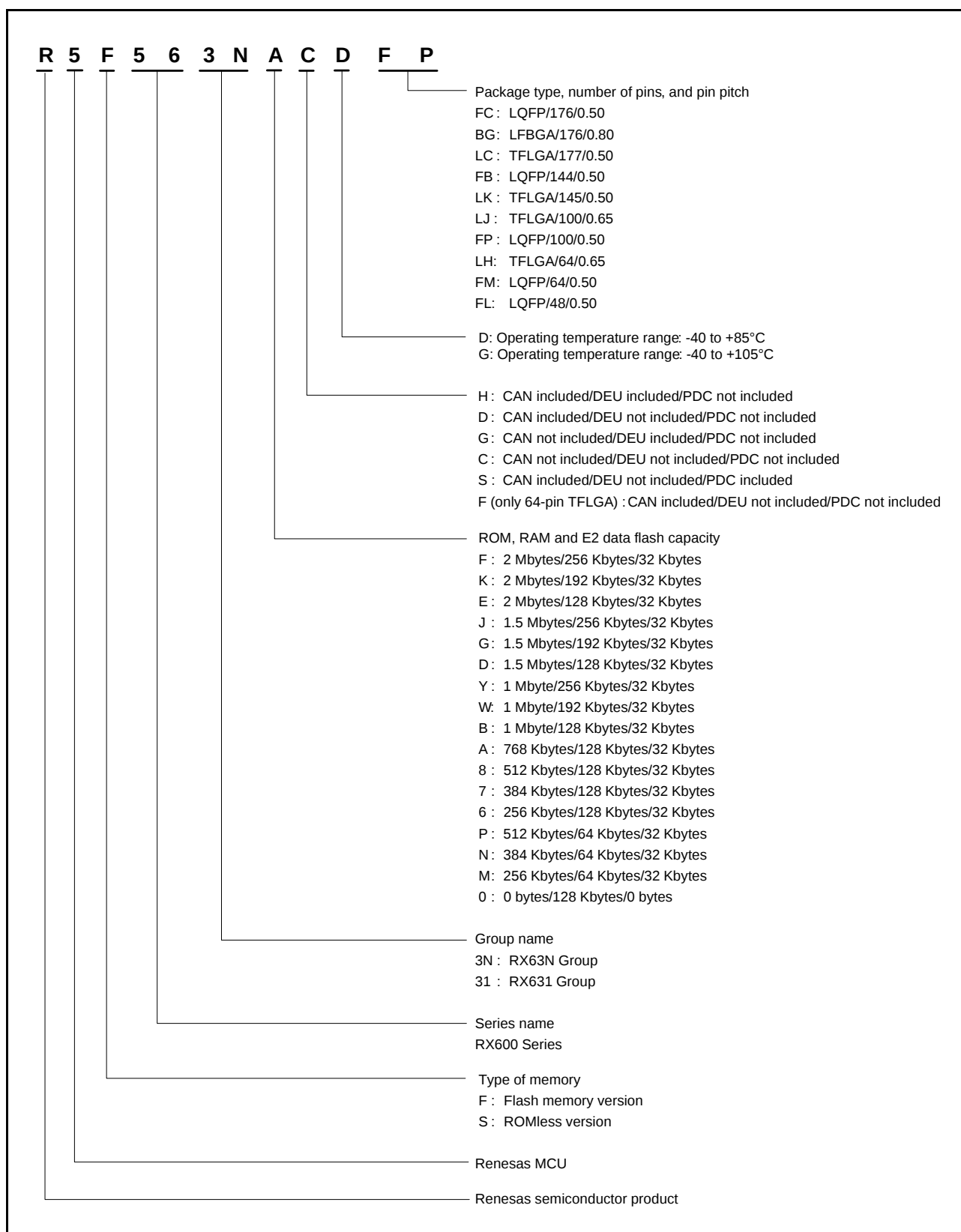


Figure 1.1 How to Read the Product Part No.

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/6)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin. When the battery backup function is not to be used, connect it to the VCC pin.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the clock dedicated for the SDRAM.
	XCOUT	Output	Input/output pins for the subclock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCIN	Input	
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.
On-chip emulator	FINEC	Input	Fine interface clock pin
	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	This pin outputs the clock for synchronization with the trace data.
	TRCLK	Output	
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0 to TRDATA3	Output	These pins output the trace information.
Address bus	A0 to A23	Output	Output pins for the address.
Data bus	D0 to D31	I/O	Input and output pins for the bidirectional data bus.
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	PE3	PE4	VSS	PE6	P67	PA2	PA4	PA7	PB1	PB5	VSS	VCC	P74	13
12	PE1	PE2	P70	PE5	P65	PA1	VCC	PB0	PB2	PB6	P73	PC1	P75	12
11	P62	P61	PE0	VCC	P66	VSS	PA6	P71	PB4	PB7	PC2	PC0	PC3	11
10	VSS	VCC	P63	PE7	PA0	PA3	PA5	P72	PB3	P76	PC4	P77	P82	10
9	PD6	PD4	PD7	P64	RX63N Group RX631 Group PTLG0145KA-A (145-pin TFLGA) (Top perspective view)					P80	PC5	P81	PC7	9
8	PD2	PD0	PD3	P60						VCC	P83	PC6	VSS	8
7	P92	P91	PD1	PD5						P51	P52	P50	P55	7
6	P90	P47	VSS	P93						P53	P56	VSS_ USB	USB0_ DP	6
5	P45	P43	P46	VCC	P44					P54	P13	VCC_ USB	USB0_ DM	5
4	P42	VREFL0	P41	P01	EMLE	VBATT	BSCANP	P35	P30	P15	P24	P12	P14	4
3	P40	P05	VREFH0	P03	PJ5	PJ3	MD/ FINED	VSS	P32	P31	P16	P86	P87	3
2	P07	AVCC0	P02	PF5	VCL	XCOUT	RES#	VCC	P33	P26	P23	P17	P20	2
1	AVSS0	VREFH	VREFL	P00	VSS	XCIN	XTAL	EXTAL	P34	P27	P25	P22	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pins and Pin Functions (145-Pin TFLGA).

Figure 1.6 Pin Assignment (145-Pin TFLGA)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
H3	RES#						
H4		P35				NMI	
H12		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	ET_MDC/TXD5/SMOSI5/ SSDA5/SSLA0	IRQ5-DS	
H13		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	ET_MDIO/RXD5/SMISO5/ SSCL5	IRQ6-DS	
H14		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
H15	TRDATA3	PG7	D31				
J1	EXTAL	P36					
J2	VCC						
J3		P34		MTIOC0A/TMCI3/PO12/ POE2#	SCK6/SCK0/ USB_DPRPD	IRQ4	
J4	TMS	PF3					
J12		PA5	A5	TIOC0B1/PO21	ET_LINKSTA/RSPCKA		
J13	VSS						
J14		PA7	A7	TIOC0B2/PO23	ET_WOL/MISOA		
J15		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	ET_EXOUT/CTS5#/ RTS5#SS5#MOSIA		
K1		P33		MTIOC0D/TIOC0D/ TMRI3/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0/PCKO	IRQ3-DS	
K2		P32		MTIOC0C/TIOC0C/TMO3/ PO10/RTCOU/RTIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC	IRQ2-DS	
K3	TDI	PF2			RXD1/SMISO1/SSCL1		
K4	TCK/FINEC	PF1			SCK1		
K12		PB2	A10	TIOC0C3/TCLKC/PO26	ET_RX_CLK/REF50CK/ CTS4#RTS4#CTS6#/ RTS6#SS4#SS6#		
K13		P71	CS1#		ET_MDIO		
K14	VCC						
K15		PB0	A8	MTIC5W/TIOCA3/PO24	ET_ERXD1/RMII_RXD1/ RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA	IRQ12	
L1		P31		MTIOC4D/TMCI2/PO9/ RTIC1	CTS1#RTS1#SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
L2		P30		MTIOC4B/TMRI3/PO8/ RTIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
L3	TDO	PF0			TXD1/SMOSI1/SSDA1		
L4		P25	CS5#/EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3/ USB_DPRPD/HSYNC		ADTRG0#
L12		PB6	A14	MTIOC3D/TIOCA5/PO30	ET_ETXD1/RMII_TXD1/ RXD9/SMISO9/SSCL9		
L13		PB3	A11	MTIOC0A/MTIOC4A/ TIOC0D/TCLKD/TMO0/ PO27/POE3#	ET_RX_ER/RMII_RX_ER/ SCK4/SCK6		
L14		PB1	A9	MTIOC0C/MTIOC4C/ TIOC0B3/TMCI0/PO25	ET_ERXD0/RMII_RXD0/ TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6	IRQ4-DS	
L15		P72	CS2#		ET_MDC		
M1		P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (1/5)

Pin No.	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
A1	AVSS0						
A2		P07				IRQ15	ADTRG0#
A3		P40				IRQ8-DS	AN000
A4		P42				IRQ10-DS	AN002
A5		P45				IRQ13-DS	AN005
A6		P90	A16		TXD7/SMOSI7/SSDA7		AN014
A7		P92	A18		RXD7/SMISO7/SSCL7		AN016
A8		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
A9		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
A10	VSS						
A11		P62	CS2#/RAS#				
A12		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/ PO18	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB		ANEX1
A13		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/ PO26/POE8#	CTS12#/RTS12#/SS12#/ MISOB/ET_ERXD3		AN1
B1	VREFH						
B2	AVCC0						
B3		P05				IRQ13	DA1
B4	VREFL0						
B5		P43				IRQ11-DS	AN003
B6		P47				IRQ15-DS	AN007
B7		P91	A17		SCK7		AN015
B8		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
B9		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
B10	VCC						
B11		P61	CS1#/SDCS#				
B12		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/ PO23	RXD12/SMISO12/SSCL12/ RXDX12/SSLB3/MOSIB	IRQ7-DS	AN0
B13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0/ET_ERXD2		AN2
C1	VREFL						
C2		P02		TMC11	SCK6	IRQ10	AN020
C3	VREFH0						
C4		P41				IRQ9-DS	AN001
C5		P46				IRQ14-DS	AN006
C6	VSS						
C7		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
C8		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
C9		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
C10		P63	CS3#/CAS#				
C11		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
C12	SDCLK	P70					
C13	VSS						
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
D2		PF5				IRQ4	
D3		P03				IRQ11	DA0
D4		P01		TMC10	RXD6/SMISO6/SSCL6	IRQ9	AN019

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (5/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
N7	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET_EXOUT	IRQ10	
N8	VSS						
N9		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA/ET_COL	IRQ14	
N10	TRSYNC	P82	EDREQ1	MTIOC4A/PO28	TXD10/SMOSI10/SSDA10/ ET_ETXD1/RMII_TXD1		
N11		PC3	A19	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ IETXD/ET_TX_ER		
N12		P75	CS5#	PO20	SCK11/ET_ERXD0/ RMII_RXD0		
N13		P74	CS4#	PO19	CTS11#/RTS11#/SS11#/ ET_ERXD1/RMII_RXD1		

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (2/5)

Pin No. 144-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
36		P21		MTIOC1B/TIOCA3/ TMCIO/PO1	RXD0/SMISO0/SSCL0/ SCL1/USB0_EXICEN/ PIXD5	IRQ9	
37		P20		MTIOC1A/TIOCB3/ TMRIO/PO0	TXD0/SMOSI0/SSDA0/ SDA1/USB0_ID/PIXD4	IRQ8	
38		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2- DS/IETXD/PIXD3	IRQ7	ADTRG#
39		P87		TIOCA2	PIXD2		
40		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/MOSIA/SCL2- DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
41		P86		TIOCA0	PIXD1		
42		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/ TMCIO/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ PIXD0	IRQ5	
43		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRIO/PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
44		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
45		P12		TMCIO	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
46	VCC_USB						
47					USB0_DM		
48					USB0_DP		
49	VSS_USB						
50		P56	EDACK1	MTIOC3C/TIOCA1			
51	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET_EXOUT	IRQ10	
52	TRDATA2	P54	ALE/EDACK0	MTIOC4B/TMCIO	CTS2#/RTS2#/SS2#/ CTX1/ET_LINKSTA		
53		P53*1	BCLK				
54		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
55		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
56		P50	WRO#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
57	VSS						
58	TRCLK	P83	EDACK1	MTIOC4C	CTS10#/RTS10#/ SS10#/ET_CRS/ RMII_CRS_DV		
59	VCC						
60		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA/ET_COL	IRQ14	
61		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TIOCA6/TMCIO/PO30	RXD8/SMOSI8/SSCL8/ MOSIA/ET_ETXD3	IRQ13	
62		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/ TMRIO/PO29	SCK8/RSPCKA/ ET_ETXD2		
63	TRSYNC	P82	EDREQ1	MTIOC4A/PO28	TXD10/SMOSI10/ SSDA10/ET_ETXD1/ RMII_TXD1		

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (2/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
D2	XCOUT						
D3	MD/FINED						
D4	VBATT						
D5		P45				IRQ13-DS	AN005
D6		P46				IRQ14-DS	AN006
D7		PE6	D14[A14/D14]		MOSIB	IRQ6	AN4
D8		PE7	D15[A15/D15]		MISOB	IRQ7	AN5
D9		PA1	A1	MTIOC0B/ MTCLKC/ TIOCBO/PO17	SCK5/SSLA2/ ET_WOL	IRQ11	
D10		PA0	A0/BC0#	MTIOC4A/ TIOCA0/PO16	SSLA1/ET_TX_EN/ RMII_TXD_EN		
E1	XTAL	P37					
E2	VSS						
E3	RES#						
E4	TRST#	P34		MTIOC0A/ TMC13/PO12/ POE2#	SCK6/SCK0/ USB0_DPRPD	IRQ4	
E5		P41				IRQ9-DS	AN001
E6		PA2	A2	PO18	RXD5/SMISO5/ SSCL5/SSLA3		
E7		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMC13/PO22/ POE2#	CTS5#/RTS5#/ SS5#/MOSIA/ ET_EXOUT		
E8		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0/ ET_MDC	IRQ5-DS	
E9		PA5	A5	TIOCBI/PO21	RSPCKA/ ET_LINKSTA		
E10		PA3	A3	MTIOC0D/ MTCLKD/ TIOCDO/ TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET_MDIO	IRQ6-DS	
F1	EXTAL	P36					
F2	VCC						
F3		P35				NMI	
F4		P32		MTIOC0C/ TIOCC0/TMO3/ PO10/ RTCOUT/ RTCIC2	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0*1/ USB0_VBUSEN	IRQ2-DS	
F5		P12		TMC11	RXD2/SMISO2/ SSCL2/SCL0[FM+]	IRQ2	
F6		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCDO/ TCLKD/TMO0/ PO27/POE3#	SCK6/ET_RX_ER/ RMII_RX_ER		

Table 1.11 List of Pins and Pin Functions (64-Pin TFLGA) (2/2)

Pin No. 64-pin TFLGA	Power Supply Clock System Control	I/O Port	Timers (MTU2a, TPUa, TMR, PPG, RTCa, POE2a)	Communications (SClC, SClD, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
E4	TMS	P16	MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ RTCOUT	TXD1/SMOSI1/SSDA1/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
E5		PC4	MTIOC3D/MTCLKC/TMC1/ PO25/POE0#	SCK5/SSLA0/ USB0_DPRPD		
E6	VCC					
E7	VSS					
E8		PB0	MTIC5W/TIOCA3/PO24	RXD6/SMISO6/SSCL6/ RSPCKA	IRQ12	
F1	VCC					
F2		P35			NMI	
F3		P31	MTIOC4D/TMC12/RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
F4		PC5	MTIOC3B/MTCLKD/TMR12/ PO29	RSPCKA/USB0_ID		
F5		P15	MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12	RXD1/SMISO1/SSCL1/ CRX1-DS/USB1_DPUPE	IRQ5	
F6		PB1	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD6/SMOSI6/SSDA6	IRQ4-DS	
F7		PB5	MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1#	SCK9		
F8		PB3	MTIOC0A/MTIOC4A/ TIOC3D/TCLKD/TMO0/ PO27/POE3#	SCK6		
G1	EXTAL	P36				
G2	TDO	P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ MOSIB/USB0_VBUSEN		
G3	VCC_USB					
G4	VSS_USB					
G5	VCC_USB					
G6		PC6	MTIOC3C/MTCLKA/TMC12/ PO30	MOSIA/USB0_EXICEN	IRQ13	
G7		PC3	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ SDA2/IETXD		
G8		PB6	MTIOC3D/TIOCA5/PO30	RXD9/SMISO9/SSCL9		
H1	XTAL	P37				
H2	TRST#	P17	MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ POE8#	SCK1/MISOA/SDA2-DS/ IETXD/USB1_VBUS	IRQ7	
H3				USB0_DM		
H4				USB0_DP		
H5				USB1_DM		
H6				USB1_DP		
H7		PC2	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/SCL2/IERXD		
H8		PB7	MTIOC3B/TIOCB5/PO31	TXD9/SMOSI9/SSDA9		

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP).

The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

Table 4.1 List of I/O Registers (Address Order) (3/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 2818h	EXDMAC0	EXDMA offset register	EDMOFR	32	32	1, 2 BCLK		EXDMACa
0008 281Ch	EXDMAC0	EXDMA transfer enable register	EDMCNT	8	8	1, 2 BCLK		
0008 281Dh	EXDMAC0	EXDMA software start register	EDMREQ	8	8	1, 2 BCLK		
0008 281Eh	EXDMAC0	EXDMA status register	EDMSTS	8	8	1, 2 BCLK		
0008 2820h	EXDMAC0	EXDMA external request sense mode register	EDMRMD	8	8	1, 2 BCLK		
0008 2821h	EXDMAC0	EXDMA external request flag register	EDMERF	8	8	1, 2 BCLK		
0008 2822h	EXDMAC0	EXDMA peripheral request flag register	EDMPRF	8	8	1, 2 BCLK		
0008 2840h	EXDMAC1	EXDMA source address register	EDMSAR	32	32	1, 2 BCLK		
0008 2844h	EXDMAC1	EXDMA destination address register	EDMDAR	32	32	1, 2 BCLK		
0008 2848h	EXDMAC1	EXDMA transfer count register	EDMCRA	32	32	1, 2 BCLK		
0008 284Ch	EXDMAC1	EXDMA block transfer count register	EDMCRB	16	16	1, 2 BCLK		
0008 2850h	EXDMAC1	EXDMA transfer mode register	EDMTMD	16	16	1, 2 BCLK		
0008 2852h	EXDMAC1	EXDMA output setting register	EDMOMD	8	8	1, 2 BCLK		
0008 2853h	EXDMAC1	EXDMA interrupt setting register	EDMINT	8	8	1, 2 BCLK		
0008 2854h	EXDMAC1	EXDMA address mode register	EDMAMD	32	32	1, 2 BCLK		
0008 285Ch	EXDMAC1	EXDMA transfer enable register	EDMCNT	8	8	1, 2 BCLK		
0008 285Dh	EXDMAC1	EXDMA software start register	EDMREQ	8	8	1, 2 BCLK		
0008 285Eh	EXDMAC1	EXDMA status register	EDMSTS	8	8	1, 2 BCLK		
0008 2860h	EXDMAC1	EXDMA external request sense mode register	EDMRMD	8	8	1, 2 BCLK		
0008 2861h	EXDMAC1	EXDMA external request flag register	EDMERF	8	8	1, 2 BCLK		
0008 2862h	EXDMAC1	EXDMA peripheral request flag register	EDMPRF	8	8	1, 2 BCLK		
0008 2A00h	EXDMAC	EXDMA module start register	EDMAST	8	8	1, 2 BCLK		
0008 2BE0h	EXDMAC	Cluster buffer register 0	CLSBR0	32	32	1, 2 BCLK		
0008 2BE4h	EXDMAC	Cluster buffer register 1	CLSBR1	32	32	1, 2 BCLK		
0008 2BE8h	EXDMAC	Cluster buffer register 2	CLSBR2	32	32	1, 2 BCLK		
0008 2BECh	EXDMAC	Cluster buffer register 3	CLSBR3	32	32	1, 2 BCLK		
0008 2BF0h	EXDMAC	Cluster buffer register 4	CLSBR4	32	32	1, 2 BCLK		
0008 2BF4h	EXDMAC	Cluster buffer register 5	CLSBR5	32	32	1, 2 BCLK		
0008 2BF8h	EXDMAC	Cluster buffer register 6	CLSBR6	32	32	1, 2 BCLK		
0008 2BFCh	EXDMAC	Cluster buffer register 7	CLSBR7	32	32	1, 2 BCLK		
0008 3002h	BSC	CS0 mode register	CS0MOD	16	16	1, 2 BCLK		Buses
0008 3004h	BSC	CS0 wait control register 1	CS0WCR1	32	32	1, 2 BCLK		
0008 3008h	BSC	CS0 wait control register 2	CS0WCR2	32	32	1, 2 BCLK		
0008 3012h	BSC	CS1 mode register	CS1MOD	16	16	1, 2 BCLK		
0008 3014h	BSC	CS1 wait control register 1	CS1WCR1	32	32	1, 2 BCLK		
0008 3018h	BSC	CS1 wait control register 2	CS1WCR2	32	32	1, 2 BCLK		
0008 3022h	BSC	CS2 mode register	CS2MOD	16	16	1, 2 BCLK		
0008 3024h	BSC	CS2 wait control register 1	CS2WCR1	32	32	1, 2 BCLK		
0008 3028h	BSC	CS2 wait control register 2	CS2WCR2	32	32	1, 2 BCLK		
0008 3032h	BSC	CS3 mode register	CS3MOD	16	16	1, 2 BCLK		
0008 3034h	BSC	CS3 wait control register 1	CS3WCR1	32	32	1, 2 BCLK		
0008 3038h	BSC	CS3 wait control register 2	CS3WCR2	32	32	1, 2 BCLK		
0008 3042h	BSC	CS4 mode register	CS4MOD	16	16	1, 2 BCLK		
0008 3044h	BSC	CS4 wait control register 1	CS4WCR1	32	32	1, 2 BCLK		
0008 3048h	BSC	CS4 wait control register 2	CS4WCR2	32	32	1, 2 BCLK		
0008 3052h	BSC	CS5 mode register	CS5MOD	16	16	1, 2 BCLK		
0008 3054h	BSC	CS5 wait control register 1	CS5WCR1	32	32	1, 2 BCLK		
0008 3058h	BSC	CS5 wait control register 2	CS5WCR2	32	32	1, 2 BCLK		
0008 3062h	BSC	CS6 mode register	CS6MOD	16	16	1, 2 BCLK		
0008 3064h	BSC	CS6 wait control register 1	CS6WCR1	32	32	1, 2 BCLK		
0008 3068h	BSC	CS6 wait control register 2	CS6WCR2	32	32	1, 2 BCLK		

Table 4.1 List of I/O Registers (Address Order) (24/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 9034h	S12AD	A/D data register 10	ADDR10	16	16	2, 3 PCLKB	2 ICLK	S12ADa
0008 9036h	S12AD	A/D data register 11	ADDR11	16	16	2, 3 PCLKB	2 ICLK	
0008 9038h	S12AD	A/D data register 12	ADDR12	16	16	2, 3 PCLKB	2 ICLK	
0008 903Ah	S12AD	A/D data register 13	ADDR13	16	16	2, 3 PCLKB	2 ICLK	
0008 903Ch	S12AD	A/D data register 14	ADDR14	16	16	2, 3 PCLKB	2 ICLK	
0008 903Eh	S12AD	A/D data register 15	ADDR15	16	16	2, 3 PCLKB	2 ICLK	
0008 9040h	S12AD	A/D data register 16	ADDR16	16	16	2, 3 PCLKB	2 ICLK	
0008 9042h	S12AD	A/D data register 17	ADDR17	16	16	2, 3 PCLKB	2 ICLK	
0008 9044h	S12AD	A/D data register 18	ADDR18	16	16	2, 3 PCLKB	2 ICLK	
0008 9046h	S12AD	A/D data register 19	ADDR19	16	16	2, 3 PCLKB	2 ICLK	
0008 9048h	S12AD	A/D data register 20	ADDR20	16	16	2, 3 PCLKB	2 ICLK	
0008 9060h	S12AD	A/D sampling state register01	ADSSTR01	16	16	2, 3 PCLKB	2 ICLK	
0008 9070h	S12AD	A/D sampling state register 23	ADSSTR23	16	16	2, 3 PCLKB	2 ICLK	
0008 9800h	AD	A/D data register A	ADDRA	16	16	2, 3 PCLKB	2 ICLK	ADb
0008 9802h	AD	A/D data register B	ADDRB	16	16	2, 3 PCLKB	2 ICLK	
0008 9804h	AD	A/D data register C	ADDRC	16	16	2, 3 PCLKB	2 ICLK	
0008 9806h	AD	A/D data register D	ADDRD	16	16	2, 3 PCLKB	2 ICLK	
0008 9808h	AD	A/D data register E	ADDRE	16	16	2, 3 PCLKB	2 ICLK	
0008 980Ah	AD	A/D data register F	ADDRF	16	16	2, 3 PCLKB	2 ICLK	
0008 980Ch	AD	A/D data register G	ADDRG	16	16	2, 3 PCLKB	2 ICLK	
0008 980Eh	AD	A/D data register H	ADDRH	16	16	2, 3 PCLKB	2 ICLK	
0008 9810h	AD	A/D control/status register	ADCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 9811h	AD	A/D control register	ADCR	8	8	2, 3 PCLKB	2 ICLK	
0008 9812h	AD	A/D control register 2	ADCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 9813h	AD	A/D sampling state register	ADSSTR	8	8	2, 3 PCLKB	2 ICLK	
0008 981Fh	AD	A/D self-diagnostic register	ADDIAGR	8	8	2, 3 PCLKB	2 ICLK	
0008 A000h	SCI0	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIC, SCID
0008 A001h	SCI0	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A002h	SCI0	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A003h	SCI0	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A004h	SCI0	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A005h	SCI0	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A006h	SCI0	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A007h	SCI0	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A008h	SCI0	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A009h	SCI0	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A00Ah	SCI0	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A00Bh	SCI0	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A00Ch	SCI0	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A00Dh	SCI0	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A020h	SCI1	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A021h	SCI1	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A022h	SCI1	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A023h	SCI1	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A024h	SCI1	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A025h	SCI1	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A026h	SCI1	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A027h	SCI1	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A028h	SCI1	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A029h	SCI1	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A02Ah	SCI1	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (30/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C046h	PORT6	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C047h	PORT7	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C048h	PORT8	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C049h	PORT9	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Ah	PORTA	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Bh	PORTB	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Ch	PORTC	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Dh	PORTD	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Eh	PORTE	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Fh	PORTF	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C050h	PORTG	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C052h	PORTJ	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C060h	PORT0	Port input data register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C061h	PORT1	Port input data register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C062h	PORT2	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C063h	PORT3	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C064h	PORT4	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C065h	PORT5	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C066h	PORT6	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C067h	PORT7	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C068h	PORT8	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C069h	PORT9	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Ah	PORTA	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Bh	PORTB	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Ch	PORTC	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Dh	PORTD	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Eh	PORTE	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Fh	PORTF	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C070h	PORTG	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C072h	PORTJ	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C080h	PORT0	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C081h	PORT0	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C082h	PORT1	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C083h	PORT1	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C084h	PORT2	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C085h	PORT2	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C086h	PORT3	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C087h	PORT3	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C088h	PORT4	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C089h	PORT4	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Ah	PORT5	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Bh	PORT5	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Ch	PORT6	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Dh	PORT6	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Eh	PORT7	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Fh	PORT7	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C090h	PORT8	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C091h	PORT8	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C092h	PORT9	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C093h	PORT9	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C094h	PORTA	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (35/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C344h	ICU	Group 1 interrupt enable register	GEN01	32	32	1 to 2PCLKB	2 ICLK	ICUb
0008 C348h	ICU	Group 2 interrupt enable register	GEN02	32	32	1 to 2PCLKB	2 ICLK	
0008 C34Ch	ICU	Group 3 interrupt enable register	GEN03	32	32	1 to 2PCLKB	2 ICLK	
0008 C350h	ICU	Group 4 interrupt enable register	GEN04	32	32	1 to 2PCLKB	2 ICLK	
0008 C354h	ICU	Group 5 interrupt enable register	GEN05	32	32	1 to 2PCLKB	2 ICLK	
0008 C358h	ICU	Group 6 interrupt enable register	GEN06	32	32	1 to 2PCLKB	2 ICLK	
0008 C370h	ICU	Group 12 interrupt enable register	GEN12	32	32	1 to 2PCLKB	2 ICLK	
0008 C380h	ICU	Group 0 interrupt clear register	GCR00	32	32	1 to 2PCLKB	2 ICLK	
0008 C384h	ICU	Group 1 interrupt clear register	GCR01	32	32	1 to 2PCLKB	2 ICLK	
0008 C388h	ICU	Group 2 interrupt clear register	GCR02	32	32	1 to 2PCLKB	2 ICLK	
0008 C38Ch	ICU	Group 3 interrupt clear register	GCR03	32	32	1 to 2PCLKB	2 ICLK	
0008 C390h	ICU	Group 4 interrupt clear register	GCR04	32	32	1 to 2PCLKB	2 ICLK	
0008 C394h	ICU	Group 5 interrupt clear register	GCR05	32	32	1 to 2PCLKB	2 ICLK	
0008 C398h	ICU	Group 6 interrupt clear register	GCR06	32	32	1 to 2PCLKB	2 ICLK	
0008 C3C0h	ICU	Unit select register	SEL	32	32	1 to 2PCLKB	2 ICLK	
0008 C400h	RTC	64-Hz counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK	RTCa
0008 C402h	RTC	Second counter	RSECCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C404h	RTC	Minute counter	RMINCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C406h	RTC	Hour counter	RHRCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C408h	RTC	Day-of-week counter	RWKCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Ah	RTC	Date counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Ch	RTC	Month counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Eh	RTC	Year counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 C410h	RTC	Second alarm register	RSECAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C412h	RTC	Minute alarm register	RMINAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C414h	RTC	Hour alarm register	RHRAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C416h	RTC	Day-of-week alarm register	RWKAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C418h	RTC	Date alarm register	RDAYAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C41Ah	RTC	Month alarm register	RMONAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C41Ch	RTC	Year alarm register	RYRAR	16	16	2, 3 PCLKB	2 ICLK	
0008 C41Eh	RTC	Year alarm enable register	RYRAREN	8	8	2, 3 PCLKB	2 ICLK	
0008 C422h	RTC	RTC control register 1	RCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C424h	RTC	RTC control register 2	RCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 C426h	RTC	RTC control register 3	RCR3	8	8	2, 3 PCLKB	2 ICLK	
0008 C428h	RTC	RTC control register 4	RCR4	8	8	2, 3 PCLKB	2 ICLK	
0008 C42Ah	RTC	Frequency register H	RFRH	16	16	2, 3 PCLKB	2 ICLK	
0008 C42Ch	RTC	Frequency register L	RFRL	16	16	2, 3 PCLKB	2 ICLK	
0008 C42Eh	RTC	Time error adjustment register	RADJ	8	8	2, 3 PCLKB	2 ICLK	
0008 C440h	RTC	Time capture control register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK	
0008 C442h	RTC	Time capture control register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C444h	RTC	Time capture control register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 C452h	RTC	Second capture register 0	RSECCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C454h	RTC	Minute capture register 0	RMINCP0	8	8	2, 3 PCLKB	2 ICLK	

Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V _{RAM}	2.7	—	—	V	
VCC rising gradient	SrVCC	8.4	—	20000	μs/V	
VCC falling gradient*8	SfVCC	8.4	—	—	μs/V	

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.

Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK:PCLK:BCLK:BCLK pin = 8:4:4:2)

I_{CC} Max. = 0.87 × f + 13 (max. operation in high-speed operating mode)

I_{CC} Typ. = 0.35 × f + 5 (normal operation in high-speed operating mode)

I_{CC} Typ. = 1.0 × f + 3 (low-speed operating mode 1)

I_{CC} Max. = 0.53 × f + 12 (sleep mode)

Note 4. This does not include the BGO operation.

Note 5. This is the increase for programming or erasure of the ROM or flash memory for data storage during program execution.

Note 6. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Note 7. The reference power supply current is included in the power supply current value for 10-bit A/D conversion and D/A conversion.

Note 8. When V_{BATT} is used

Note 9. The current values for 10-bit A/D converter and 10-bit D/A converter are included in the current from the VREFH pin.

Note 10. The values are the sum of I_{AVCC0} and I_{VREFH}.

Table 5.6 DC Characteristics (4)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible total power consumption*1	P_d	—	—	380	mW	*2

Note 1. This is the total power consumption of the chip as a whole (including the power consumed by the output buffers).

Note 2. Contact a Renesas sales office or agent regarding further details of the conditions of measurement.

Table 5.7 Permissible Output Currents

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	2.0	mA
	All output pins*2	High drive	I_{OL}			3.8	mA
Permissible output low current (max. value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	4.0	mA
	All output pins*2	High drive	I_{OL}			7.6	mA
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	−2.0	mA
	USB_DPUPE pin*2	High drive	I_{OH}	—	—	−3.8	mA
Permissible output high current (max. value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	−4.0	mA
	All output pins*2	High drive	I_{OH}	—	—	−7.6	mA
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	—	—	−80	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

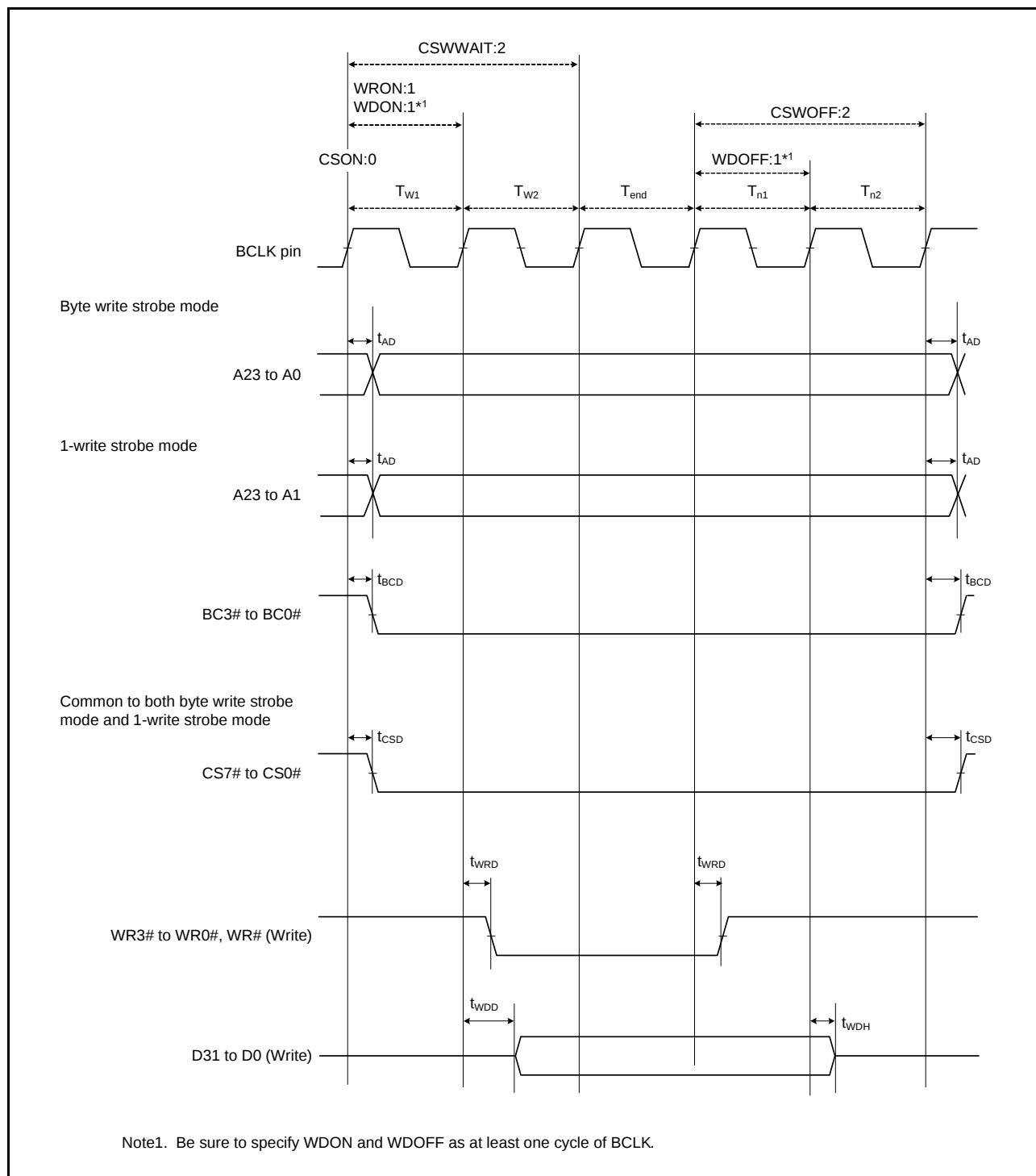


Figure 5.20 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

5.3.6 EXDMAC Timing

Table 5.18 EXDMAC Timing

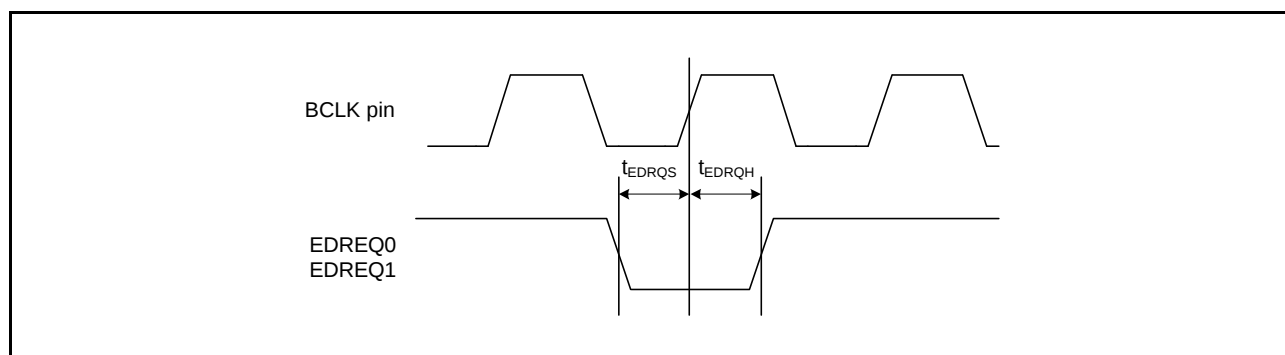
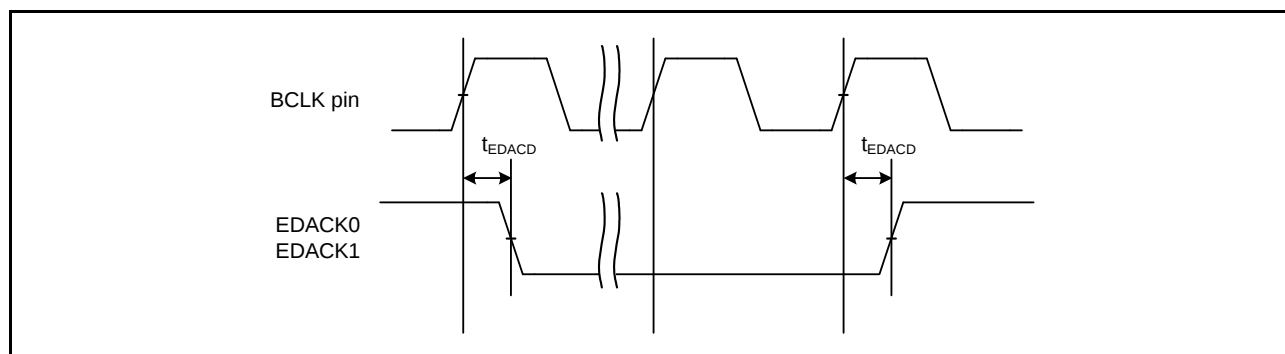
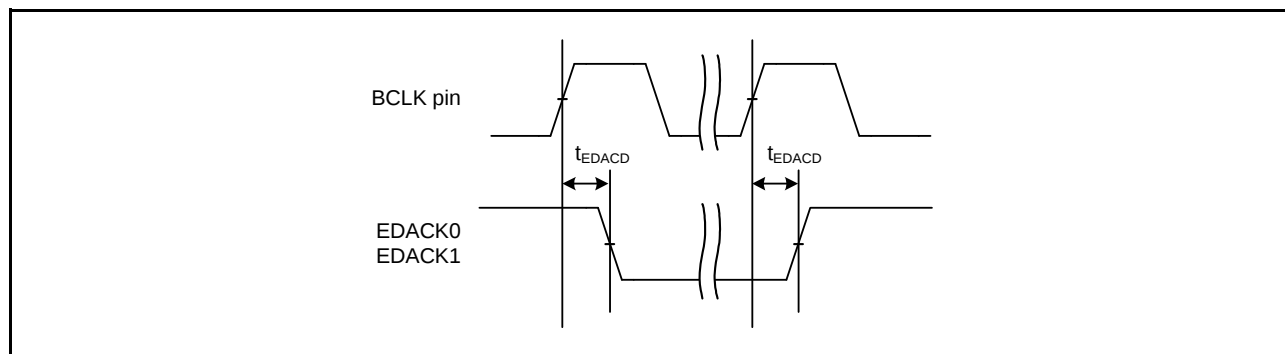
Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,

$V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V

$ICLK = 8$ to 100 MHz, $PCLK = 8$ to 50 MHz, $BCLK$ pin = 8 to 100 MHz, $SDCLK$ pin = 8 to 50 MHz, $T_a = T_{opr}$

High drive output is selected by the drive capacity control register

	Item	Symbol	Min.	Max.	Unit	Test Conditions
EXDMAC	EDREQ setup time	t_{EDRQS}	20	—	ns	Figure 5.31
	EDREQ hold time	t_{EDRQH}	5	—	ns	Figure 5.32 and Figure 5.33
	EDACK delay time	t_{EDACD}	—	15	ns	Figure 5.33

**Figure 5.31 EDREQ0 and EDREQ1 Input Timing****Figure 5.32 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)****Figure 5.33 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)**

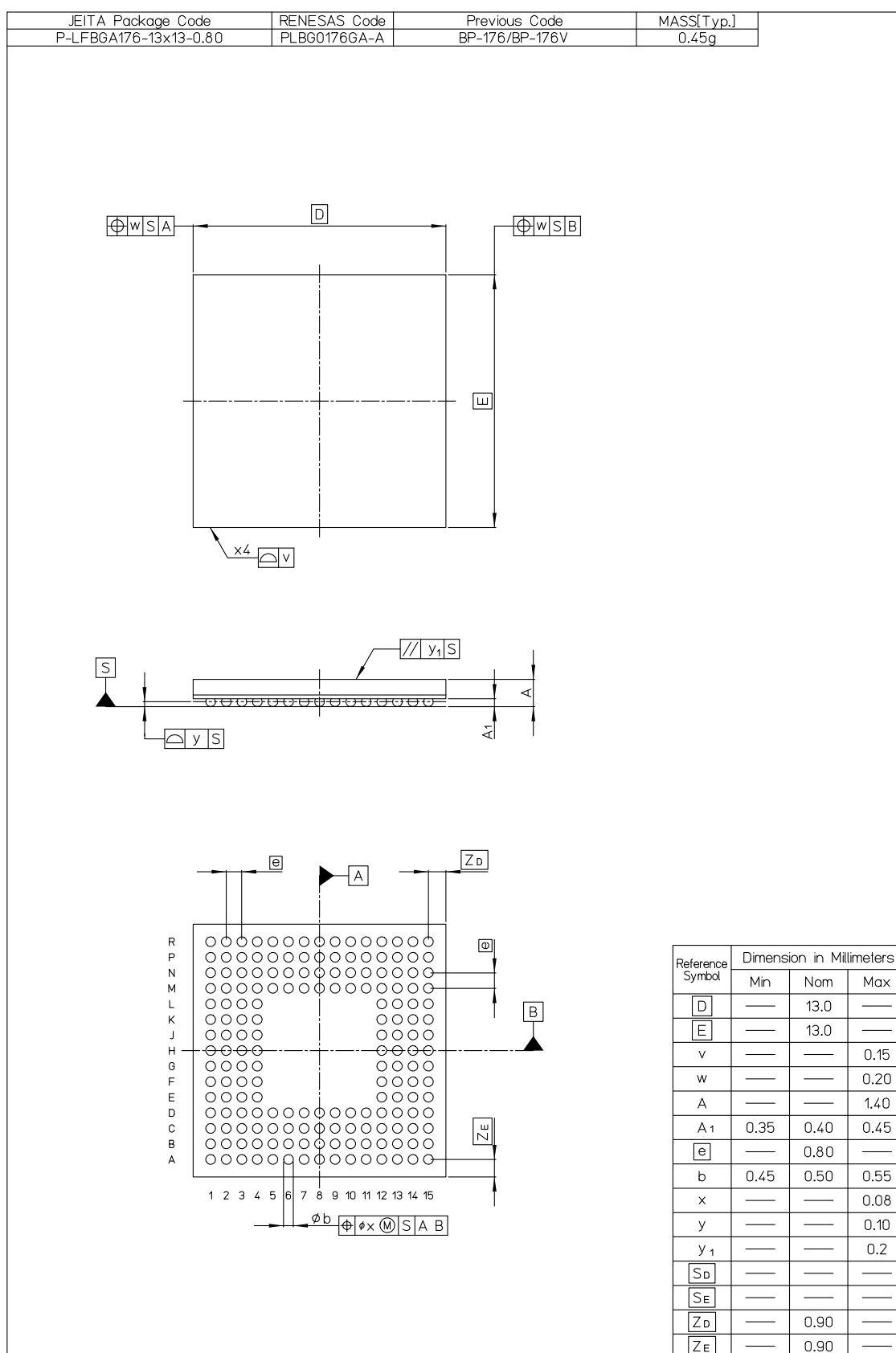


Figure B 176-pin LFBGA (PLBG0176GA-A)

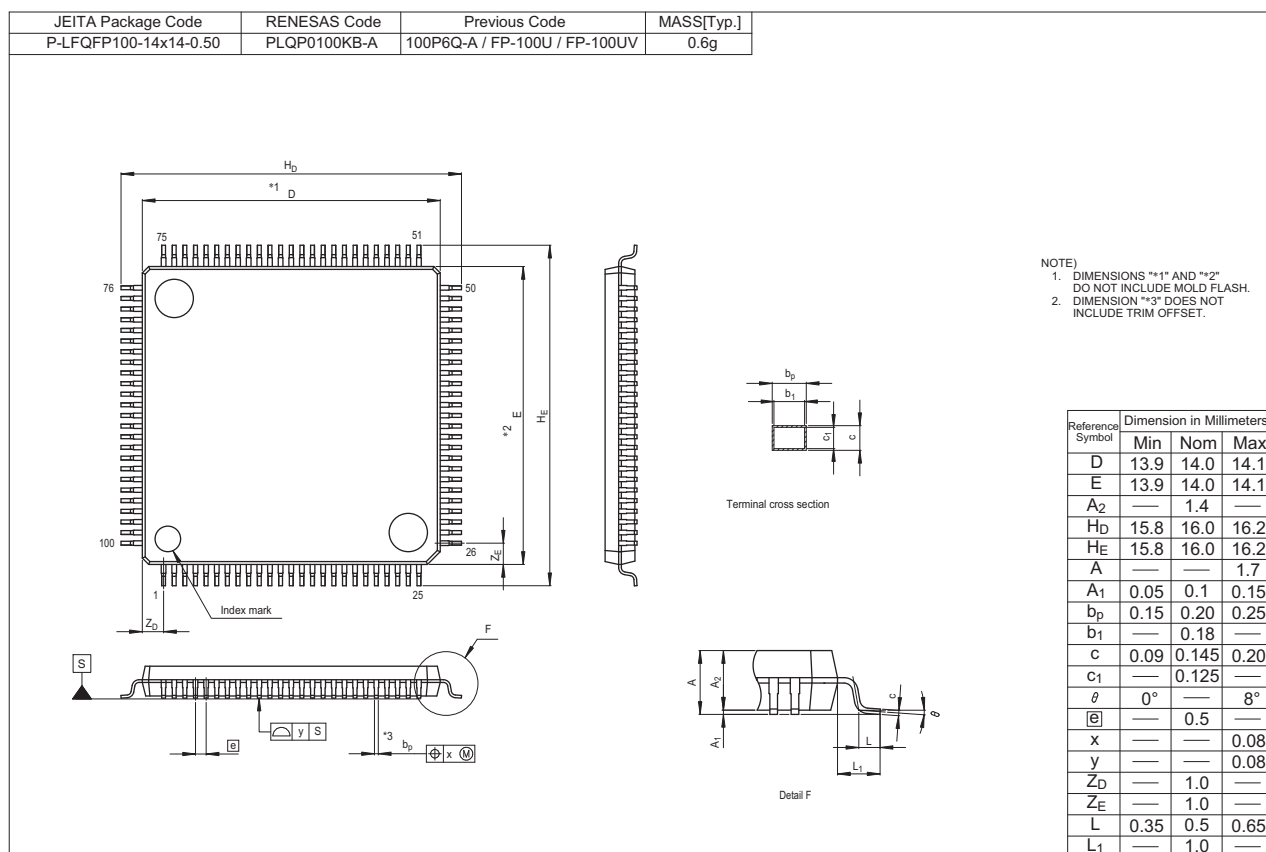


Figure G 100-pin LQFP (PLQP0100KB-A)