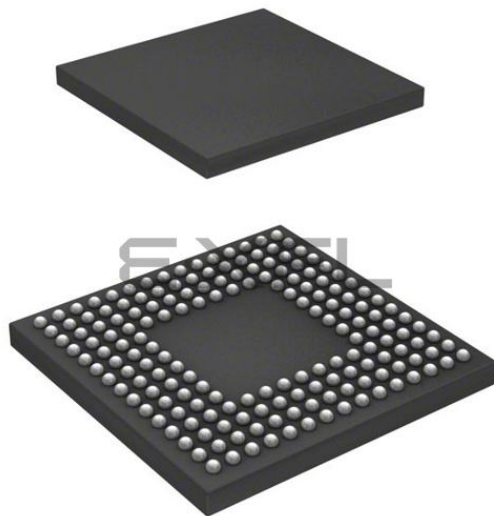




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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56317ddbg-u0

Table 1.3 List of Products (3/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX63N (D version)	R5F563NYHDFP	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYDDFP	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWHDFP	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWDDFP	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWGDFP	PLQP0100KB-A*1	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWCDFP	PLQP0100KB-A*1	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDFP	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDFP	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDFP	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDFP	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
RX63N (G version) *2	R5F563NFHGFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFDGFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NKDGFC	PLQP0176KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NEDGFC	PLQP0176KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NDDGFC	PLQP0176KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYHGFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYDGFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWHGFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWDGFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NBDGFC	PLQP0176KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NADGFC	PLQP0176KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFHGF	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFDGF	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NKDGF	PLQP0144KA-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NEDGF	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NDDGF	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYHGF	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYDGF	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWHGF	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWDGF	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NBDGF	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NADGF	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFHGF	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFDGF	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NKDGF	PLQP0100KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NEDGF	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NDDGF	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYHGF	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYDGF	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWHGF	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWDGF	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NBDGF	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NADGF	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
RX631 (D version)	R5F5631ECDLC	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631EDDLC	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

Table 1.3 List of Products (8/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX631 (G version) *2	R5F5631GDGFB	PLQP0144KA-A	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631DDGFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631YDGFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631WDGFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631BDGFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631ADGFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56318SGFB	PLQP0144KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56318DGFB	PLQP0144KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56317SGFB	PLQP0144KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56317DGFB	PLQP0144KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56316SGFB	PLQP0144KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56316DGFB	PLQP0144KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631FDGFP	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631KDGFP	PLQP0100KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631EDGFP	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631JDGFP	PLQP0100KB-A	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631GDGFP	PLQP0100KB-A	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631DDGFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631YDGFP	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631WDGFP	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631BDGFP	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631ADGFP	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56318DGFP	PLQP0100KB-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56317DGFP	PLQP0100KB-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56316DGFP	PLQP0100KB-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631PDGFM	PLQP0064KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631NDGFM	PLQP0064KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631MDGFM	PLQP0064KB-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631PDGFL	PLQP0048KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631NDGFL	PLQP0048KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631MDGFL	PLQP0048KB-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C

Note 1. In the planning stage

Note 2. The specifications of the temperature sensor calibration and unique ID for G-version products differ from those for other products. For details, see section 45.2.2, Temperature Sensor Calibration Data Registers (TSCDRH, TSCDRL), section 45.3, Using the Temperature Sensor, and section 47.2.22, Unique ID Registers n (UIDRn) (n = 0 to 15) in the User's manual: Hardware.

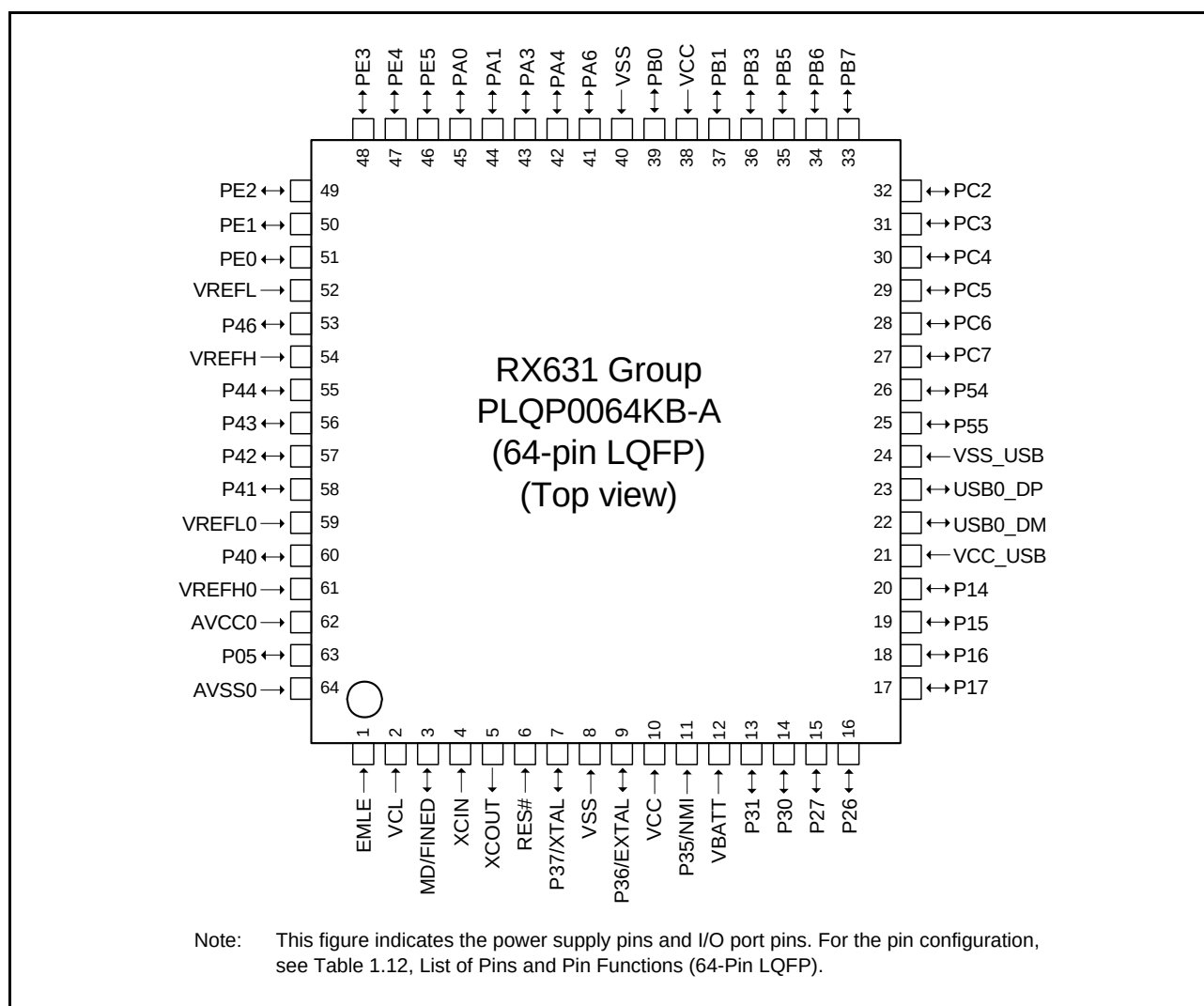


Figure 1.11 Pin Assignment (64-Pin LQFP)

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (5/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
N7	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET_EXOUT	IRQ10	
N8	VSS						
N9		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA/ET_COL	IRQ14	
N10	TRSYNC	P82	EDREQ1	MTIOC4A/PO28	TXD10/SMOSI10/SSDA10/ ET_ETXD1/RMII_TXD1		
N11		PC3	A19	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ IETXD/ET_TX_ER		
N12		P75	CS5#	PO20	SCK11/ET_ERXD0/ RMII_RXD0		
N13		P74	CS4#	PO19	CTS11#/RTS11#/SS11#/ ET_ERXD1/RMII_RXD1		

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (1/5)

Pin No. 144-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
1	AVSS0						
2		P05				IRQ13	DA1
3	VREFH						
4		P03				IRQ11	DA0
5	VREFL						
6		P02		TMC11	SCK6	IRQ10	AN020
7		P01		TMC10	RXD6/SMISO6/SSCL6	IRQ9	AN019
8		P00		TMR10	TXD6/SMOSI6/SSDA6	IRQ8	AN018
9		PF5				IRQ4	
10	EMLE						
11		PJ5					
12	VSS						
13		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
14	VCL						
15	VBATT						
16	MD/FINED						
17	XCIN						
18	XCOUT						
19	RES#						
20	XTAL	P37					
21	VSS						
22	EXTAL	P36					
23	VCC						
24		P35				NMI	
25	TRST#	P34		MTIOC0A/TMC13/ PO12/POE2#	SCK6/SCK0/ USB0_DPRPD	IRQ4	
26		P33		MTIOC0D/TIOC0D/ TMR13/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0/PCKO	IRQ3-DS	
27		P32		MTIOC0C/TIOC0C/ TMO3/PO10/RTCOUT/ RTCIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN/ VSYNC	IRQ2-DS	
28	TMS	P31		MTIOC4D/TMC12/PO9/ RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
29	TDI	P30		MTIOC4B/TMR13/PO8/ RTCIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
30	TCK/FINEC	P27	CS7#	MTIOC2B/TMC13/PO7	SCK1/RSPCKB		
31	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
32		P25	CS5#/EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC		ADTRG0#
33		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMR11/PO4	SCK3/USB0_VBUSEN/ PIXCLK		
34		P23	EDACK0	MTIOC3D/MTCLKD/ TIOC3D/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7		
35		P22	EDREQ0	MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0/USB0_DRPD/ PIXD6		

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (1/4)

Pin No. 100-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCId, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
1	VREFH						
2	EMLE						
3	VREFL						
4		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
5	VCL						
6	VBATT						
7	MD/FINED						
8	XCIN						
9	XCOUT						
10	RES#						
11	XTAL	P37					
12	VSS						
13	EXTAL	P36					
14	VCC						
15		P35				NMI	
16	TRST#	P34		MTIOC0A/TMC13/ PO12/POE2#	SCK6/SCK0/ USB0_DPRPD	IRQ4	
17		P33		MTIOC0D/TIOC0D/ TMR13/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0*1	IRQ3-DS	
18		P32		MTIOC0C/TIOC0C/ TMR03/PO10/RTCOU1/ RTIC12	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0*1/ USB0_VBUSEN	IRQ2-DS	
19	TMS	P31		MTIOC4D/TMC12/PO9/ RTIC11	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
20	TDI	P30		MTIOC4B/TMR13/PO8/ RTIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
21	TCK/FINEC	P27	CS7#	MTIOC2B/TMC13/PO7	SCK1/RSPCKB		
22	TDO	P26	CS6#	MTIOC2A/TMR01/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
23		P25	CS5#/EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3/ USB0_DPRPD		ADTRG0#
24		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMR11/PO4	SCK3/USB0_VBUSEN		
25		P23	EDACK0	MTIOC3D/MTCLKD/ TIOC03/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE		
26		P22	EDREQ0	MTIOC3B/MTCLKC/ TIOC03/TMR0/PO2	SCK0/USB0_DRPD		
27		P21		MTIOC1B/TIOCA3/ TMC10/PO1	RXD0/SMISO0/SSCL0/ USB0_EXICEN	IRQ9	
28		P20		MTIOC1A/TIOCB3/ TMR10/PO0	TXD0/SMOSI0/SSDA0/ USB0_ID	IRQ8	
29		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMR01/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2- DS/IETXD	IRQ7	ADTRG#
30		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMR02/ PO14/RTCOU1	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/MOSIA/SCL2- DS/IETXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#

Table 4.1 List of I/O Registers (Address Order) (8/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 70CBh	ICU	Interrupt request register 203	IR203	8	8	2	ICLK	ICUb
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2	ICLK	
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2	ICLK	
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2	ICLK	
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2	ICLK	
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2	ICLK	
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2	ICLK	
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2	ICLK	
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2	ICLK	
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2	ICLK	
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2	ICLK	
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2	ICLK	
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2	ICLK	
0008 70E2h	ICU	Interrupt request register 226	IR226	8	8	2	ICLK	
0008 70E3h	ICU	Interrupt request register 227	IR227	8	8	2	ICLK	
0008 70E4h	ICU	Interrupt request register 228	IR228	8	8	2	ICLK	
0008 70E5h	ICU	Interrupt request register 229	IR229	8	8	2	ICLK	
0008 70E6h	ICU	Interrupt request register 230	IR230	8	8	2	ICLK	
0008 70E7h	ICU	Interrupt request register 231	IR231	8	8	2	ICLK	
0008 70E8h	ICU	Interrupt request register 232	IR232	8	8	2	ICLK	
0008 70E9h	ICU	Interrupt request register 233	IR233	8	8	2	ICLK	
0008 70EAh	ICU	Interrupt request register 234	IR234	8	8	2	ICLK	
0008 70EBh	ICU	Interrupt request register 235	IR235	8	8	2	ICLK	
0008 70ECh	ICU	Interrupt request register 236	IR236	8	8	2	ICLK	
0008 70EDh	ICU	Interrupt request register 237	IR237	8	8	2	ICLK	
0008 70EEh	ICU	Interrupt request register 238	IR238	8	8	2	ICLK	
0008 70EFh	ICU	Interrupt request register 239	IR239	8	8	2	ICLK	
0008 70F0h	ICU	Interrupt request register 240	IR240	8	8	2	ICLK	
0008 70F1h	ICU	Interrupt request register 241	IR241	8	8	2	ICLK	
0008 70F2h	ICU	Interrupt request register 242	IR242	8	8	2	ICLK	
0008 70F3h	ICU	Interrupt request register 243	IR243	8	8	2	ICLK	
0008 70F4h	ICU	Interrupt request register 244	IR244	8	8	2	ICLK	
0008 70F5h	ICU	Interrupt request register 245	IR245	8	8	2	ICLK	
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2	ICLK	
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2	ICLK	
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2	ICLK	
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2	ICLK	
0008 70FAh	ICU	Interrupt request register 250	IR250	8	8	2	ICLK	
0008 70FBh	ICU	Interrupt request register 251	IR251	8	8	2	ICLK	
0008 70FCh	ICU	Interrupt request register 252	IR252	8	8	2	ICLK	
0008 70FDh	ICU	Interrupt request register 253	IR253	8	8	2	ICLK	
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8	2	ICLK	
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8	2	ICLK	
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8	2	ICLK	
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8	2	ICLK	
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8	2	ICLK	
0008 7121h	ICU	DTC activation enable register 033	DTCER033	8	8	2	ICLK	
0008 7122h	ICU	DTC activation enable register 034	DTCER034	8	8	2	ICLK	
0008 7124h	ICU	DTC activation enable register 036	DTCER036	8	8	2	ICLK	
0008 7125h	ICU	DTC activation enable register 037	DTCER037	8	8	2	ICLK	
0008 7127h	ICU	DTC activation enable register 039	DTCER039	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (38/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 0000h	USB0	System configuration control register	SYSCFG	16	16	3 to 4 PCLKB	2, 3 ICLK	USBa
000A 0004h	USB0	System configuration status register 0	SYSSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0008h	USB0	Device state control register 0	DVSTCTR0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0014h	USB0	CFIFO port register	CFIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 0018h	USB0	D0FIFO port register	D0FIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 001Ch	USB0	D1FIFO port register	D1FIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 0020h	USB0	CFIFO port select register	CFIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0022h	USB0	CFIFO port control register	CFIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0028h	USB0	D0FIFO port select register	D0FIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 002Ah	USB0	D0FIFO port control register	D0FIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 002Ch	USB0	D1FIFO port select register	D1FIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 002Eh	USB0	D1FIFO port control register	D1FIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0030h	USB0	Interrupt enable register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0032h	USB0	Interrupt enable register 1	INTENB1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0036h	USB0	BRDY interrupt enable register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0038h	USB0	NRDY interrupt enable register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	

- Note 1. This is the time until the clock is used after setting P36 and P37 as inputs, and then clearing the main clock oscillator stop bit (MOSCCR.MOSTP) to 0 (selecting operation).
- Note 2. This is the time until the frequency of oscillation by the HOCO (fHOCO) reaches the range for guaranteed operation after release from the reset state.
- Note 3. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.
- Note 4. The number of cycles n selected by the value of the MOSCWTCR.MSTS[4:0] bits determines the main-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{\text{MAINOSCWT}} = t_{\text{MAINOSC}} + \frac{n + 16384}{f_{\text{MAIN}}}$$

- Note 5. The number of cycles n selected by the value of the PLLWTCR.PSTS[4:0] bits determines the PLL-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{\text{PLLWT1}} = t_{\text{PLL}} + \frac{n + 131072}{f_{\text{PLL}}}$$

$$t_{\text{PLLWT2}} = t_{\text{PLL2}} + \frac{n + 131072}{f_{\text{PLL}}} = t_{\text{MAINOSC}} + t_{\text{PLL1}} + \frac{n + 131072}{f_{\text{PLL}}}$$

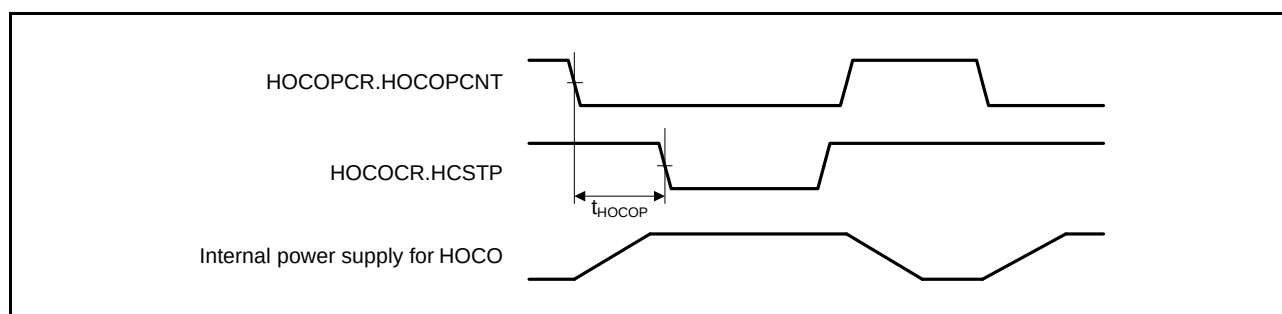


Figure 5.9 HOCO Power Supply Control Timing

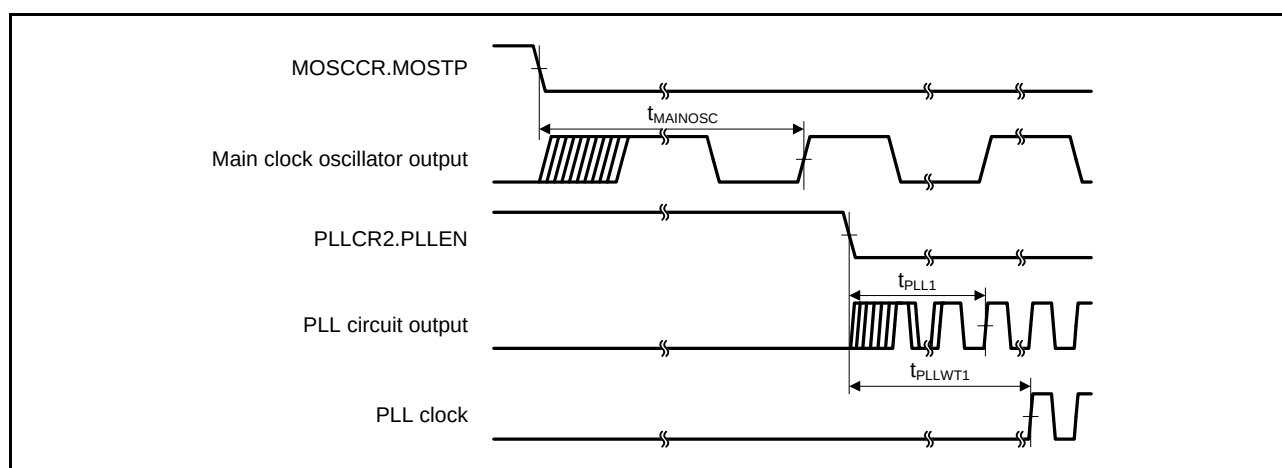


Figure 5.10 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

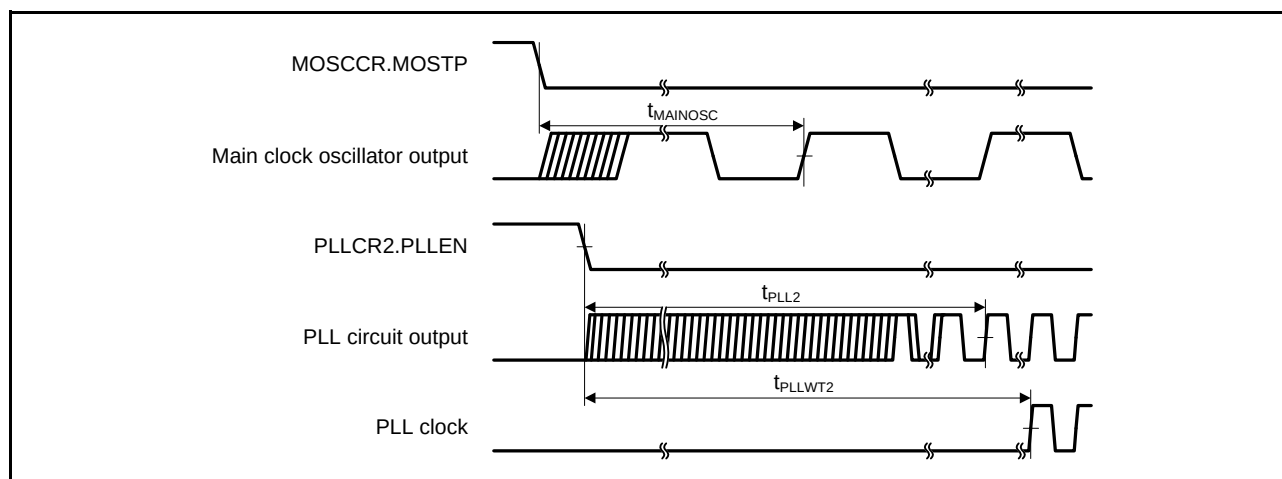


Figure 5.11 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

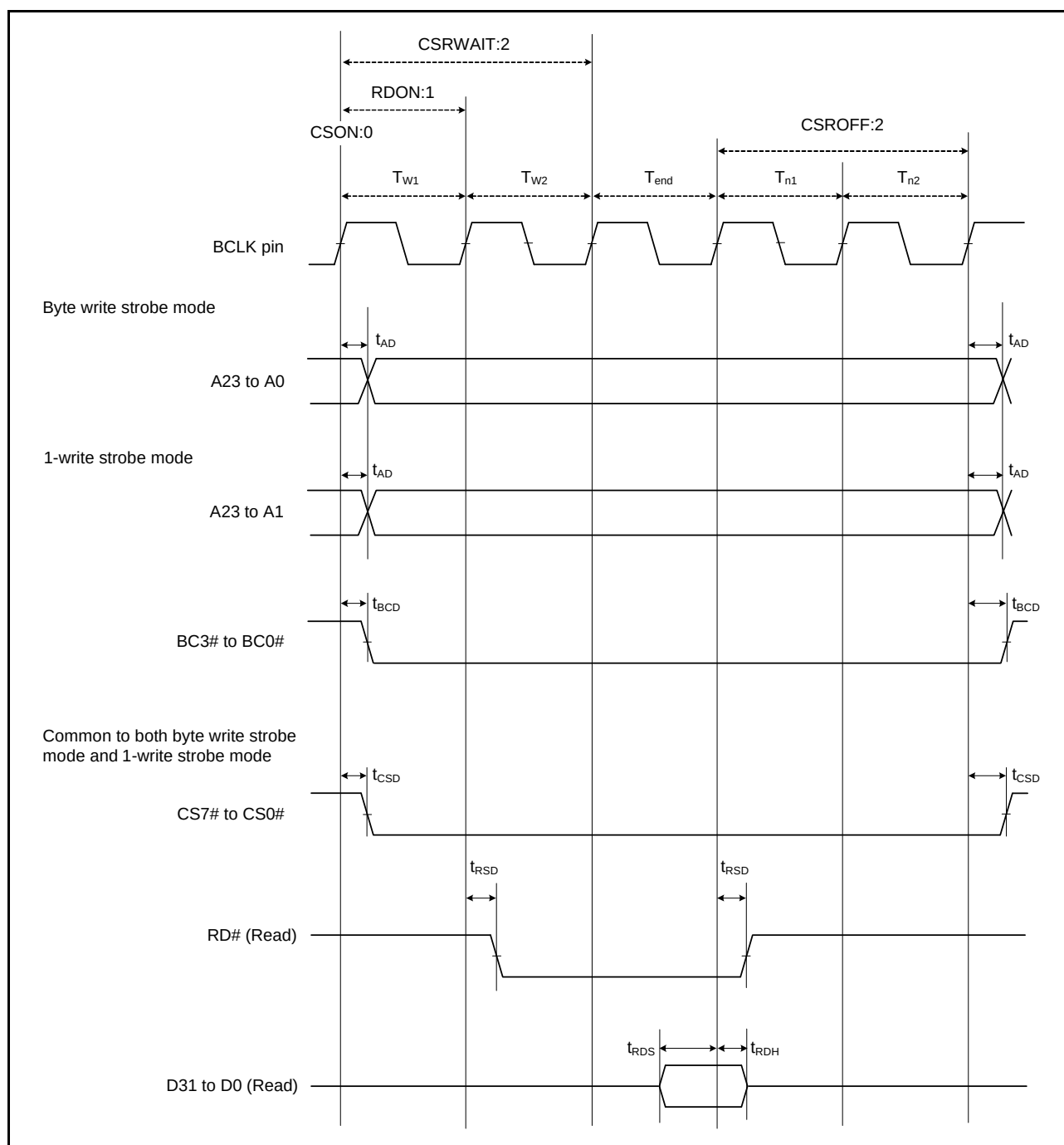
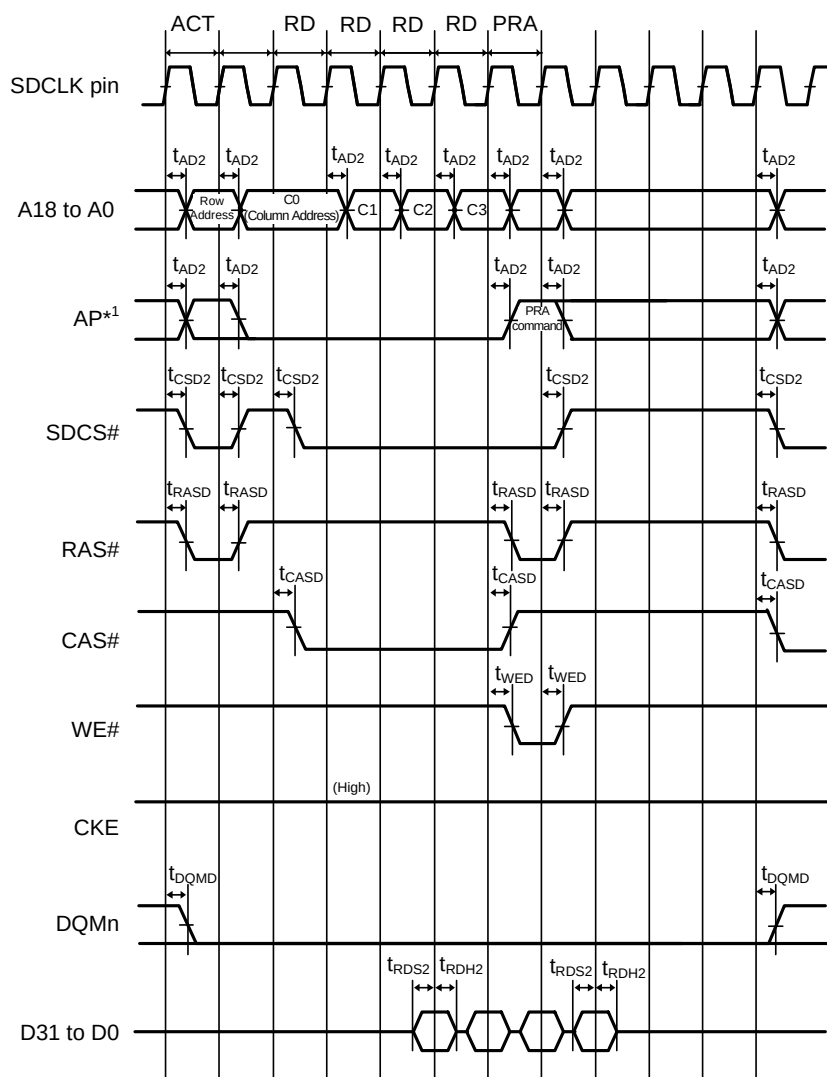


Figure 5.19 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.26 SDRAM Space Multiple Read Bus Timing

Table 5.25 Timing of On-Chip Peripheral Modules (7)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

ICLK = 12.5 to 100 MHz, T_a = T_{opr}

High drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
ETHERC(RMII)	REF50CK cycle time	T _{ck}	20	—	ns	Figure 5.48 to Figure 5.51
	REF50CK frequency Typ. 50 MHz	—	—	50 + 100ppm	MHz	
	REF50CK duty	—	35	65	%	
	REF50CK rise/fall time	T _{ckr/ckf}	0.5	3.5	ns	
	RMII_*** ^{*1} output delay time	T _{co}	2.5	15.0	ns	
	RMII_*** ^{*2} setup time	T _{su}	3	—	ns	
	RMII_*** ^{*2} hold time	T _{hd}	1	—	ns	
	RMII_*** ^{*1, *2} rise/fall time	Tr/Tf	0.5	6	ns	
	ET_WOL output delay time	t _{WOLd}	1	23.5	ns	Figure 5.52
ETHERC(MII)	ET_TX_CLK cycle time	t _{Tcyc}	40	—	ns	—
	ET_TX_EN output delay time	t _{TEND}	1	20	ns	Figure 5.53
	ET_ETXD0 to ET_ETXD3 output delay time	t _{MTDd}	1	20	ns	
	ET_CRs setup time	t _{CRSs}	10	—	ns	
	ET_CRs hold time	t _{CRSh}	10	—	ns	
	ET_COL setup time	t _{COLs}	10	—	ns	Figure 5.54
	ET_COL hold time	t _{COLh}	10	—	ns	
	ET_RX_CLK cycle time	t _{TRcyc}	40	—	ns	—
	ET_RX_DV setup time	t _{RDVs}	10	—	ns	Figure 5.55
	ET_RX_DV hold time	t _{RDVh}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 setup time	t _{MRDs}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 hold time	t _{MRDh}	10	—	ns	
	ET_RX_ER setup time	t _{RERs}	10	—	ns	Figure 5.56
	ET_RX_ER hold time	t _{RESh}	10	—	ns	
	ET_WOL output delay time	t _{WOLd}	1	23.5	ns	Figure 5.57

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0.

Note 2. RMII_CRs_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

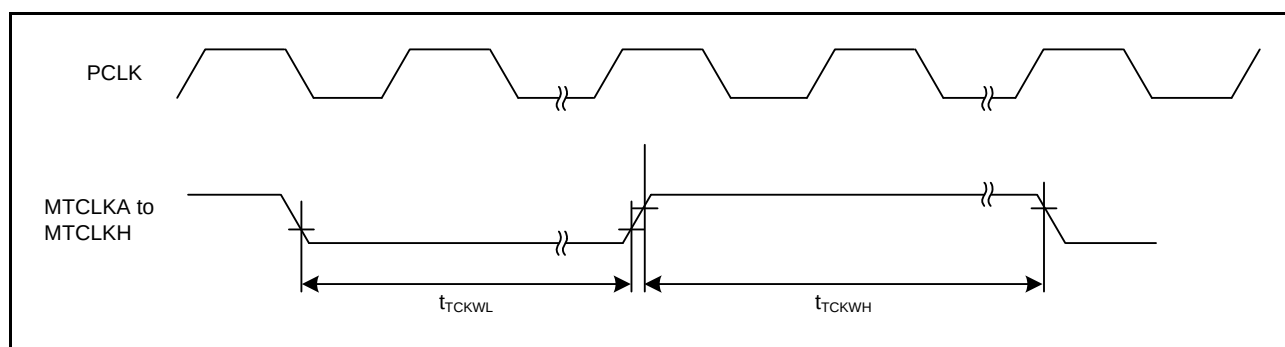


Figure 5.36 MTU Clock Input Timing

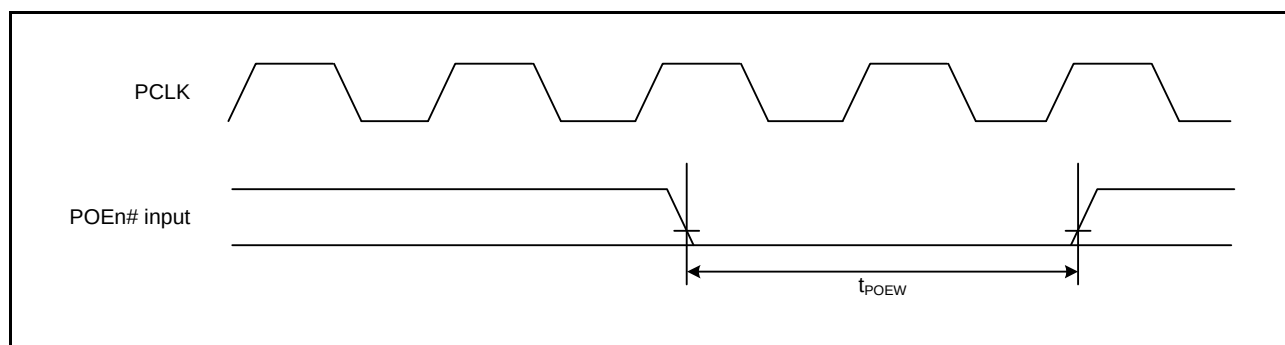


Figure 5.37 POE# Input Timing

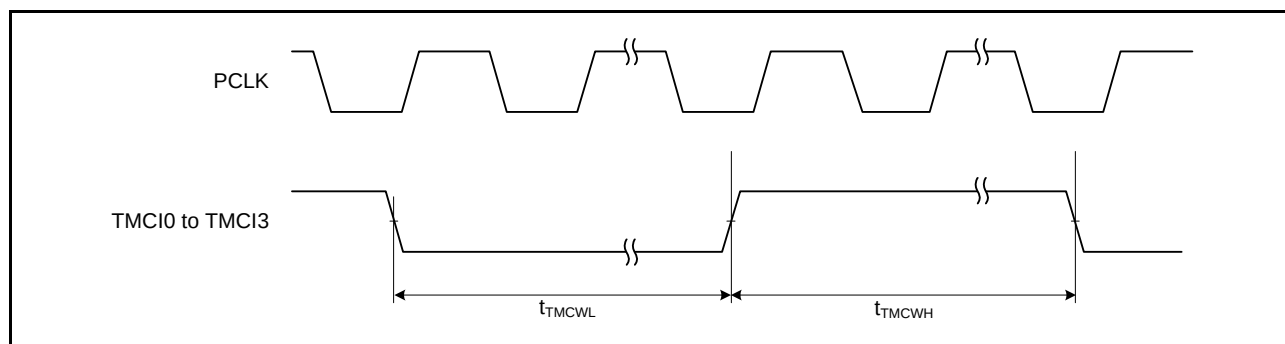


Figure 5.38 8-Bit Timer Clock Input Timing

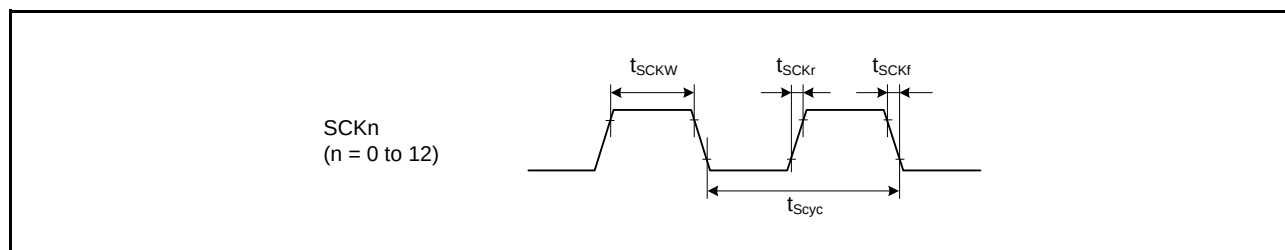


Figure 5.39 SCK Clock Input Timing

Table 5.29 12-Bit A/D Conversion CharacteristicsConditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$ $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V $PCLK = 8$ to 50 MHz $T_a = T_{opr}$

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			—	—	12	Bit	
Conversion time*1 (Operation at PCLK = 50 MHz)	AN0 to AN7	Permissible signal source impedance (max.) = 1.0 kΩ	1.0 (0.4)*2	—	—	μs	Sampling in 20 states
	Other channels	Permissible signal source impedance (max.) = 1.0 kΩ, AVCC ≥ 3.0 V	2.0 (1.4)*2	—	—	μs	Sampling in 70 states
		Permissible signal source impedance (max.) = 1.0 kΩ, AVCC ≥ 2.7 V	5.6 (5.0)*2	—	—	μs	Sampling in 250 states
Analog input capacitance			—	—	30	pF	
Offset error			—	±2.0	±7.5	LSB	
Full-scale error			—	±2.0	±7.5	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	±2.5	±8.0	LSB	
DNL differential nonlinearity error			—	±2.0	±4.0	LSB	
INL integral nonlinearity error			—	±2.0	±4.0	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.30 A/D Internal Reference Voltage CharacteristicsConditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$ $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V $PCLK = 8$ to 50 MHz $T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
A/D Internal reference voltage		1.45	1.50	1.55	V	

5.11 ROM (Flash Memory for Code Storage) Characteristics

Table 5.36 ROM (Flash Memory for Code Storage) Characteristics (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V
Temperature range for the programming/erasure operation: T_a = T_{opr}

Item	Symbol	min	typ	max	Unit	Condition
Reprogram/erasure cycle*1	N _{PEC}	1000	—	—	Times	
Data hold time	t _{DRP}	30*2	—	—	Year	T _a = +85°C

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The result obtained from the reliability test.

Table 5.37 ROM (Flash Memory for Code Storage) Characteristics (2)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
Temperature range for the programming/erasure operation: T_a = T_{opr}

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time N _{PEC} ≤ 100 times	128 bytes	t _{P128}	—	2.8	28	—	1	10	ms
	4 Kbytes	t _{P4K}	—	63	140	—	23	50	ms
	16 Kbytes	t _{P16K}	—	252	560	—	90	200	ms
Programming time N _{PEC} > 100 times	128 bytes	t _{P128}	—	3.4	33.6	—	1.2	12	ms
	4 Kbytes	t _{P4K}	—	75.6	168	—	27.6	60	ms
	16 Kbytes	t _{P16K}	—	302.4	672	—	108	240	ms
Erasure time N _{PEC} ≤ 100 times	4 Kbytes	t _{E4K}	—	50	120	—	25	60	ms
	16 Kbytes	t _{E16K}	—	200	480	—	100	240	ms
Erasure time N _{PEC} > 100 times	4 Kbytes	t _{E4K}	—	60	144	—	30	72	ms
	16 Kbytes	t _{E16K}	—	240	576	—	120	288	ms
Suspend delay time during programming		t _{SPD}	—	—	400	—	—	120	μs
First suspend delay time during erasure (in suspend priority mode)		t _{SESD1}	—	—	300	—	—	120	μs
Second suspend delay time during erasure (in suspend priority mode)		t _{SESD2}	—	—	1.7	—	—	1.7	ms
Suspend delay time during erasure (in erasure priority mode)		t _{SEED}	—	—	1.7	—	—	1.7	ms
FCU reset time		t _{FCUR}	35	—	—	35	—	—	μs

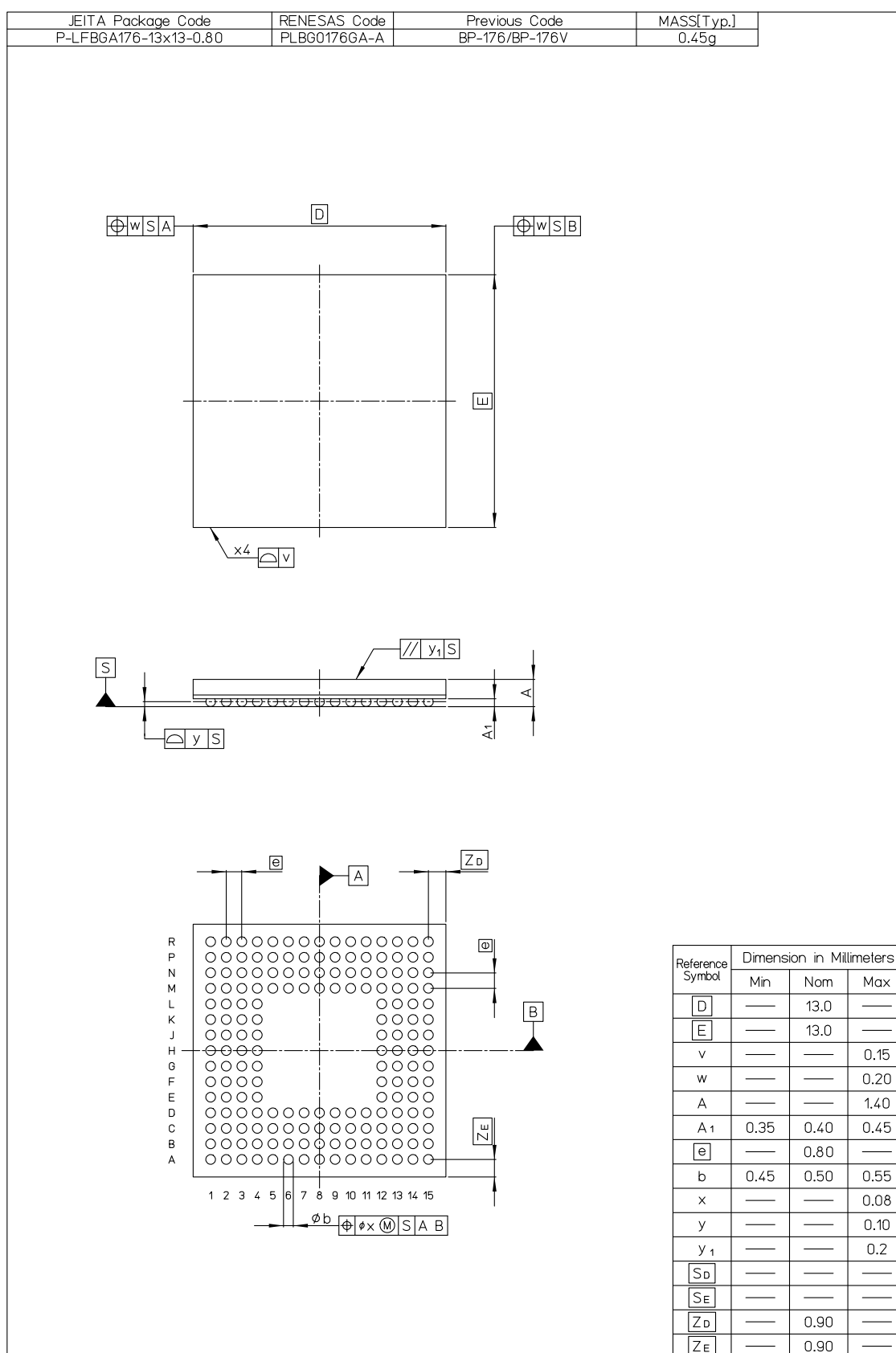


Figure B 176-pin LFBGA (PLBG0176GA-A)

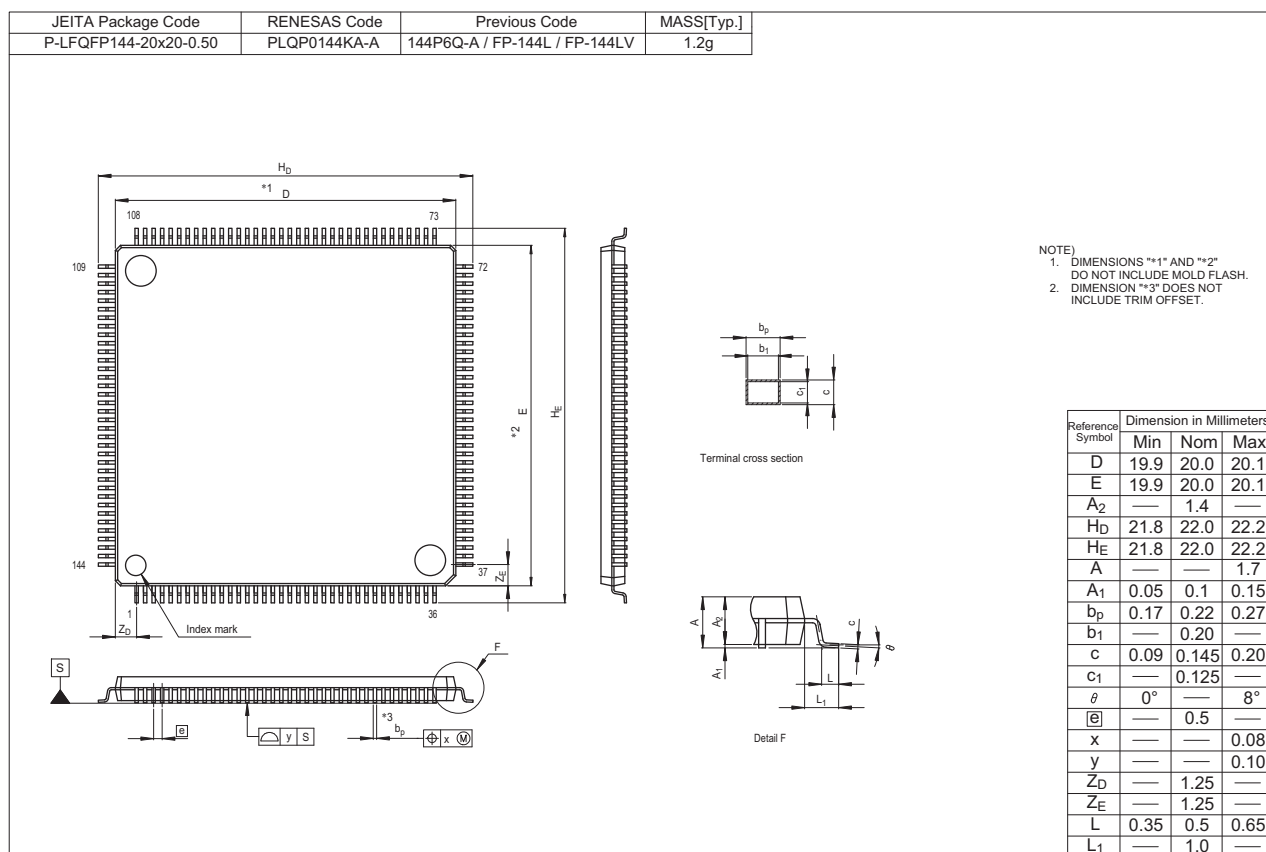


Figure E 144-pin LQFP (PLQP0144KA-A)

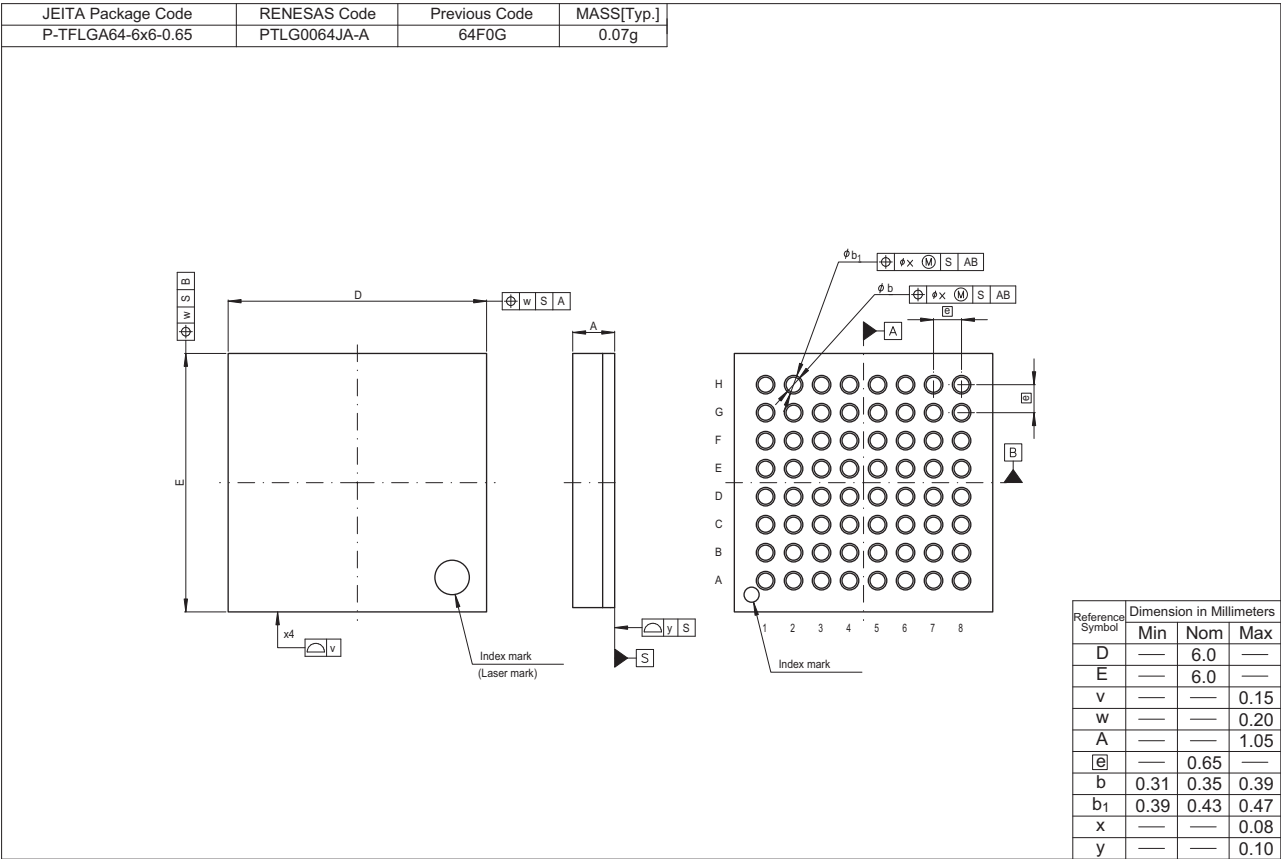


Figure H 64-pin TFLGA (PTLG0064JA-A)

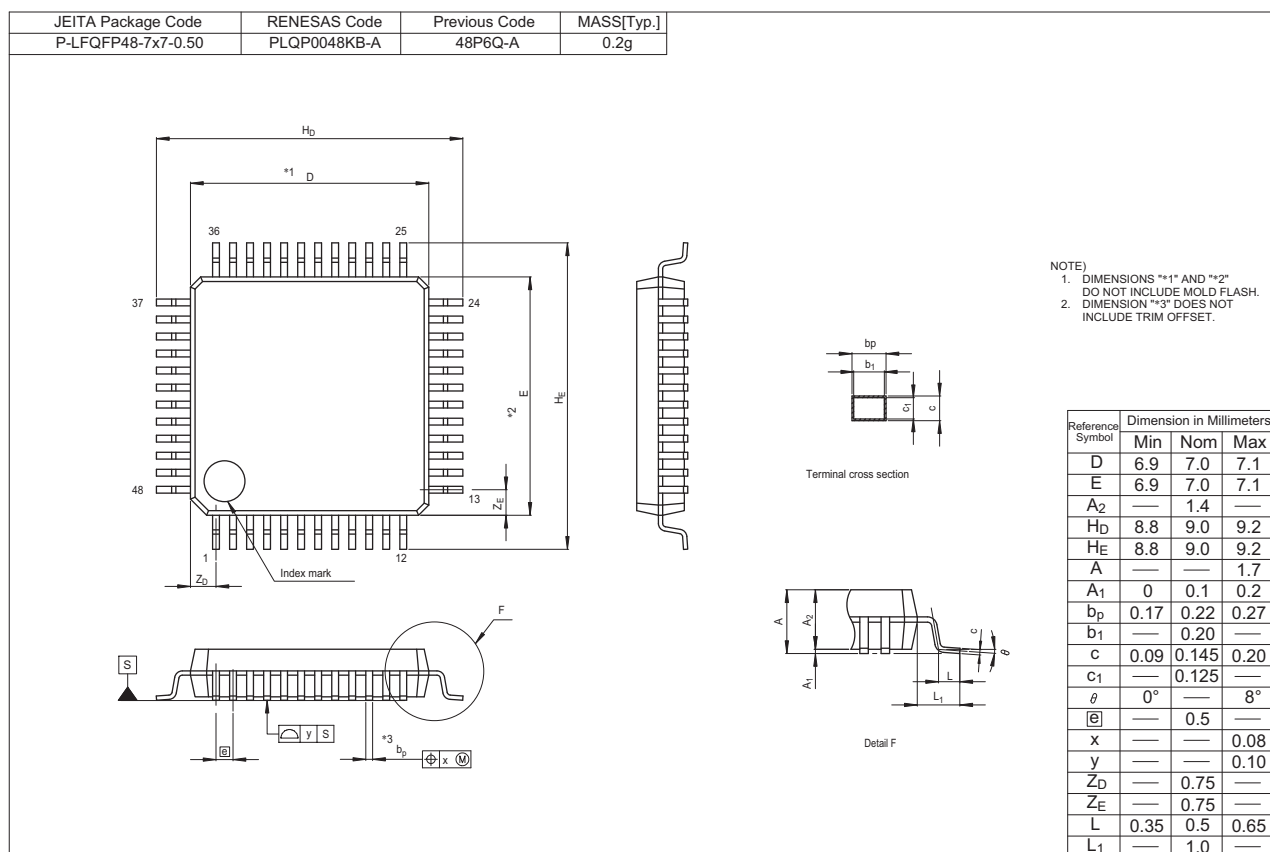


Figure J 48-pin LQFP (PLQP0048KB-A)