Renesas Electronics America Inc - R5F56317DDFC#V0 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56317ddfc-v0

Table 1.1 Outline of Specifications (3/6)

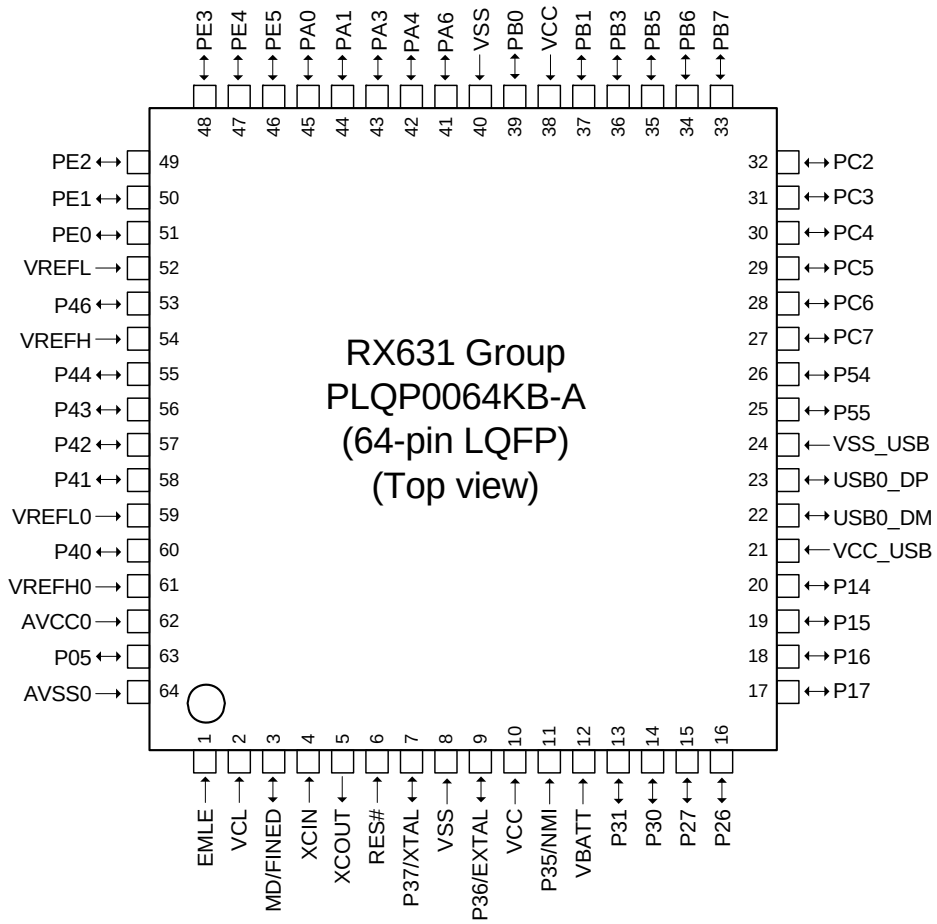
Classification	Module/Function	Description
I/O ports	General I/O ports	• I/O ports for the 177-pin TFLGA, 176-pin LFBGA and 176-pin LQFP I/O pins: 133 Input pins: 1 Pull-up resistors: 133 Open-drain outputs: 133 5-V tolerance: 18 • I/O ports for the 145-pin TFLGA and 144-pin LQFP I/O pins: 111 Input pins: 1 Pull-up resistors: 111 Open-drain outputs: 111 5-V tolerance: 18 • I/O ports for the 100-pin TFLGA (in the planning stage) and 100-pin LQFP I/O pins: 78 Input pins: 1 Pull-up resistors: 78 Open-drain outputs: 78 5-V tolerance: 17 • I/O ports for the 64-pin TFLGA I/O pins: 39 Input pin: 1 Pull-up resistors: 39 Open-drain outputs: 39 5-V tolerance: 8 • I/O ports for the 64-pin LQFP I/O pins: 42 Input pin: 1 Pull-up resistors: 42 Open-drain outputs: 42 5-V tolerance: 8 8-bit port switching function • I/O ports for the 48-pin LQFP I/O pins: 30 Input pin: 1 Pull-up resistors: 30 Open-drain outputs: 30 5-V tolerance: 6 8-bit port switching function

Table 1.1 Outline of Specifications (5/6)

Classification	Module/Function	Description
Communication function	Ethernet controller (ETHERC)	• Input and output of Ethernet/IEEE 802.3 frames • Transfer at 10 or 100 Mbps • Full- and half-duplex modes • MII (Media Independent Interface) or RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u • Detection of Magic Packets™*1 or output of a "wake-on-LAN" signal (WOL) • Compliance with flow control as defined in IEEE 802.3x standards Note 1. Magic PacketTM is a registered trademark of Advanced Micro Devices, Inc.
	DMA controller for Ethernet controller (EDMAC)	• Alleviation of CPU loads by the descriptor control method • Transmission FIFO: 2 Kbytes; Reception FIFO: 2 Kbytes
	USB 2.0 host/function module (USBa)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 • Host/function module: one port, function module: one port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps) • Self-power mode and bus-power mode are selectable • OTG (On the Go) operation is possible • Incorporates 2 Kbytes of RAM as a transfer buffer
	Serial communications interfaces (SCIc, SCId)	• 13 channels (SCIc: 12 channels + SCId: 1 channel) • SCIc Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Simple I^2C Simple SPI • SCId (The following functions are added to SCIc) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	I^2C bus interfaces (RIIC)	• 4 channels (one of them is FM+) • Communication formats I^2C bus format/SMBus format Supports the multi-master Max. transfer rate: 1 Mbps (channel 0)
	IEBus (IEB)	• 1 channel • Supports protocol control for the IEBus Half-duplex asynchronous transfer Multi-master operation Broadcast communications function Two selectable modes, differentiated by transfer rate
	CAN module (CAN)	• 3 channels • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes each
	Serial peripheral interfaces (SPI)	• 3 channels • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure Double buffers for both transmission and reception

Table 1.4 Pin Functions (2/6)

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode.
	WR0# to WR3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16, and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0# to BC3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16, and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
	CKE	Output	Output pin for SDRAM clock enable signals.
	SDCS#	Output	Output pin for SDRAM chip select signals.
	RAS#	Output	Output pin for SDRAM row address strobe signals.
	CAS#	Output	Output pin for SDRAM column address strobe signals.
	WE#	Output	Output pin for SDRAM write enable signals.
	DQM0 to DQM3	Output	Output pins for SDRAM I/O data mask enable signals.
	CS0# to CS7#	Output	Select signals for CS area.
	WAIT#	Input	Input pins for wait request signals in access to the external space.
EXDMA controller	EDREQ0, EDREQ1		Input pins for external DMA transfer requests.
	EDACK0, EDACK1		Output pins for single address transfer acknowledge signals.
Interrupt	NMI	Input	Non-maskable interrupt request signal.
	IRQ0 to IRQ15	Input	Maskable interrupt request signals.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins.
	MTCLKA, MTCLKB MTCLKC, MTCLKD	Input	Input pins for external clock signals.
Port output enable 2	POE0# to POE3# POE8#	Input	Input pins for request signals to place the MTU large-current pins in the high impedance state.



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.12, List of Pins and Pin Functions (64-Pin LQFP).

Figure 1.11 Pin Assignment (64-Pin LQFP)

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (5/5)

Pin No. 144-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
125		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
126		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
127		P93	A19		CTS7#/RTS7#/SS7#		AN017
128		P92	A18		RXD7/SMISO7/SSCL7		AN016
129		P91	A17		SCK7		AN015
130	VSS						
131		P90	A16		TXD7/SMOSI7/SSDA7		AN014
132	VCC						
133		P47				IRQ15-DS	AN007
134		P46				IRQ14-DS	AN006
135		P45				IRQ13-DS	AN005
136		P44				IRQ12-DS	AN004
137		P43				IRQ11-DS	AN003
138		P42				IRQ10-DS	AN002
139		P41				IRQ9-DS	AN001
140	VREFL0						
141		P40				IRQ8-DS	AN000
142	VREFH0						
143	AVCC0						
144		P07				IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (3/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
F7		PB2	A10	TIOCC3/ TCLKC/PO26	CTS6#/RTS6#/ SS6#/ET_RX_CLK/ REF50CK		
F8		PB0	A8	MTIC5W/ TIOCA3/PO24	RXD6/SMISO6/ SSCL6/RSPCKA/ ET_ERXD1/ RMII_RXD1	IRQ12	
F9		PA7	A7	TIOCB2/PO23	MISOA/ET_WOL		
F10	VSS						
G1		P33		MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE3#	RXD6/RXD0/ SMISO6/SMISO0/ SSCL6/SSCL0/ CRX0*1	IRQ3-DS	
G2	TMS	P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0/ USB0_DPUPE	IRQ1-DS	
G3	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/MISOB/ USB0_DRPD	IRQ0-DS	
G4	TCK/FINEC	P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB		
G5	BCLK	P53*2					
G6		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3		
G7		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE1#	SCK9/ET_ETXD0/ RMII_TXD0		
G8		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/ SS9#/ET_TX_EN/ RMII_TXD_EN		
G9		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	TXD6/SMOSI6/ SSDA6/ET_ERXD0/ RMII_RXD0	IRQ4-DS	
G10	VCC						
H1	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ MOSIB		
H2		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/ USB0_DPRPD		ADTRG0#
H3		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT	TXD1/RXD3/ SMOSI1/SMISO3/ SSDA1/SSCL3/ MOSIA/SCL2-DS/ IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Table 4.1 List of I/O Registers (Address Order) (16/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 814Ch	TPU3	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Eh	TPU3	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 8150h	TPU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8151h	TPU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8152h	TPU4	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8154h	TPU4	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8155h	TPU4	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8156h	TPU4	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8158h	TPU4	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 815Ah	TPU4	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8160h	TPU5	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8161h	TPU5	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8162h	TPU5	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8164h	TPU5	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8165h	TPU5	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8166h	TPU5	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8168h	TPU5	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 816Ah	TPU5	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8170h	TPUB	Timer start register	TSTR	8	8	2, 3 PCLKB	2 ICLK	
0008 8171h	TPUB	Timer synchronous register	TSYR	8	8	2, 3 PCLKB	2 ICLK	
0008 8178h	TPU6	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8179h	TPU7	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 817Ah	TPU8	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 817Bh	TPU9	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 817Ch	TPU10	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 817Dh	TPU11	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8180h	TPU6	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8181h	TPU6	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8182h	TPU6	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8183h	TPU6	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8184h	TPU6	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8185h	TPU6	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8186h	TPU6	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8188h	TPU6	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 818Ah	TPU6	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 818Ch	TPU6	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 818Eh	TPU6	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 8190h	TPU7	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8191h	TPU7	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8192h	TPU7	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8194h	TPU7	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8195h	TPU7	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8196h	TPU7	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8198h	TPU7	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 819Ah	TPU7	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81A0h	TPU8	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81A1h	TPU8	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81A2h	TPU8	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81A4h	TPU8	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81A5h	TPU8	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81A6h	TPU8	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (18/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 8200h	TMR0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8201h	TMR1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8202h	TMR0	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8203h	TMR1	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8204h	TMR0	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	
0008 8205h	TMR1	Time constant register A	TCORA	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8206h	TMR0	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	
0008 8207h	TMR1	Time constant register B	TCORB	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8208h	TMR0	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 8209h	TMR1	Timer counter	TCNT	8	8*5	2, 3 PCLKB	2 ICLK	
0008 820Ah	TMR0	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK	
0008 820Bh	TMR1	Timer counter control register	TCCR	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8210h	TMR2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8211h	TMR3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8212h	TMR2	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8213h	TMR3	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8214h	TMR2	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	
0008 8215h	TMR3	Time constant register A	TCORA	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8216h	TMR2	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	
0008 8217h	TMR3	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	
0008 8218h	TMR2	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 8219h	TMR3	Timer counter	TCNT	8	8*5	2, 3 PCLKB	2 ICLK	
0008 821Ah	TMR2	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK	
0008 821Bh	TMR3	Timer counter control register	TCCR	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8280h	CRC	CRC control register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK	
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8300h	RIIC0	I^2C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIIC
0008 8301h	RIIC0	I^2C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8302h	RIIC0	I^2C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8303h	RIIC0	I^2C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8304h	RIIC0	I^2C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8305h	RIIC0	I^2C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8306h	RIIC0	I^2C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8307h	RIIC0	I^2C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8308h	RIIC0	I^2C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8309h	RIIC0	I^2C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ah	RIIC0	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ah	RIIC0	Timeout Internal Counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK	
0008 830Bh	RIIC0	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 830Bh	RIIC0	Timeout Internal Counter U	TMOCNTU	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ch	RIIC0	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8310h	RIIC0	I^2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8311h	RIIC0	I^2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8312h	RIIC0	I^2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (21/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 83BAh	RSPI1	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	RSPI
0008 83BCh	RSPI1	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 83BEh	RSPI1	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 83C0h	RSPI2	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C1h	RSPI2	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 83C2h	RSPI2	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C3h	RSPI2	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C4h	RSPI2	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 83C8h	RSPI2	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C9h	RSPI2	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83CAh	RSPI2	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 83CBh	RSPI2	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83CCh	RSPI2	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 83CDh	RSPI2	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 83CEh	RSPI2	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 83CFh	RSPI2	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 83D0h	RSPI2	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 83D2h	RSPI2	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 83D4h	RSPI2	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 83D6h	RSPI2	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 83D8h	RSPI2	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	
0008 83DAh	RSPI2	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	
0008 83DCh	RSPI2	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 83DEh	RSPI2	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 8600h	MTU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	MTU2a
0008 8601h	MTU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8602h	MTU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8603h	MTU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8604h	MTU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8605h	MTU3	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8606h	MTU4	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8607h	MTU4	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8608h	MTU3	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8609h	MTU4	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 860Ah	MTU	Timer output master enable register	TOER	8	8	2, 3 PCLKB	2 ICLK	
0008 860Dh	MTU	Timer gate control register	TGCR	8	8	2, 3 PCLKB	2 ICLK	
0008 860Eh	MTU	Timer output control register 1	TOCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 860Fh	MTU	Timer output control register 2	TOCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8610h	MTU3	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8612h	MTU4	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8614h	MTU	Timer cycle data register	TCDR	16	16	2, 3 PCLKB	2 ICLK	
0008 8616h	MTU	Timer dead time data register	TDDR	16	16	2, 3 PCLKB	2 ICLK	
0008 8618h	MTU3	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 861Ah	MTU3	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 861Ch	MTU4	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 861Eh	MTU4	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8620h	MTU	Timer subcounter	TCNTS	16	16	2, 3 PCLKB	2 ICLK	
0008 8622h	MTU	Timer cycle buffer register	TCBR	16	16	2, 3 PCLKB	2 ICLK	
0008 8624h	MTU3	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 8626h	MTU3	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 8628h	MTU4	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (28/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 A806h	IEB	IEBus slave address setting register 2	IESA2	8	8	3 to 4 PCLKB	2, 3 ICLK	IEB
0008 A807h	IEB	IEBus transmit message length register	IETBFL	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A809h	IEB	IEBus reception master address register 1	IEMA1	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A80Ah	IEB	IEBus reception master address register 2	IEMA2	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A80Bh	IEB	IEBus receive control field register	IERCTL	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A80Ch	IEB	IEBus receive message length register	IERBFL	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A80Eh	IEB	IEBus lock address register 1	IELA1	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A80Fh	IEB	IEBus lock address register 2	IELA2	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A810h	IEB	IEBus general flag register	IEFLG	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A811h	IEB	IEBus transmit status register	IETSR	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A812h	IEB	IEBus transmit interrupt enable register	IEIET	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A814h	IEB	IEBus receive status register	IERSR	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A815h	IEB	IEBus receive interrupt enable register	IEIER	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A818h	IEB	IEBus clock select register	IECKSR	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A900h to 0008 A91Fh	IEB	IEBus transmit data buffer register 001 to 032	IETB001 to 032	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 AA00h to 0008 AA1Fh	IEB	IEBus receive data buffer register 001 to 032	IERB001 to 032	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 B300h	SCI12	Serial mode register	SMR12	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId
0008 B301h	SCI12	Bit rate register	BRR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B302h	SCI12	Serial control register	SCR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B303h	SCI12	Transmit data register	TDR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B304h	SCI12	Serial status register	SSR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B305h	SCI12	Receive data register	RDR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B306h	SCI12	Smart card mode register	SCMR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B307h	SCI12	Serial extended mode register	SEMR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B308h	SCI12	Noise filter setting register	SNFR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B309h	SCI12	I^2C mode register 1	SIMR112	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Ah	SCI12	I^2C mode register 2	SIMR212	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Bh	SCI12	I^2C mode register 3	SIMR312	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Ch	SCI12	I^2C status register	SISR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Dh	SCI12	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 B320h	SCI12	Extended serial module enable register	ESMER	8	8	2, 3 PCLKB	2 ICLK	
0008 B321h	SCI12	Control register 0	CR0	8	8	2, 3 PCLKB	2 ICLK	
0008 B322h	SCI12	Control register 1	CR1	8	8	2, 3 PCLKB	2 ICLK	
0008 B323h	SCI12	Control register 2	CR2	8	8	2, 3 PCLKB	2 ICLK	
0008 B324h	SCI12	Control register 3	CR3	8	8	2, 3 PCLKB	2 ICLK	
0008 B325h	SCI12	Port control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 B326h	SCI12	Interrupt control register	ICR	8	8	2, 3 PCLKB	2 ICLK	
0008 B327h	SCI12	Status register	STR	8	8	2, 3 PCLKB	2 ICLK	
0008 B328h	SCI12	Status clear register	STCR	8	8	2, 3 PCLKB	2 ICLK	
0008 B329h	SCI12	Control field 0 data register	CF0DR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Ah	SCI12	Control field 0 compare enable register	CF0CR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Bh	SCI12	Control field 0 receive data register	CF0RR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId
0008 B32Ch	SCI12	Primary control field 1 data register	PCF1DR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Dh	SCI12	Secondary control field 1 data register	SCF1DR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Eh	SCI12	Control field 1 compare enable register	CF1CR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Fh	SCI12	Control field 1 receive data register	CF1RR	8	8	2, 3 PCLKB	2 ICLK	
0008 B330h	SCI12	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 B331h	SCI12	Timer mode register	TMR	8	8	2, 3 PCLKB	2 ICLK	
0008 B332h	SCI12	Timer prescaler register	TPRE	8	8	2, 3 PCLKB	2 ICLK	
0008 B333h	SCI12	Timer count register	TCNT	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (38/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 0000h	USB0	System configuration control register	SYSCFG	16	16	3 to 4 PCLKB	2, 3 ICLK	USBa
000A 0004h	USB0	System configuration status register 0	SYSSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0008h	USB0	Device state control register 0	DVSTCTR0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0014h	USB0	CFIFO port register	CFIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 0018h	USB0	D0FIFO port register	D0FIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 001Ch	USB0	D1FIFO port register	D1FIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 0020h	USB0	CFIFO port select register	CFIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0022h	USB0	CFIFO port control register	CFIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0028h	USB0	D0FIFO port select register	D0FIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 002Ah	USB0	D0FIFO port control register	D0FIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 002Ch	USB0	D1FIFO port select register	D1FIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 002Eh	USB0	D1FIFO port control register	D1FIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0030h	USB0	Interrupt enable register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0032h	USB0	Interrupt enable register 1	INTENB1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0036h	USB0	BRDY interrupt enable register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0038h	USB0	NRDY interrupt enable register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	

Table 4.1 List of I/O Registers (Address Order) (42/50)

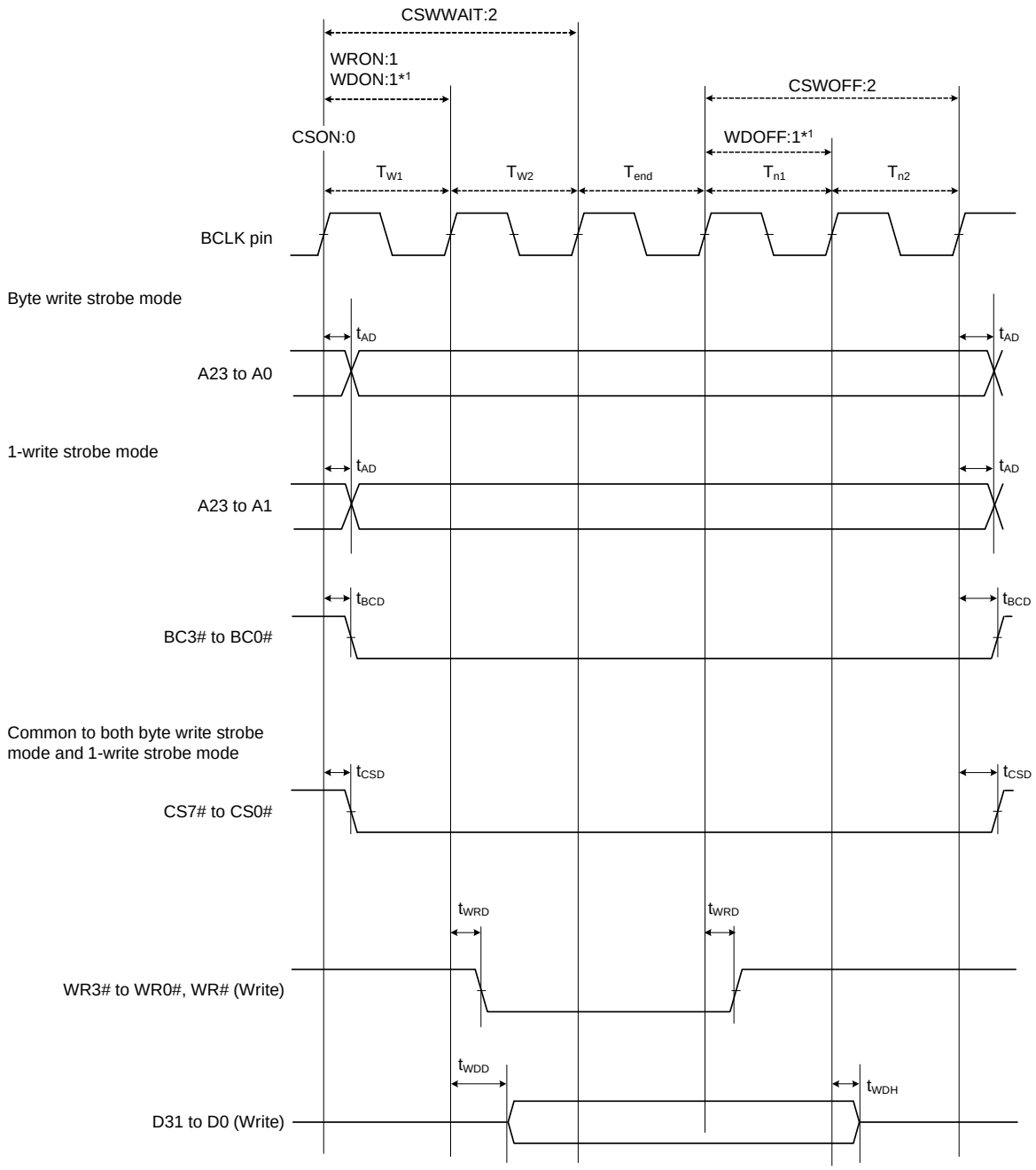
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 0090h	USB0	Pipe 1 transaction counter enable register	PIPE1TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0092h	USB0	Pipe 1 transaction counter register	PIPE1TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0094h	USB0	Pipe 2 transaction counter enable register	PIPE2TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0096h	USB0	Pipe 2 transaction counter register	PIPE2TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	USBa
000A 0098h	USB0	Pipe 3 transaction counter enable register	PIPE3TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 009Ah	USB0	Pipe 3 transaction counter register	PIPE3TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 009Ch	USB0	Pipe 4 transaction counter enable register	PIPE4TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 009Eh	USB0	Pipe 4 transaction counter register	PIPE4TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 00A0h	USB0	Pipe 5 transaction counter enable register	PIPE5TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 00A2h	USB0	Pipe 5 transaction counter register	PIPE5TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	

Table 4.1 List of I/O Registers (Address Order) (47/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 027Eh	USB1	Pipe 8 control register	PIPE8CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0280h	USB1	Pipe 9 control register	PIPE9CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	USBa
000A 0290h	USB1	Pipe 1 transaction counter enable register	PIPE1TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0292h	USB1	Pipe 1 transaction counter register	PIPE1TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0294h	USB1	Pipe 2 transaction counter enable register	PIPE2TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0296h	USB1	Pipe 2 transaction counter register	PIPE2TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0298h	USB1	Pipe 3 transaction counter enable register	PIPE3TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 029Ah	USB1	Pipe 3 transaction counter register	PIPE3TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 029Ch	USB1	Pipe 4 transaction counter enable register	PIPE4TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 029Eh	USB1	Pipe 4 transaction counter register	PIPE4TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	USBa

Table 4.1 List of I/O Registers (Address Order) (49/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000C 0100h	ETHERC	ETHERC mode register	ECMR	32	32	5, 6 PCLKA	—	ETHERC
000C 0108h	ETHERC	Receive frame length register	RFLR	32	32	5, 6 PCLKA	—	
000C 0110h	ETHERC	ETHERC status register	ECSR	32	32	5, 6 PCLKA	—	
000C 0118h	ETHERC	ETHERC interrupt permission register	ECSIPR	32	32	5, 6 PCLKA	—	
000C 0120h	ETHERC	PHY interface register	PIR	32	32	5, 6 PCLKA	—	
000C 0128h	ETHERC	PHY status register	PSR	32	32	5, 6 PCLKA	—	
000C 0140h	ETHERC	Random number generation counter upper limit setting register	RDMLR	32	32	5, 6 PCLKA	—	
000C 0150h	ETHERC	IPG register	IPGR	32	32	5, 6 PCLKA	—	
000C 0154h	ETHERC	Automatic PAUSE frame register	APR	32	32	5, 6 PCLKA	—	
000C 0158h	ETHERC	Manual PAUSE frame register	MPR	32	32	5, 6 PCLKA	—	
000C 0160h	ETHERC	PAUSE Frame receive counter register	RFCF	32	32	5, 6 PCLKA	—	
000C 0164h	ETHERC	Automatic PAUSE frame retransmit count register	TPAUSER	32	32	5, 6 PCLKA	—	
000C 0168h	ETHERC	PAUSE frame retransmit counter register	TPAUSECR	32	32	5, 6 PCLKA	—	
000C 016Ch	ETHERC	Broadcast frame receive count setting register	BCFRR	32	32	5, 6 PCLKA	—	
000C 01C0h	ETHERC	MAC address high register	MAHR	32	32	5, 6 PCLKA	—	
000C 01C8h	ETHERC	MAC address low register	MALR	32	32	5, 6 PCLKA	—	
000C 01D0h	ETHERC	Transmit retry over counter register	TROCR	32	32	5, 6 PCLKA	—	
000C 01D4h	ETHERC	Delayed collision detect counter register	CDCR	32	32	5, 6 PCLKA	—	
000C 01D8h	ETHERC	Lost carrier counter register	LCCR	32	32	5, 6 PCLKA	—	
000C 01DCh	ETHERC	Carrier not detect counter register	CNDCR	32	32	5, 6 PCLKA	—	
000C 01E4h	ETHERC	CRC error frame receive counter register	CEFCR	32	32	5, 6 PCLKA	—	
000C 01E8h	ETHERC	Frame receive error counter register	FRECR	32	32	5, 6 PCLKA	—	
000C 01ECh	ETHERC	Too-short frame receive counter register	TSFRCR	32	32	5, 6 PCLKA	—	
000C 01F0h	ETHERC	Too-long frame receive counter register	TLFRCR	32	32	5, 6 PCLKA	—	
000C 01F4h	ETHERC	Residual-bit frame receive counter register	RFCR	32	32	5, 6 PCLKA	—	
000C 01F8h	ETHERC	Multicast address frame receive counter register	MAFCR	32	32	5, 6 PCLKA	—	



Note1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.20 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

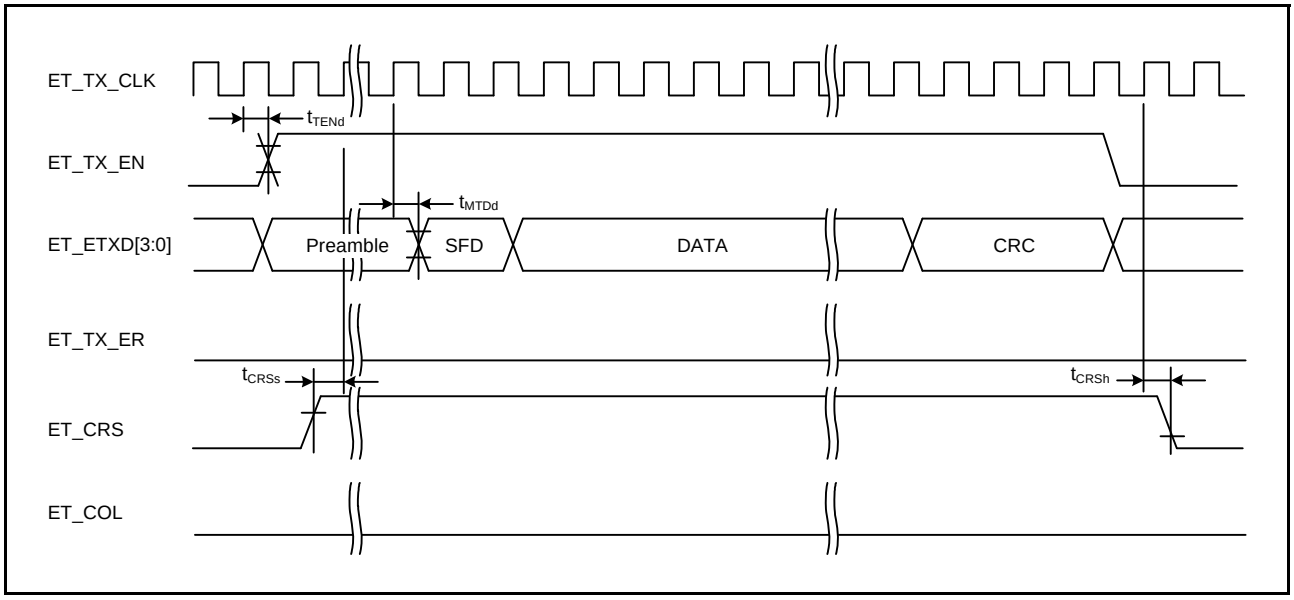


Figure 5.53 MII Transmission Timing (Normal Operation)

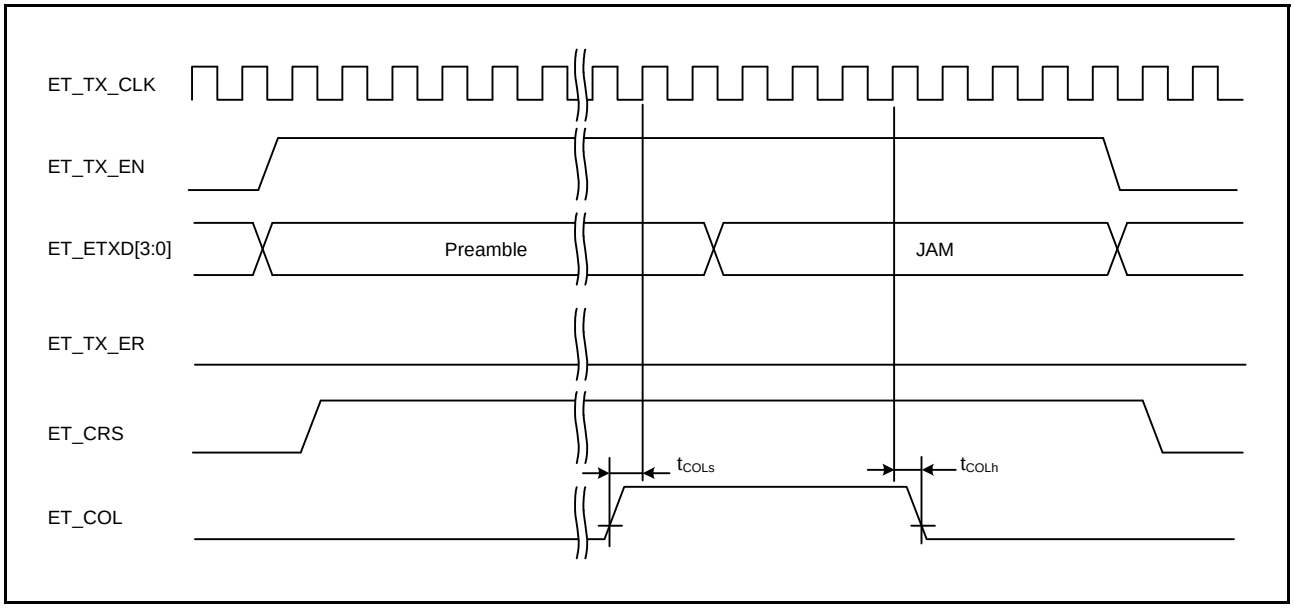


Figure 5.54 MII Transmission Timing (Conflict Occurrence)

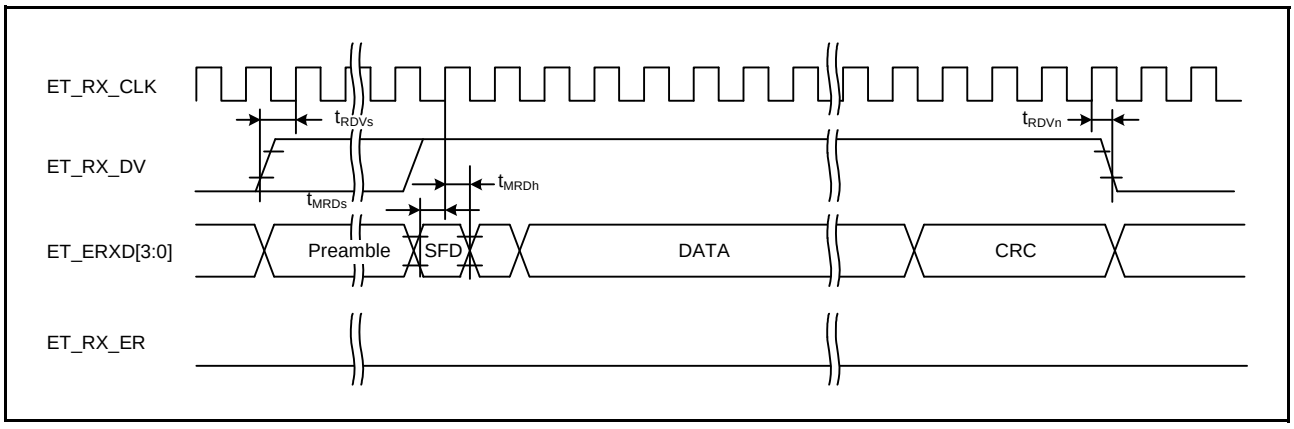


Figure 5.55 MII Reception Timing (Normal Operation)

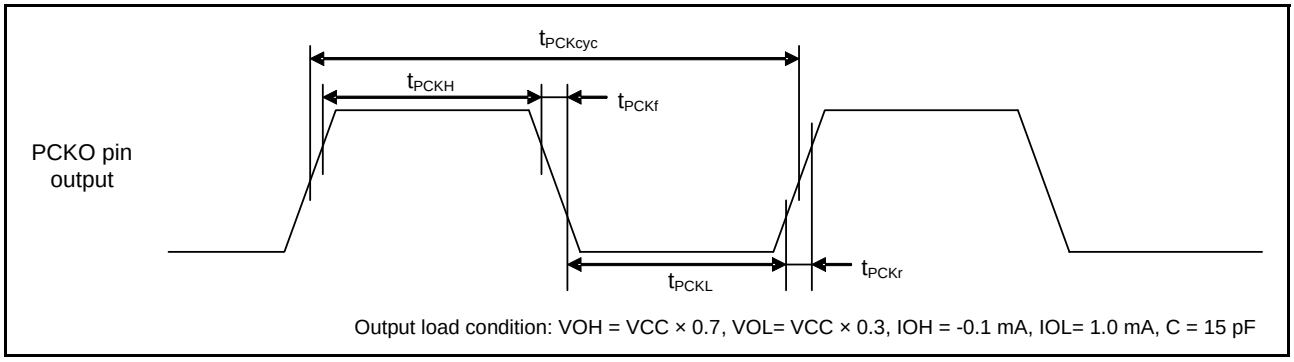


Figure 5.60 PDC Output Clock Characteristic

5.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.33 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled	V_{POR}	2.5	2.6	2.7	V	Figure 5.63
		Low power consumption function enabled		2.0	2.35	2.7		
	Voltage detection circuit (LVD0)		V_{det0}	2.7	2.80	2.9		Figure 5.64
	Voltage detection circuit (LVD1)		V_{det1_A}	2.75	2.95	3.15		Figure 5.65
	Voltage detection circuit (LVD2)		V_{det2_A}	2.75	2.95	3.15		Figure 5.66
Internal reset time	Power-on reset time		t_{POR}	—	4.6	—	ms	Figure 5.63
	LVD0 reset time		t_{LVD0}	—	4.6	—		Figure 5.64
	LVD1 reset time		t_{LVD1}	—	0.9	—		Figure 5.65
	LVD2 reset time		t_{LVD2}	—	0.9	—		Figure 5.66
Minimum VCC down time			t_{VOFF}	200	—	—	µs	Figure 5.63 and Figure 5.64
Response delay time			t_{det}	—	—	200	µs	Figure 5.63 to Figure 5.66
LVD operation stabilization time (after LVD is enabled)			$Td_{(E-A)}$	—	—	3	µs	Figure 5.65 and Figure 5.66
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	80	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.

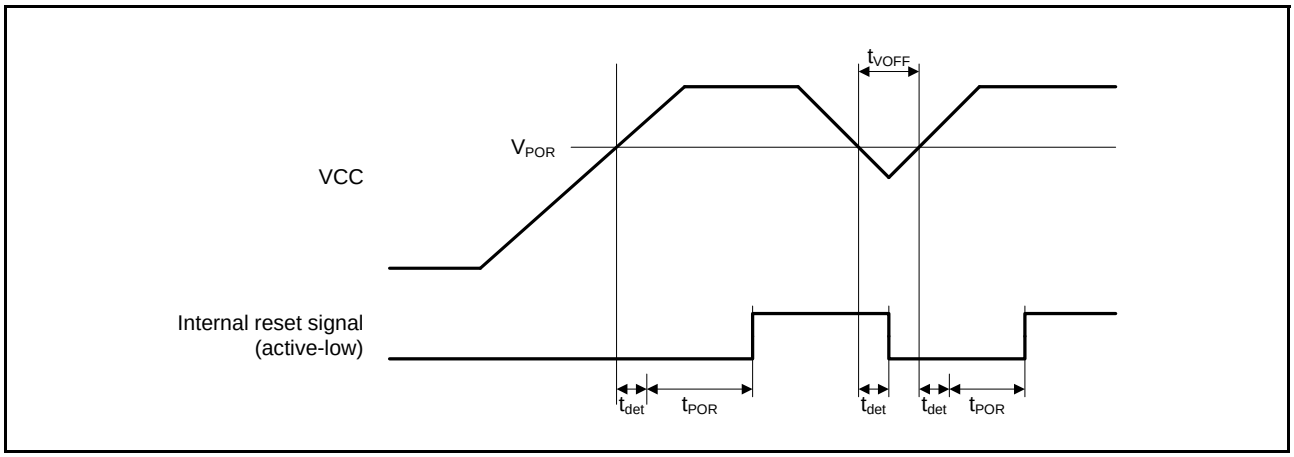
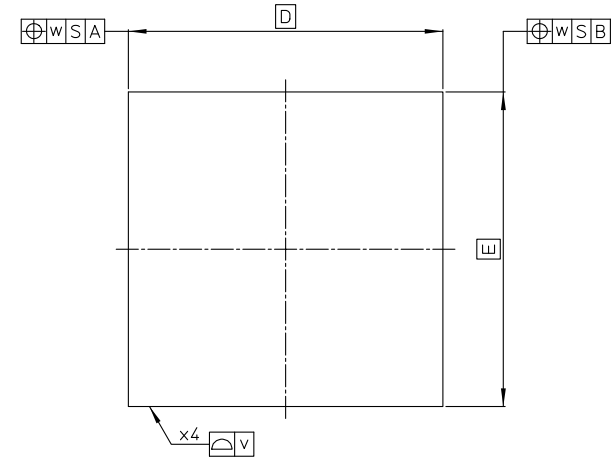
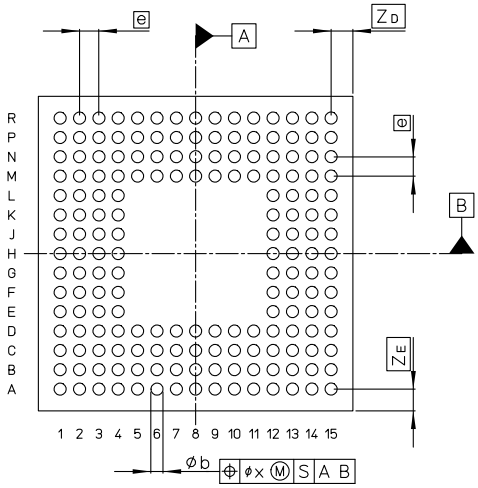


Figure 5.63 Power-on Reset Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g





Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

Figure B 176-pin LFBGA (PLBG0176GA-A)