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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56317sdfb-v0

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
C14	VSS						
C15	SDCLK	P70					
D1		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019
D2		P02		TMCI1	SCK6	IRQ10	AN020
D3		P03				IRQ11	DA0
D4		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
D5		P44				IRQ12-DS	AN004
D6		P93	A19/D19		CTS7#/RTS7#/SS7#		AN017
D7		P95	A21/D21				
D8	VSS						
D9		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
D10		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
D11		P61	CS1#/SDCS#				
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	ET_RX_CLK/REF50CK/ RSPCKB	IRQ5	AN3
D13	VCC						
D14		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
D15		P65	CS5#/CKE				
E1		PJ5					
E2	EMLE						
E3		PF5				IRQ4	
E4	VSS						
E5*1	NC						
E12		PE6	D14[A14/D14]	TIOCA11	MOSIB	IRQ6	AN4
E13	TRDATA0	PG2	D26				
E14	TRDATA1	PG3	D27				
E15		P67	CS7#/DQM1		CRX2*3	IRQ15	
F1	VBATT						
F2	VCL						
F3		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
F4	BSCANP						
F12		P66	CS6#/DQM0		CTX2*3		
F13	TRSYNC	PG4	D28				
F14		PA0	A0/BC0#/DQM2	MTIOC4A/TIOCA0/PO16	ET_TX_EN/ RMII_TXD_EN/SSLA1		
F15	VSS						
G1	XCIN						
G2	XCOUT						
G3	MD/FINED						
G4	TRST#	PF4					
G12	TRCLK	PG5	D29				
G13	TRDATA2	PG6	D30				
G14		PA1	A1/DQM3	MTIOC0B/MTCLKC/ TIOCB0/PO17	ET_WOL/SCK5/SSLA2	IRQ11	
G15	VCC						
H1	XTAL	P37					
H2	VSS						

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
M2		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3# SMOSI1/SS3#/SSDA1/ MOSIB		
M3		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/USB0_VBUSEN/ PIXCLK		
M4		P86		TIOCA0	PIXD1		
M5		P13		MTIOC0B/TIOCA5/TMO3/ PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
M6		P56	WR2#/BC2#/ EDACK1	MTIOC3C/TIOCA1			
M7		P54	ALE/EDACK0	MTIOC4B/TMCI1	ET_LINKSTA/CTS2#/ RTS2#/SS2#/CTX1		
M8		P53*2	BCLK				
M9		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
M10		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	ET_ETXD2/SCK8/ RSPCKA		
M11		P81	EDACK0	MTIOC3D/PO27	ET_ETXD0/RMII_TXD0/ RXD10/SMISO10/SSCL10		
M12		P77	CS7#	PO23	ET_RX_ER/RMII_RX_ER/ TXD11/SMOSI11/SSDA11		
M13		PB7	A15	MTIOC3B/TIOCB5/PO31	ET_CRS/RMII_CRS_DV/ TXD9/SMOSI9/SSDA9		
M14		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	ET_ETXD0/RMII_TXD0/ SCK9		
M15		PB4	A12	TIOCA4/PO28	ET_TX_EN/ RMII_TXD_EN/CTS9#/ RTS9#/SS9#		
N1	VCC						
N2		P23	EDACK0	MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7		
N3		P22	EDREQ0	MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0/USB0_DRPD/ PIXD6		
N4		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ USB1_DPUPE/PIXD0	IRQ5	
N5		P12		MTIC5U/TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
N6		P57	WAIT#/WR3#/ BC3#/EDREQ1				
N7		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	ET_EXOUT/CRX1	IRQ10	
N8	VCC_USB						
N9		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
N10		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	ET_COL/TXD8/SMOSI8/ SSDA8/MISOA	IRQ14	
N11		P82	EDREQ1	MTIOC4A/PO28	ET_ETXD1/RMII_TXD1/ TXD10/SMOSI10/SSDA10		
N12		PC3	A19	MTIOC4D/TCLKB/PO24	ET_TX_ER/TXD5/ SMOSI5/SSDA5/IETXD		
N13		PC0	A16	MTIOC3C/TCLKC/PO17	ET_ERXD3/CTS5#/ RTS5#/SS5#/SSLA1/ SCL3	IRQ14	
N14		P73	CS3#	PO16	ET_WOL		
N15	VSS						

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (1/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
A1	AVSS0						
A2		P07				IRQ15	ADTRG0#
A3		P40				IRQ8-DS	AN000
A4		P42				IRQ10-DS	AN002
A5		P45				IRQ13-DS	AN005
A6		P90	A16		TXD7/SMOSI7/SSDA7		AN014
A7		P92	A18		RXD7/SMISO7/SSCL7		AN016
A8		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
A9		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
A10	VSS						
A11		P62	CS2#/RAS#				
A12		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/ PO18	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB		ANEX1
A13		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/ PO26/POE8#	CTS12#/RTS12#/SS12#/ MISOB/ET_ERXD3		AN1
B1	VREFH						
B2	AVCC0						
B3		P05				IRQ13	DA1
B4	VREFL0						
B5		P43				IRQ11-DS	AN003
B6		P47				IRQ15-DS	AN007
B7		P91	A17		SCK7		AN015
B8		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
B9		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
B10	VCC						
B11		P61	CS1#/SDCS#				
B12		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/ PO23	RXD12/SMISO12/SSCL12/ RXDX12/SSLB3/MOSIB	IRQ7-DS	AN0
B13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0/ET_ERXD2		AN2
C1	VREFL						
C2		P02		TMCI1	SCK6	IRQ10	AN020
C3	VREFH0						
C4		P41				IRQ9-DS	AN001
C5		P46				IRQ14-DS	AN006
C6	VSS						
C7		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
C8		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
C9		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
C10		P63	CS3#/CAS#				
C11		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
C12	SDCLK	P70					
C13	VSS						
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
D2		PF5				IRQ4	
D3		P03				IRQ11	DA0
D4		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (2/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
D5	VCC						
D6		P93	A19		CTS7#/RTS7#/SS7#		AN017
D7		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
D8		P60	CS0#				
D9		P64	CS4#/WE#				
D10		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
D11	VCC						
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	RSPCKB/ET_RX_CLK/ REF50CK	IRQ5	AN3
D13		PE6	D14[A14/D14]	TIOCA11	MOSIB	IRQ6	AN4
E1	VSS						
E2	VCL						
E3		PJ5					
E4	EMLE						
E5		P44				IRQ12-DS	AN004
E10		PA0	A0/BC0#	MTIOC4A/TIOCA0/ PO16	SSLA1/ET_TX_EN/ RMII_TXD_EN		
E11		P66	CS6#/DQM0		CTX2*2		
E12		P65	CS5#/CKE				
E13		P67	CS7#/DQM1		CRX2*2	IRQ15	
F1	XCIN						
F2	XCOUT						
F3		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
F4	VBATT						
F10		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/SSCL5/ ET_MDIO	IRQ6-DS	
F11	VSS						
F12		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2/ET_WOL	IRQ11	
F13		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
G1	XTAL	P37					
G2	RES#						
G3	MD/FINED						
G4	BSCANP						
G10		PA5	A5	TIOCB1/PO21	RSPCKA/ET_LINKSTA		
G11		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	CTS5#/RTS5#/SS5# MOSIA/ET_EXOUT		
G12	VCC						
G13		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0/ET_MDC	IRQ5-DS	
H1	EXTAL	P36					
H2	VCC						
H3	VSS						
H4		P35				NMI	
H10		P72	CS2#		ET_MDC		
H11		P71	CS1#		ET_MDIO		

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP).
The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

Table 4.1 List of I/O Registers (Address Order) (26/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 A0A6h	SCI5	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId
0008 A0A7h	SCI5	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A8h	SCI5	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A9h	SCI5	I2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A0AAh	SCI5	I2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ABh	SCI5	I2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ACh	SCI5	I2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ADh	SCI5	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C0h	SCI6	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C1h	SCI6	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C2h	SCI6	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C3h	SCI6	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C4h	SCI6	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C5h	SCI6	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C6h	SCI6	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C7h	SCI6	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C8h	SCI6	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C9h	SCI6	I2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CAh	SCI6	I2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CBh	SCI6	I2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CCh	SCI6	I2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CDh	SCI6	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E0h	SCI7	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E1h	SCI7	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E2h	SCI7	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E3h	SCI7	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E4h	SCI7	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E5h	SCI7	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E6h	SCI7	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E7h	SCI7	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E8h	SCI7	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E9h	SCI7	I2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A0EAh	SCI7	I2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A0EBh	SCI7	I2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ECh	SCI7	I2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0EDh	SCI7	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A100h	SCI8	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A101h	SCI8	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A102h	SCI8	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A103h	SCI8	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A104h	SCI8	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A105h	SCI8	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A106h	SCI8	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A107h	SCI8	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A109h	SCI8	I2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A10Ah	SCI8	I2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A10Bh	SCI8	I2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A10Ch	SCI8	I2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (28/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 A806h	IEB	IEBus slave address setting register 2	IESA2	8	8	3 to 4 PCLKB	2, 3 ICLK	IEB
0008 A807h	IEB	IEBus transmit message length register	IETBFL	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A809h	IEB	IEBus reception master address register 1	IEMA1	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A80Ah	IEB	IEBus reception master address register 2	IEMA2	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A80Bh	IEB	IEBus receive control field register	IERCTL	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A80Ch	IEB	IEBus receive message length register	IERBFL	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A80Eh	IEB	IEBus lock address register 1	IELA1	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A80Fh	IEB	IEBus lock address register 2	IELA2	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A810h	IEB	IEBus general flag register	IEFLG	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A811h	IEB	IEBus transmit status register	IETSR	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A812h	IEB	IEBus transmit interrupt enable register	IEIET	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A814h	IEB	IEBus receive status register	IERSR	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A815h	IEB	IEBus receive interrupt enable register	IEIER	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A818h	IEB	IEBus clock select register	IECKSR	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A900h to 0008 A91Fh	IEB	IEBus transmit data buffer register 001 to 032	IETB001 to 032	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 AA00h to 0008 AA1Fh	IEB	IEBus receive data buffer register 001 to 032	IERB001 to 032	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 B300h	SCI12	Serial mode register	SMR12	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId
0008 B301h	SCI12	Bit rate register	BRR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B302h	SCI12	Serial control register	SCR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B303h	SCI12	Transmit data register	TDR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B304h	SCI12	Serial status register	SSR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B305h	SCI12	Receive data register	RDR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B306h	SCI12	Smart card mode register	SCMR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B307h	SCI12	Serial extended mode register	SEMR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B308h	SCI12	Noise filter setting register	SNFR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B309h	SCI12	I^2C mode register 1	SIMR112	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Ah	SCI12	I^2C mode register 2	SIMR212	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Bh	SCI12	I^2C mode register 3	SIMR312	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Ch	SCI12	I^2C status register	SISR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Dh	SCI12	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 B320h	SCI12	Extended serial module enable register	ESMER	8	8	2, 3 PCLKB	2 ICLK	
0008 B321h	SCI12	Control register 0	CR0	8	8	2, 3 PCLKB	2 ICLK	
0008 B322h	SCI12	Control register 1	CR1	8	8	2, 3 PCLKB	2 ICLK	
0008 B323h	SCI12	Control register 2	CR2	8	8	2, 3 PCLKB	2 ICLK	
0008 B324h	SCI12	Control register 3	CR3	8	8	2, 3 PCLKB	2 ICLK	
0008 B325h	SCI12	Port control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 B326h	SCI12	Interrupt control register	ICR	8	8	2, 3 PCLKB	2 ICLK	
0008 B327h	SCI12	Status register	STR	8	8	2, 3 PCLKB	2 ICLK	
0008 B328h	SCI12	Status clear register	STCR	8	8	2, 3 PCLKB	2 ICLK	
0008 B329h	SCI12	Control field 0 data register	CF0DR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Ah	SCI12	Control field 0 compare enable register	CF0CR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Bh	SCI12	Control field 0 receive data register	CF0RR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId
0008 B32Ch	SCI12	Primary control field 1 data register	PCF1DR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Dh	SCI12	Secondary control field 1 data register	SCF1DR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Eh	SCI12	Control field 1 compare enable register	CF1CR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Fh	SCI12	Control field 1 receive data register	CF1RR	8	8	2, 3 PCLKB	2 ICLK	
0008 B330h	SCI12	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 B331h	SCI12	Timer mode register	TMR	8	8	2, 3 PCLKB	2 ICLK	
0008 B332h	SCI12	Timer prescaler register	TPRE	8	8	2, 3 PCLKB	2 ICLK	
0008 B333h	SCI12	Timer count register	TCNT	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (36/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C456h	RTC	Hour capture register 0	RHRCP0	8	8	2, 3 PCLKB	2 ICLK	RTCa
0008 C45Ah	RTC	Date capture register 0	RDAYCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C45Ch	RTC	Month capture register 0	RMONCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C462h	RTC	Second capture register 1	RSECCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C464h	RTC	Minute capture register 1	RMINCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C466h	RTC	Hour capture register 1	RHRCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C46Ah	RTC	Date capture register 1	RDAYCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C46Ch	RTC	Month capture register 1	RMONCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C472h	RTC	Second capture register 2	RSECCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C474h	RTC	Minute capture register 2	RMINCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C476h	RTC	Hour capture register 2	RHRCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C47Ah	RTC	Date capture register 2	RDAYCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C47Ch	RTC	Month capture register 2	RMONCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C500h	TEMPS	Temperature sensor control register	TSCR	8	8	2, 3 PCLKB	2 ICLK	Temperature Sensor
0008 C880h	SYSTEM	Counter-clock extension register 1	SCK1	8	8	2, 3 PCLKB	2 ICLK	MCK
0008 C890h	SYSTEM	Counter-clock extension register 2	SCK2	8	8	2, 3 PCLKB	2 ICLK	
0009 0200h to 0009 03FFh	CAN0	Mailbox registers 0 to 31	MB0 to 31	128	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 0400h to 0009 041Fh	CAN0	Mask registerer 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0420h	CAN0	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0424h	CAN0	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0428h	CAN0	Mask invalid register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 042Ch	CAN0	Mailbox interrupt enable register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0820h to 0009 083Fh	CAN0	Message control registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	
0009 0840h	CAN0	Control register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 0842h	CAN0	Status register	STR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 0844h	CAN0	Bit configuration register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0848h	CAN0	Receive FIFO control register	RFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 0849h	CAN0	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Ah	CAN0	Transmit FIFO control register	TFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Bh	CAN0	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Ch	CAN0	Error interrupt enable register	EIER	8	8	2, 3 PCLKB	2 ICLK	
0009 084Dh	CAN0	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Eh	CAN0	Receive error count register	RECR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Fh	CAN0	Transmit error count register	TECR	8	8	2, 3 PCLKB	2 ICLK	
0009 0850h	CAN0	Error code store register	ECSR	8	8	2, 3 PCLKB	2 ICLK	
0009 0851h	CAN0	Channel search support register	CSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 0852h	CAN0	Mailbox search status register	MSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 0853h	CAN0	Mailbox search mode register	MSMR	8	8	2, 3 PCLKB	2 ICLK	
0009 0854h	CAN0	Time stamp register	TSR	16	16	2, 3 PCLKB	2 ICLK	
0009 0856h	CAN0	Acceptance filter support register	AFSR	16	16	2, 3 PCLKB	2 ICLK	
0009 0858h	CAN0	Test control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0009 1200h to 0009 13FFh	CAN1	Mailbox registers 0 to 31	MB0 to 31	128	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1400h to 0009 141Fh	CAN1	Mask register 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1420h	CAN1	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1424h	CAN1	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (38/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 0000h	USB0	System configuration control register	SYSCFG	16	16	3 to 4 PCLKB	2, 3 ICLK	USBa
000A 0004h	USB0	System configuration status register 0	SYSSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0008h	USB0	Device state control register 0	DVSTCTR0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0014h	USB0	CFIFO port register	CFIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 0018h	USB0	D0FIFO port register	D0FIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 001Ch	USB0	D1FIFO port register	D1FIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 0020h	USB0	CFIFO port select register	CFIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0022h	USB0	CFIFO port control register	CFIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0028h	USB0	D0FIFO port select register	D0FIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 002Ah	USB0	D0FIFO port control register	D0FIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 002Ch	USB0	D1FIFO port select register	D1FIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 002Eh	USB0	D1FIFO port control register	D1FIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0030h	USB0	Interrupt enable register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0032h	USB0	Interrupt enable register 1	INTENB1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0036h	USB0	BRDY interrupt enable register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0038h	USB0	NRDY interrupt enable register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	

Table 4.1 List of I/O Registers (Address Order) (41/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 006Eh	USB0	Pipe cycle control register	PIPEPERI	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0070h	USB0	Pipe 1 control register	PIPE1CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0072h	USB0	Pipe 2 control register	PIPE2CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0074h	USB0	Pipe 3 control register	PIPE3CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0076h	USB0	Pipe 4 control register	PIPE4CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0078h	USB0	Pipe 5 control register	PIPE5CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	USBa
000A 007Ah	USB0	Pipe 6 control register	PIPE6CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 007Ch	USB0	Pipe 7 control register	PIPE7CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 007Eh	USB0	Pipe 8 control register	PIPE8CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0080h	USB0	Pipe 9 control register	PIPE9CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	

Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Max.*2		I_{CC}*3	—	—	100	mA	ICLK = 100 MHz PCLKA = 100MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 100MHz
		Normal *4	Peripheral function: clock signal supplied*4		—	52	—		
			Peripheral function: clock signal stopped*4		—	40	—		
		Sleep mode			—	25	65		
		All-module-clock-stop mode (reference value)			—	20	38		
		Increased by BGO operation*5			—	15	—		
	Low-speed operating mode 1*6				—	4	—		ICLK = 1 MHz
	Low-speed operating mode 2				—	1	—		ICLK = 32.768 kHz
	Software standby mode				—	0.2	6		
	Deep software standby mode	Power supplied to RAM and USB resume detecting unit			—	22	200	μA	
		Power not supplied to RAM and USB resume detecting unit	Power-on reset circuit and low-power consumption function disabled		—	21	60		
			Power-on reset circuit and low-power		—	6.2	28		
	Increase when the RTC is operating		When a crystal oscillator for low clock loads is in use		—	1.0	—		
			When a crystal oscillator for standard clock loads is in use		—	3.0	—		
	RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)		When a crystal oscillator for low clock loads is in use		—	0.9	—		V_{BATT} = 2.0 V, VCC = 0V
					—	1.6	—		V_{BATT} = 3.3 V, VCC = 0V
			When a crystal oscillator for standard clock loads is in use		—	1.7	—		V_{BATT} = 2.0 V(for products with 100 pins or more), VBATT = 2.3 V (for the 64-pin product), VCC = 0V
					—	3.3	—		V_{BATT} = 3.3 V, VCC = 0V
Analog power supply current*7	During 12-bit A/D conversion (including temperature sensor)			I_{AVCC0}	—	2.3	3.2	mA	
	During 10-bit A/D conversion			I_{VREFH}*9	—	1.0	1.65	mA	
	During D/A conversion (per unit)				—	0.7	1.0	mA	
	Waiting for A/D, D/A conversion (all units)*10			—	—	25	35	μA	
	A/D, D/A converter in standby mode (all units)*10				—	0.1	4.0	μA	
Reference power supply current	During 12-bit A/D conversion			I_{VREFH0}	—	0.6	0.7	mA	
	Waiting for 12-bit A/D conversion (per unit)				—	0.5	0.6	mA	
	12-bit A/D converter in standby mode (per unit)				—	0.1	2.0	μA	

Table 5.13 Clock Timing (Sub-Clock Related)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0, V_{BATT} = 2.0 to 3.6 V (for products with 100 pins or more), V_{BATT} = 2.3 to 3.6 V (for the 64-pin product),
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock frequency	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillator start-up time	t_{SUBOSC}	—	—	*1		Figure 5.12
Sub-clock oscillation stabilization wait offset time*3	$t_{SUBOSCWT0}$	1.8	—	2.6	s	
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	*2	s	

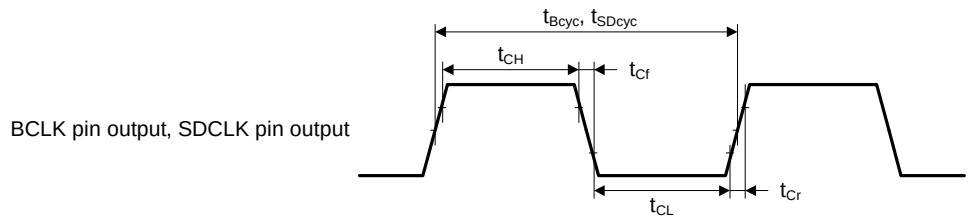
Note 1. When using a sub-clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles n selected by the value of the SOSCWTCR.SSTS[4:0] bits determines the sub-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{SUBOSCWT} = \max\left(t_{SUBOSC}, t_{SUBOSCWT0}\right) + \frac{n}{f_{SUB}}$$

The notation “max (t_{SUBOSC}, $t_{SUBOSCWT0}$)“ indicates whichever is higher of t_{SUBOSC} and $t_{SUBOSCWT0}$.

Note 3. The minimum value and maximum value of the sub-clock oscillation stabilization wait offset time (tSUBOSCWT0) is the references only for 100-pin or more products. For 64-pin products, consider the value of tSUBOSCWT0 to be 0.



Test conditions: VOH = VCC × 0.7, VOL = VCC × 0.3, IOH = –1.0 mA, IOL = 1.0 mA, C = 30 pF

Figure 5.3 BCLK Pin Output, SDCLK Pin Output Timing

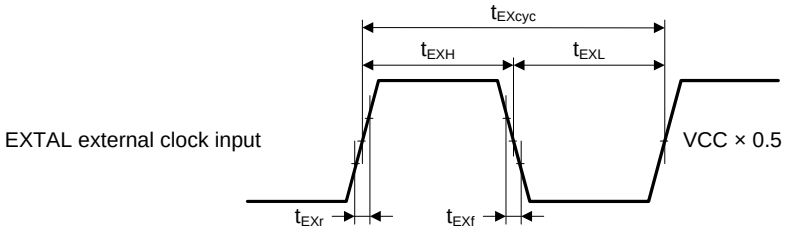


Figure 5.4 EXTAL External Clock Input Timing

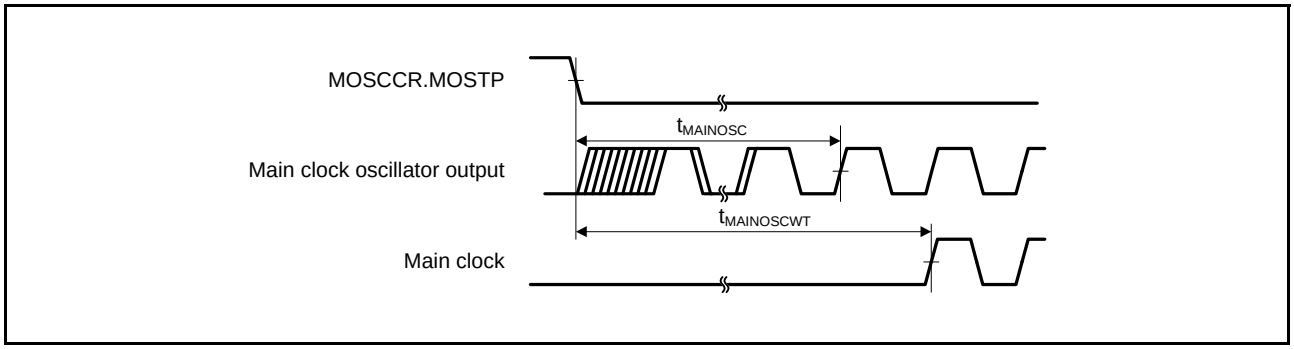


Figure 5.5 Main Clock Oscillation Start Timing

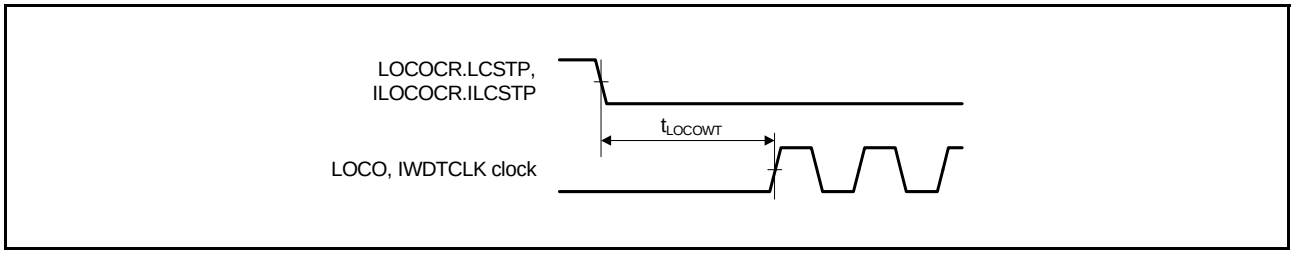


Figure 5.6 LOCO, IWDTCLK Oscillation Start Timing

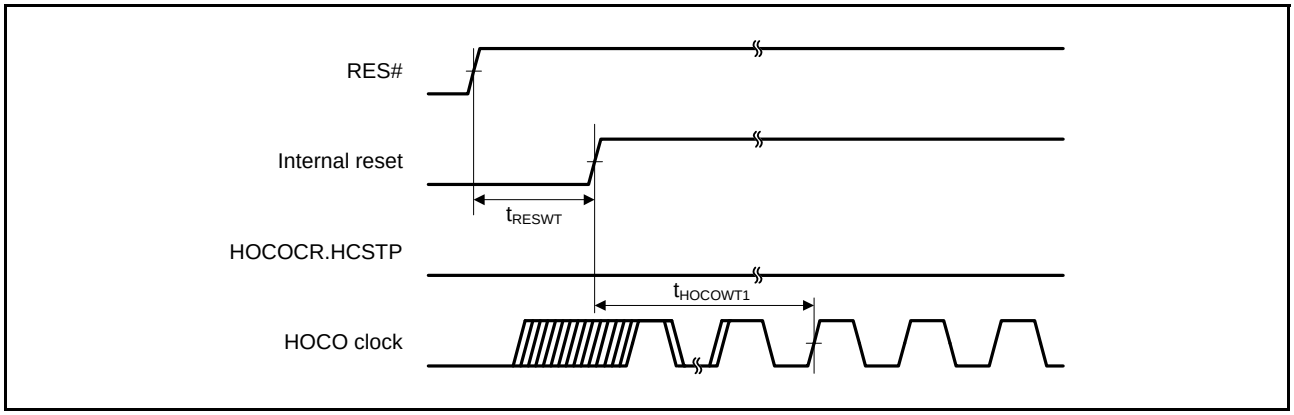


Figure 5.7 HOCO Oscillation Start Timing (After Reset is Canceled by Setting the OFS1.HOCOEN Bit to 0)

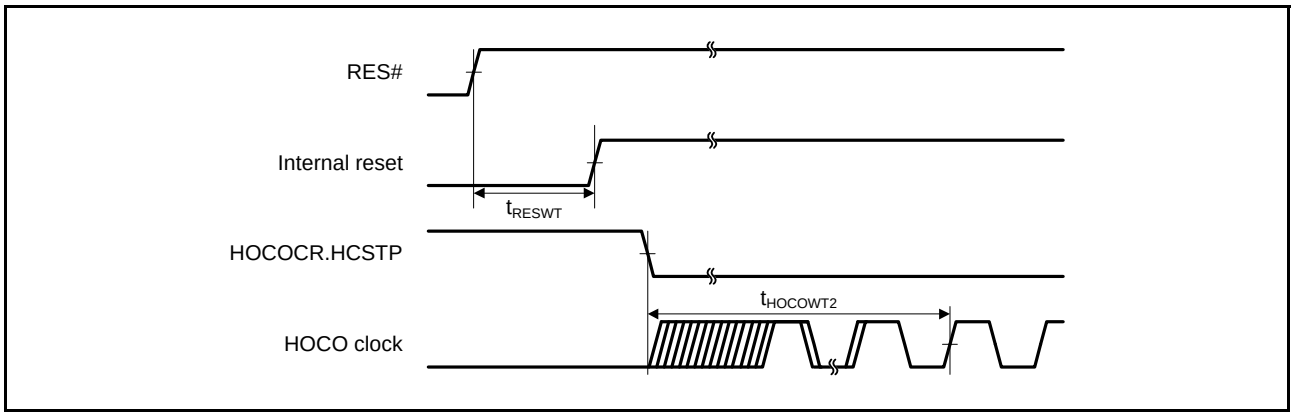


Figure 5.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

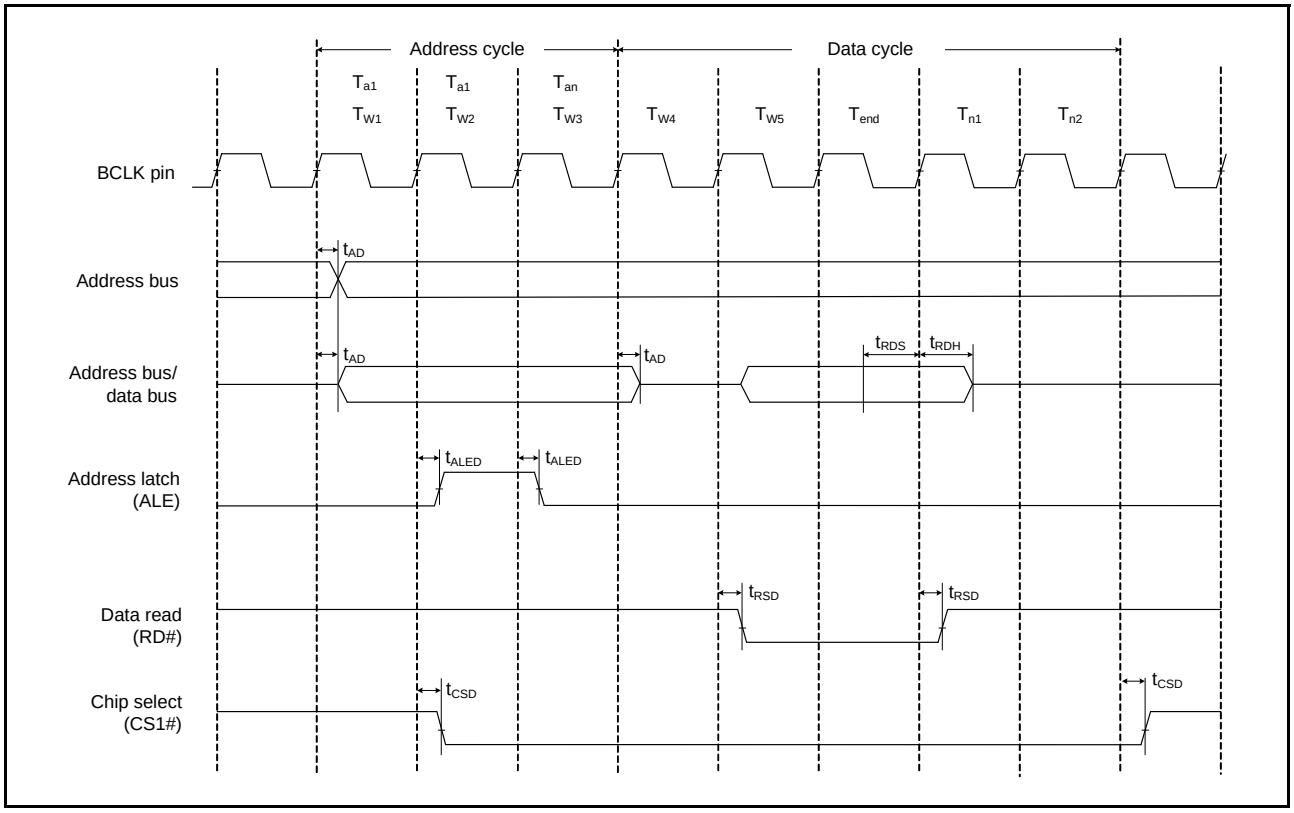


Figure 5.17 Address/Data Multiplexed Bus Read Access Timing

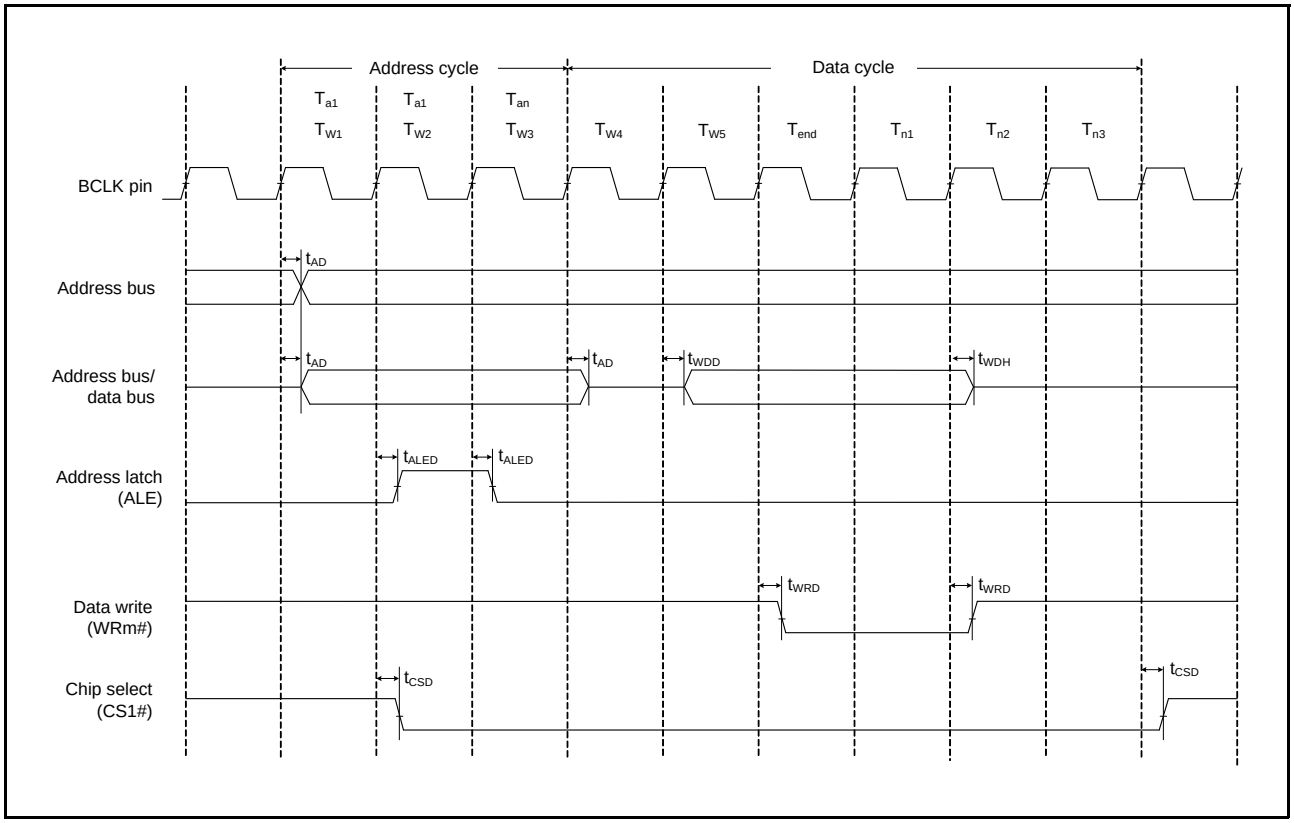
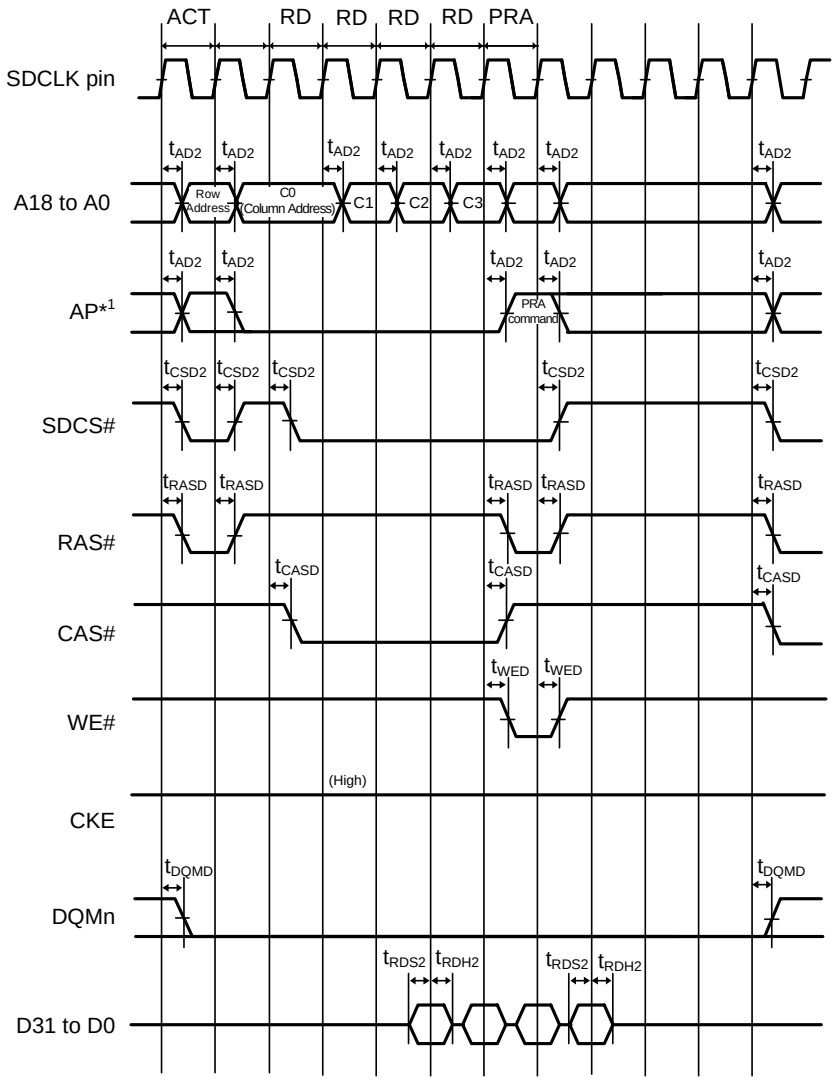


Figure 5.18 Address/Data Multiplexed Bus Write Access Timing



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.26 SDRAM Space Multiple Read Bus Timing

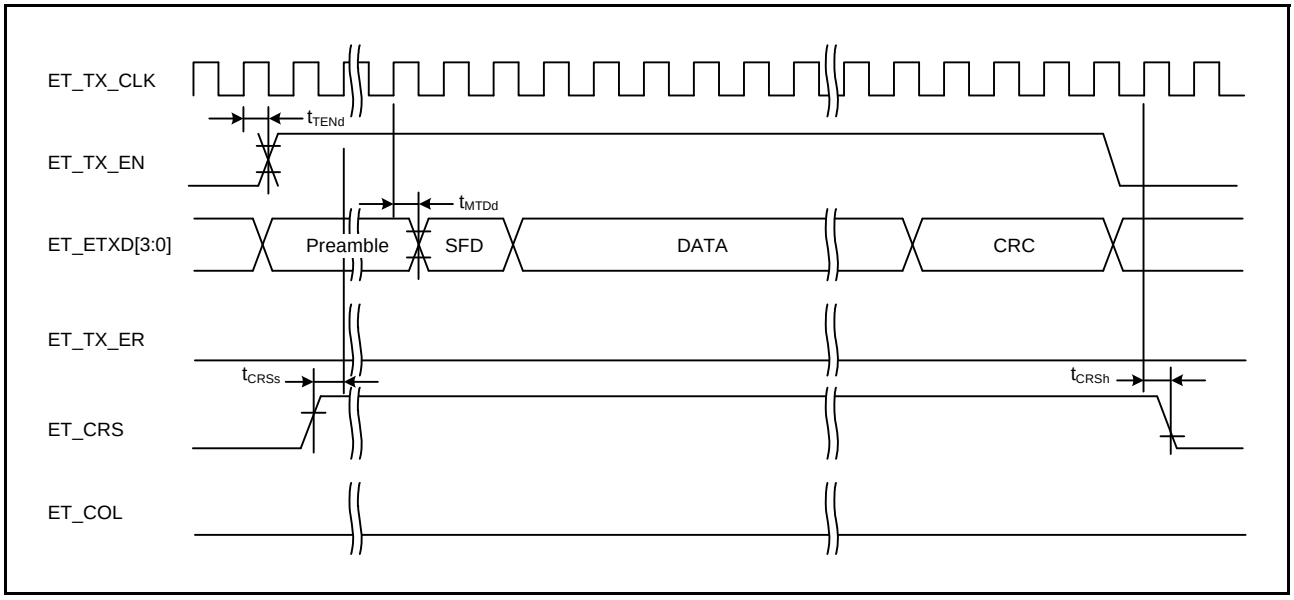


Figure 5.53 MII Transmission Timing (Normal Operation)

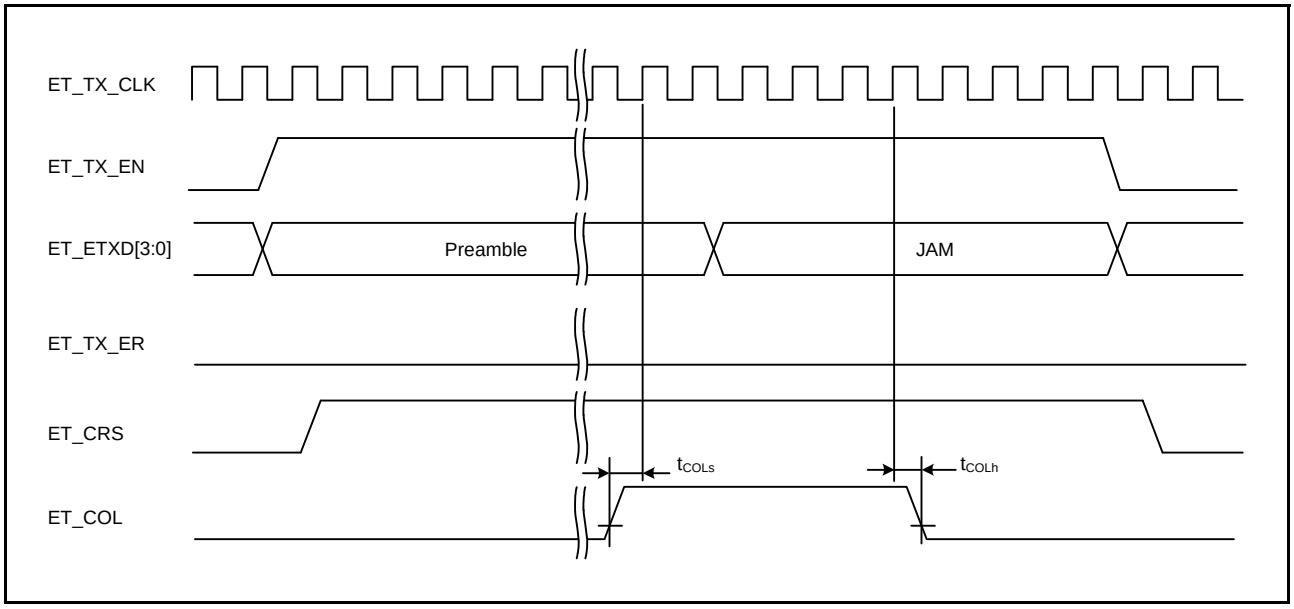


Figure 5.54 MII Transmission Timing (Conflict Occurrence)

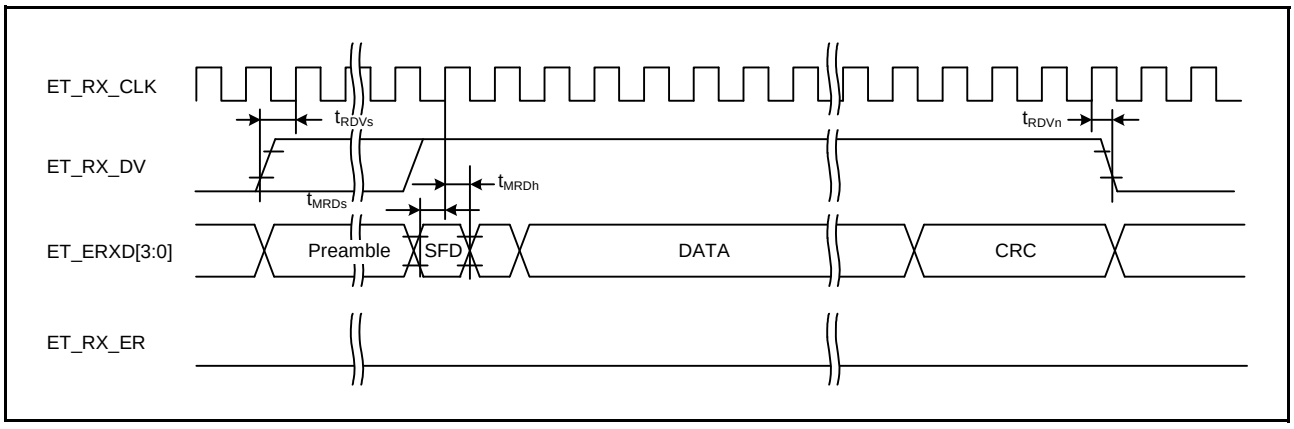
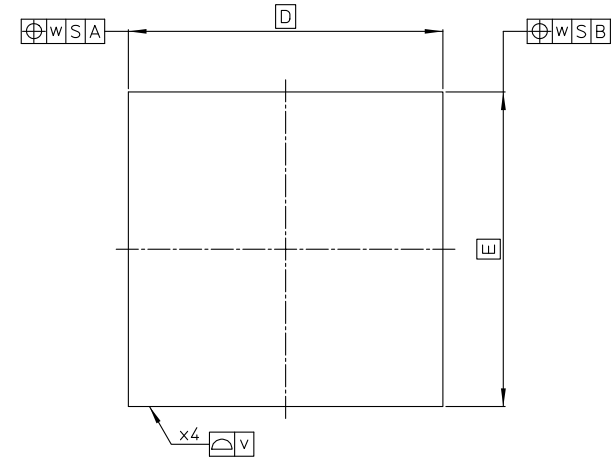
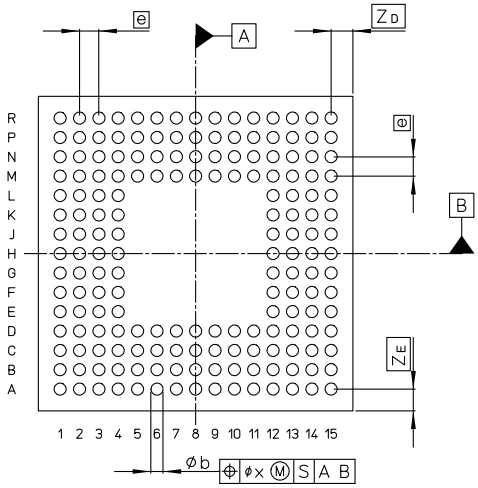


Figure 5.55 MII Reception Timing (Normal Operation)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g

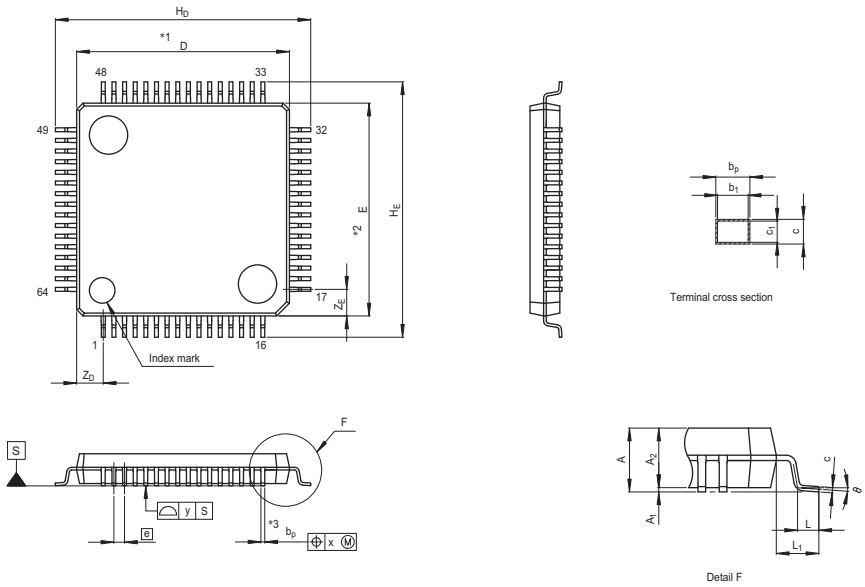




Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

Figure B 176-pin LFBGA (PLBG0176GA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g

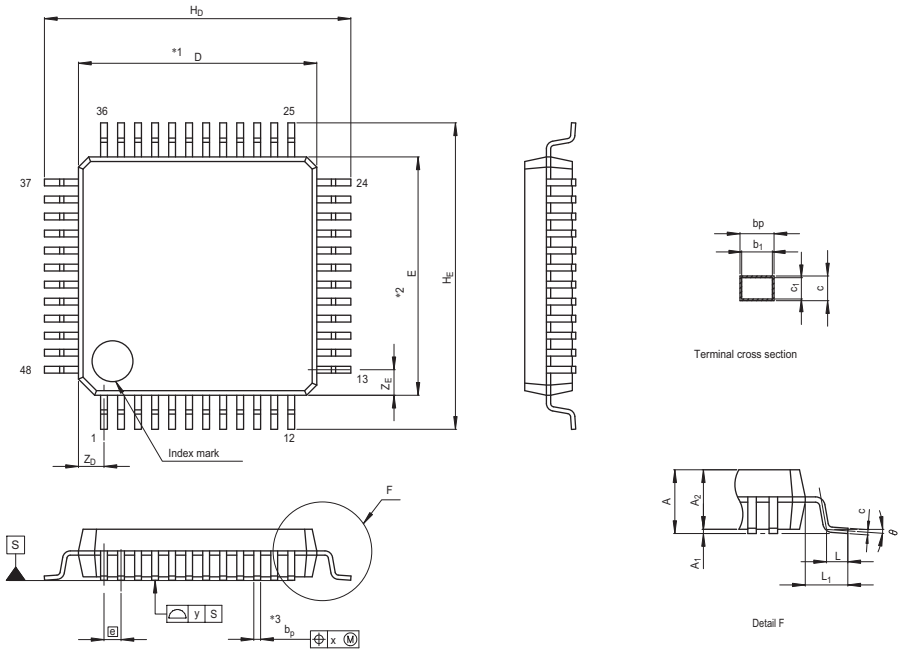


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure I 64-pin LQFP (PLQP0064KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure J 48-pin LQFP (PLQP0048KB-A)

Rev.	Date	Description	
		Page	Summary
1.60	Mar 13. 2013	Feature	
		1	Changed
		1. Overview	
		2 to 7	Table 1.1 Outline of Specifications: changed, note added
		8	Table1.2 Comparison of Functions for Different Packages in the RX63N/RX631 Group, changed
		9 to 15	Table 1.3 List of Products, changed
		16	Figure 1.1 How to Read the Product Part No., changed
		17	Figure 1.2 Block Diagram, changed
		24 to 32	Figure 1.3 to Figure 1.11 Pin Assignment: note, added
		53 to 57	Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA), added
		62 to 64	Table 1.11 List of Pins and Pin Functions (64-Pin LQFP), added
		65, 66	Table 1.12 List of Pins and Pin Functions (48-Pin LQFP), added
		3. Address Space	
		71	Figure 3.1 Memory Map in Each Operating Mode, changed
		4. I/O Registers	
		75 to 120	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics	
		All	Characteristics and timing conditions in the tables, changed
		124, 125	Table 5.4 DC Characteristics (3), changed
		126	Table 5.5 DC Characteristics (4), changed
		127	5.3 AC Characteristics, changed
		130, 131	Table 5.11, Clock Timing (Except for Sub-Clock Related): Condition and the table, changed, note, added
		132	Table 5.12 Clock Timing (Sub-Clock Related): Condition and the table, changed, note, added
		176	Table 5.33 Battery Backup Function Characteristics: Condition, changed
		Appendix 1.Package Dimensions	
		189	Figure H 64-pin LQFP (PLQP0064KB-A), added
		190	Figure I 48-pin LQFP (PLQP0048KB-A), added
1.70	Oct 08. 2013	Features	
		1	changed
		1. Overview	
		2 to 7	Table 1.1 Outline of Specifications, General I/O ports, Packages, changed, Parallel data capture unit (PDC), added.
		8	Table 1.2 Comparison of Functions for Different Packages in the RX63N/RX631 Group, 64-pin LQFP, changed, 64-pin TFLGA, Parallel data capture unit (PDC), added.
		9 to 16	Table 1.3 List of Products, changed.
		17	Figure 1.1 How to Read the Product Part No., changed
		18	Figure 1.2 Block Diagram, changed
		19 to 24	Table 1.4 Pin Functions,changed, Parallel data capture unit (PDC), added
		32	Figure 1.10 Pin Assignment (64-Pin TFLGA), added
		35 to 40	Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA), changed
		41 to 45	Table 1.6 List of Pin and Pin Functions (176-Pin LQFP), changed
		46 to 50	Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA), changed
		51 to 55	Table 1.8 List of Pins and Pin Functions (144-Pin LQFP), changed
		65 to 66	Table 1.11 List of Pins and Pin Functions (64-Pin TFLGA), added
		3. Address Space	
		76	Figure 3.1 Memory Map in Each Operating Mode, changed
		4. I/O Registers	
		79	(4) Restrictions in Relation to RMPA and String-Manipulation Instructions, added