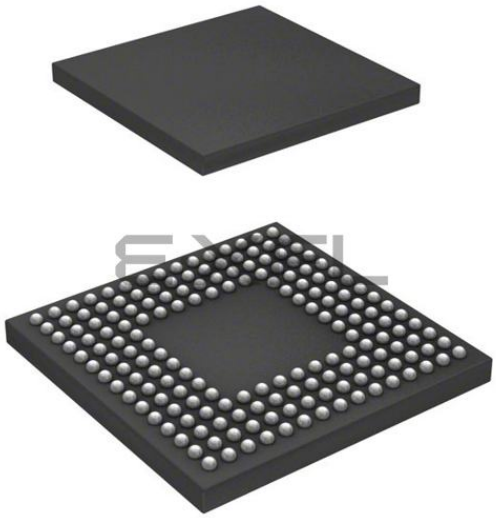
Renesas Electronics America Inc - R5F56318DDBG#U0 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

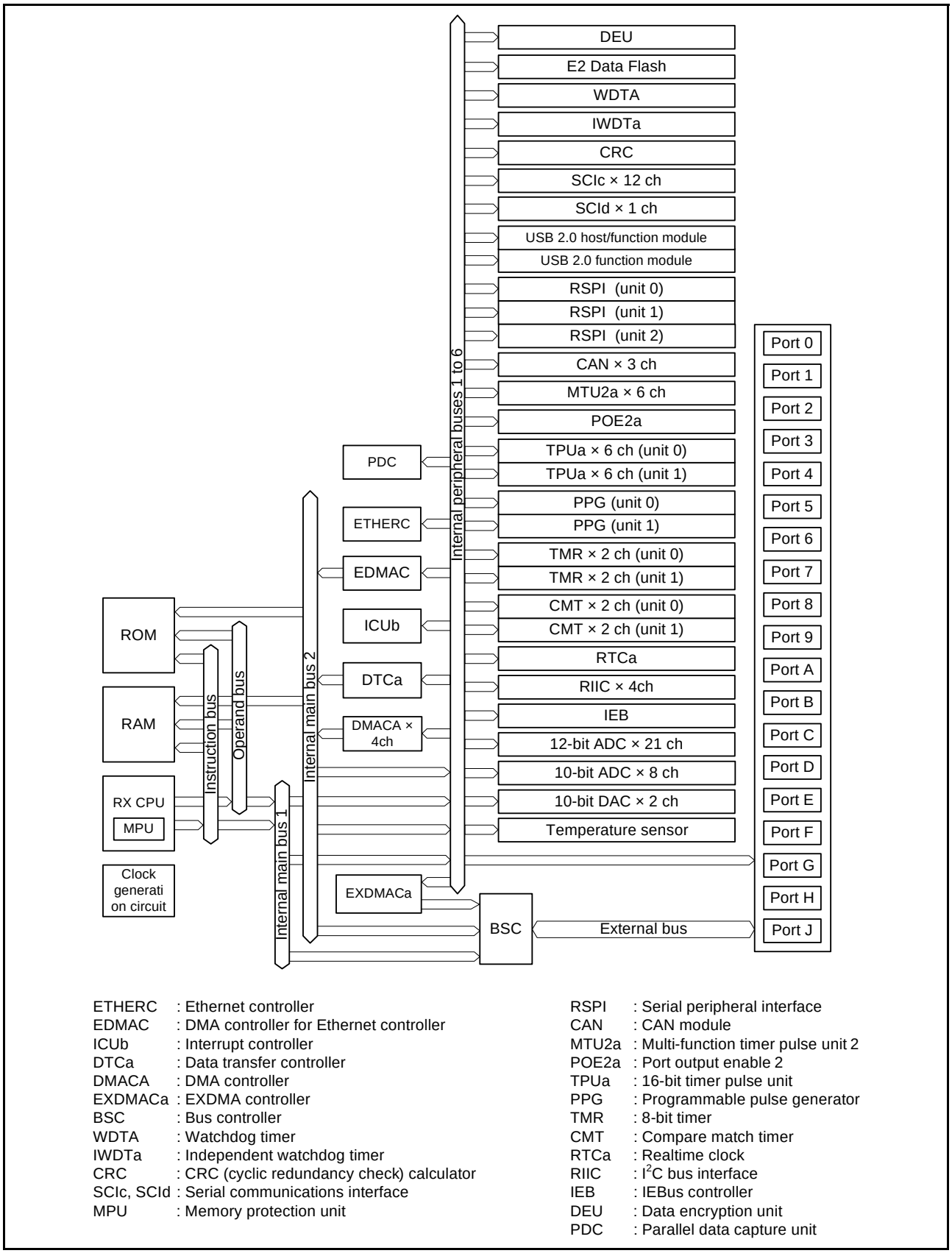
Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56318ddbg-u0

Table 1.1 Outline of Specifications (3/6)

Classification	Module/Function	Description
I/O ports	General I/O ports	• I/O ports for the 177-pin TFLGA, 176-pin LFBGA and 176-pin LQFP I/O pins: 133 Input pins: 1 Pull-up resistors: 133 Open-drain outputs: 133 5-V tolerance: 18 • I/O ports for the 145-pin TFLGA and 144-pin LQFP I/O pins: 111 Input pins: 1 Pull-up resistors: 111 Open-drain outputs: 111 5-V tolerance: 18 • I/O ports for the 100-pin TFLGA (in the planning stage) and 100-pin LQFP I/O pins: 78 Input pins: 1 Pull-up resistors: 78 Open-drain outputs: 78 5-V tolerance: 17 • I/O ports for the 64-pin TFLGA I/O pins: 39 Input pin: 1 Pull-up resistors: 39 Open-drain outputs: 39 5-V tolerance: 8 • I/O ports for the 64-pin LQFP I/O pins: 42 Input pin: 1 Pull-up resistors: 42 Open-drain outputs: 42 5-V tolerance: 8 8-bit port switching function • I/O ports for the 48-pin LQFP I/O pins: 30 Input pin: 1 Pull-up resistors: 30 Open-drain outputs: 30 5-V tolerance: 6 8-bit port switching function

1.3 Block Diagram

Figure 1.2 shows a block diagram.



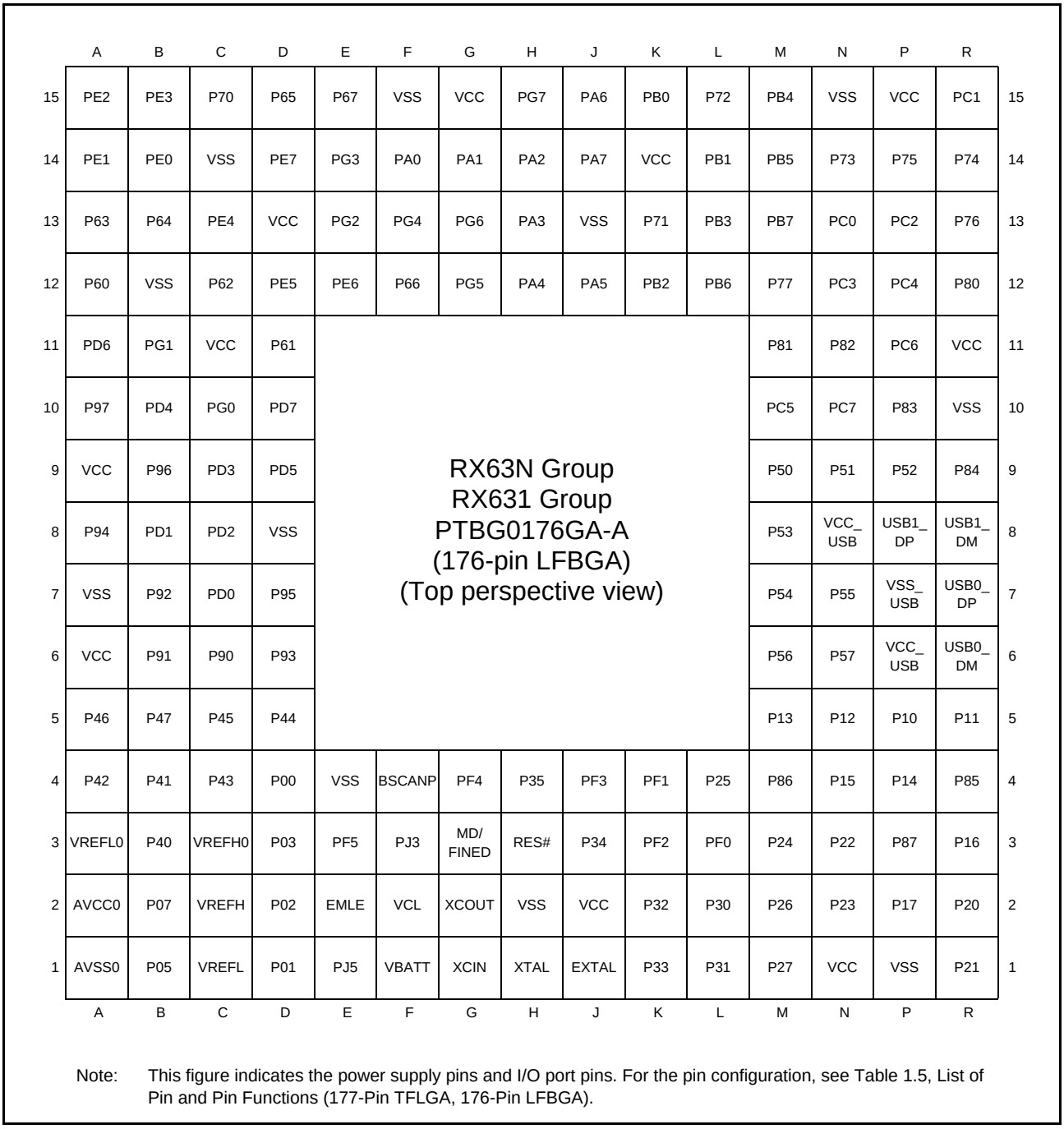
ETHERC : Ethernet controller
EDMAC : DMA controller for Ethernet controller
ICUb : Interrupt controller
DTCa : Data transfer controller
DMACA : DMA controller
EXDMACa : EXDMA controller
BSC : Bus controller
WDTA : Watchdog timer
IWDTa : Independent watchdog timer
CRC : CRC (cyclic redundancy check) calculator
SCIc, SCId : Serial communications interface
MPU : Memory protection unit

RSPI : Serial peripheral interface
CAN : CAN module
MTU2a : Multi-function timer pulse unit 2
POE2a : Port output enable 2
TPUa : 16-bit timer pulse unit
PPG : Programmable pulse generator
TMR : 8-bit timer
CMT : Compare match timer
RTCa : Realtime clock
RIIC : I^2C bus interface
IEB : IEBus controller
DEU : Data encryption unit
PDC : Parallel data capture unit

Figure 1.2 Block Diagram

Table 1.4 Pin Functions (5/6)

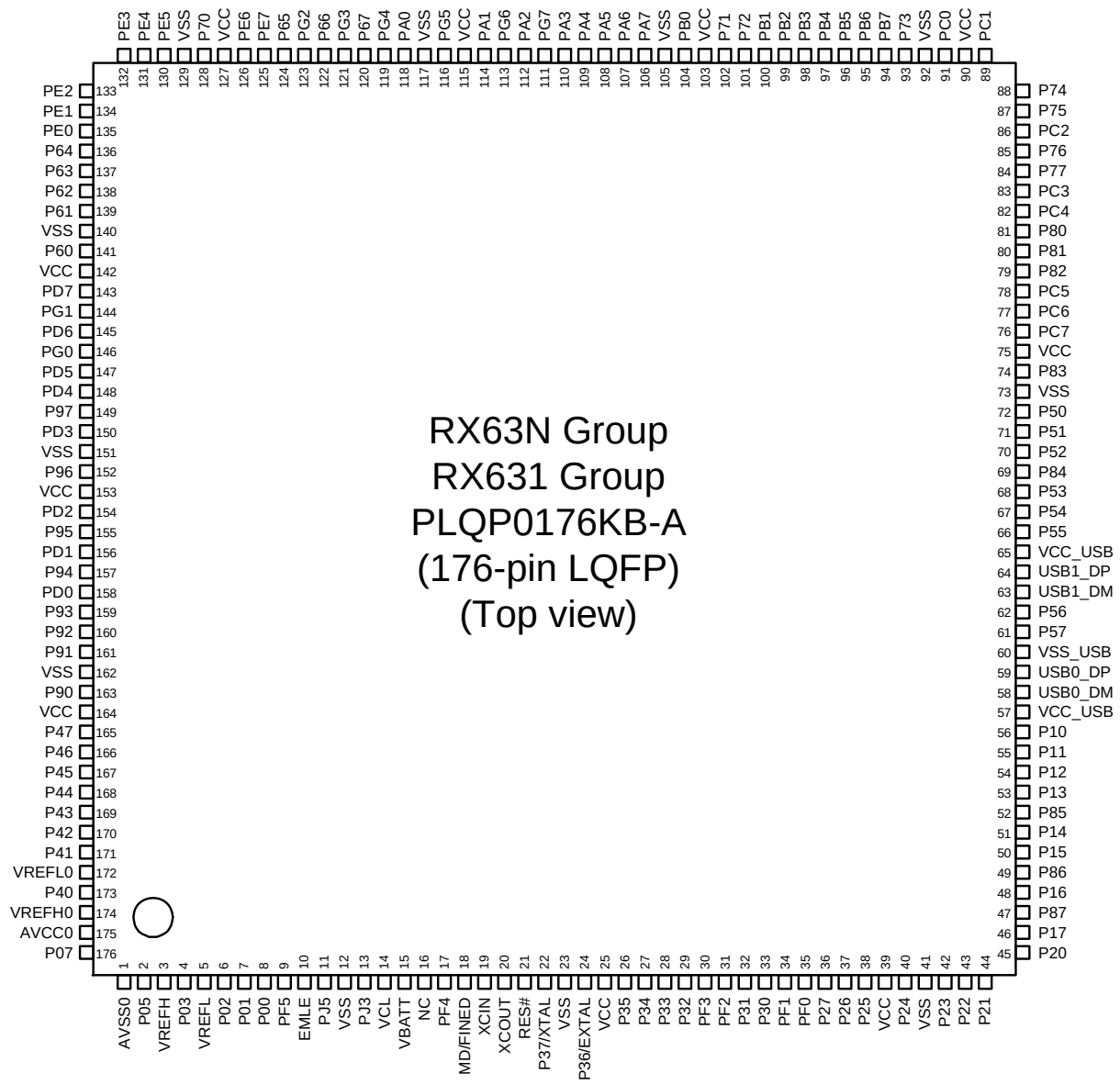
Classifications	Pin Name	I/O	Description
Ethernet controller	ET_MDIO	I/O	Inputs or outputs bidirectional signals for exchange of management information between the RX63N Group and the PHY-LSI.
Parallel data capture unit (PDC)	PIXCLK	Input	Parallel data transfer clock
	VSYNC	Input	Vertical synchronization signal
	HSYNC	Input	Horizontal synchronization signal
	PIXD7 to PIXD0	Input	8-bit data
	PCKO	Output	Outputs parallel data transfer clock signal
USB power pins	VCC_USB	Input	Power supply pin. When the USB is not to be used, connect it to the VCC pin.
	VSS_USB	Input	Ground pin. When the USB is not to be used, connect it to the VSS pin.
USB 2.0 host/function module	USB0_DP, USB1_DP	I/O	Inputs or outputs USB transceiver D+ data.
	USB0_DM, USB1_DM	I/O	Inputs or outputs USB transceiver D- data.
	USB0_VBUS, USB1_VBUS	Input	Input pins for detection of connection and disconnection of the USB cable.
	USB0_EXICEN	Output	Output pin for control the low power of the OTG chip.
	USB0_VBUSEN	Output	Supply enable pin of VBUS (5 V) for the OTG chip.
	USB0_OVRCURA, USB0_OVRCURB,	Input	Input pin for detection of external over current.
	USB0_ID	Input	ID input pin of mini-AB connector at the OTG operation.
	USB0_DPUPE, USB1_DPUPE	Output	Pull-up control pins of the D+ signal at the function operation.
	USB0_DPRPD	Output	Pull-down control pins of the D+ signal at the host operation.
	USB0_DRPD	Output	Pull-down control pins of the D- signal at the host operation.
CAN module	CRX0 to CRX2	Input	Input pin.
	CTX0 to CTX2	Output	Output pin.
Serial peripheral interface	RSPCKA, RSPCKB RSPCKC	I/O	Clock input/output pin.
	MOSIA, MOSIB, MOSIC	I/O	Inputs or outputs data output from the master.
	MISOA, MISOB, MISOC	I/O	Inputs or outputs data output from the slave.
	SSLA0, SSLB0, SSLC0	I/O	Input or output pins slave selection
	SSLA1 to SSLA3 SSLB1 to SSLB3 SSLC1 to SSLC3	Output	Output pins slave selection
IEBus controller	IERXD	Input	Input pin for data reception.
	IETXD	Output	Output pin for data transmission.
Realtime clock	RTCOUT	Output	Output pin for 1-Hz clock.
	RTCIC0 to RTCIC2	Input	Time capture event input pin
12-bit A/D converter	AN000 to AN020	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pins for the external trigger signals that start the A/D conversion.
10-bit A/D converter	AN0 to AN7	Input	Input pins for the analog signals to be processed by the A/D converter.
	ANEX0	Output	Extended analog output pin
	ANEX1	Input	Extended analog input pin
	ADTRG#	Input	Input pins for the external trigger signals that start the A/D conversion.
D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter.



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	VCC	P61								P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	VCC	P96	PD3	PD5								P50	P51	P52	P84	9
8	P94	PD1	PD2	VSS								P53	VCC_ USB	USB1_ DP	USB1_ DM	8
7	VSS	P92	PD0	P95								P54	P55	VSS_ USB	USB0_ DP	7
6	VCC	P91	P90	P93								P56	P57	VCC_ USB	USB0_ DM	6
5	P46	P47	P45	P44								P13	P12	P10	P11	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P85	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	VREFH	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	VREFL	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.4 Pin Assignment (176-Pin LFBGA)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pin and Pin Functions (176-Pin LQFP).

Figure 1.5 Pin Assignment (176-Pin LQFP)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
A1	AVSS0						
A2	AVCC0						
A3	VREFL0						
A4		P42				IRQ10-DS	AN002
A5		P46				IRQ14-DS	AN006
A6	VCC						
A7	VSS						
A8		P94	A20/D20				
A9	VCC						
A10		P97	A23/D23				
A11		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
A12		P60	CS0#				
A13		P63	CS3#/CAS#				
A14		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/RSPCKB		ANEX1
A15		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/PO23	RXD12/SMISO12/ SSCL12/RXDX12/SSLB3/ MOSIB	IRQ7-DS	AN0
B1		P05				IRQ13	DA1
B2		P07				IRQ15	ADTRG0#
B3		P40				IRQ8-DS	AN000
B4		P41				IRQ9-DS	AN001
B5		P47				IRQ15-DS	AN007
B6		P91	A17/D17		SCK7		AN015
B7		P92	A18/D18		RXD7/SMISO7/SSCL7		AN016
B8		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
B9		P96	A22/D22				
B10		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
B11		PG1	D25				
B12	VSS						
B13		P64	CS4#/WE#				
B14		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
B15		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/PO26/ POE8#	ET_ERXD3/CTS12#/ RTS12#/SS12#/MISOB		AN1
C1	VREFL						
C2	VREFH						
C3	VREFH0						
C4		P43				IRQ11-DS	AN003
C5		P45				IRQ13-DS	AN005
C6		P90	A16/D16		TXD7/SMOSI7/SSDA7		AN014
C7		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
C8		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
C9		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
C10		PG0	D24				
C11	VCC						
C12		P62	CS2#/RAS#				
C13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	ET_ERXD2/SSLB0		AN2

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (4/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
L3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
L4		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/USB0_VBUSEN/ PIXCLK		
L5		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
L6		P56	EDACK1	MTIOC3C/TIOCA1			
L7		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
L8	TRCLK	P83	EDACK1	MTIOC4C	CTS10#/RTS10#/SS10#/ ET_CRS/RMII_CRS_DV		
L9		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	SCK8/RSPCKA/ ET_ETXD2		
L10		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TIOCC6/TCLKE/TMCI1/ PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0/ET_TX_CLK		
L11		PC2	A18	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD/ET_RX_DV		
L12		P73	CS3#	PO16	ET_WOL		
L13	VSS						
M1		P22	EDREQ0	MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0/USB0_DRPD/PIXD6		
M2		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/ IETXD/PIXD3	IRQ7	ADTRG#
M3		P86		TIOCA0	PIXD1		
M4		P12		TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
M5	VCC_USB						
M6	VSS_USB						
M7		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
M8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TIOCA6/TMCI2/PO30	RXD8/SMISO8/SSCL8/ MOSIA/ET_ETXD3	IRQ13	
M9	TRDATA1	P81	EDACK0	MTIOC3D/PO27	RXD10/SMISO10/SSCL10/ ET_ETXD0/RMII_TXD0		
M10		P77	CS7#	PO23	TXD11/SMOSI11/SSDA11/ ET_RX_ER/RMII_RX_ER		
M11		PC0	A16	MTIOC3C/TCLKC/PO17	CTS5#/RTS5#/SS5#/ SSLA1/SCL3/ET_ERXD3	IRQ14	
M12		PC1	A17	MTIOC3A/TCLKD/PO18	SCK5/SSLA2/SDA3/ ET_ERXD2	IRQ12	
M13	VCC						
N1		P21		MTIOC1B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/SSCL0/ SCL1/USB0_EXICEN/ PIXD5	IRQ9	
N2		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/SSDA0/ SDA1/USB0_ID/PIXD4	IRQ8	
N3		P87		TIOCA2	PIXD2		
N4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
N5					USB0_DM		
N6					USB0_DP		

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (2/5)

Pin No. 144-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
36		P21		MTIOC1B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/SSCL0/ SCL1/USB0_EXICEN/ PIXD5	IRQ9	
37		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/SSDA0/ SDA1/USB0_ID/PIXD4	IRQ8	
38		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/IETXD/PIXD3	IRQ7	ADTRG#
39		P87		TIOCA2	PIXD2		
40		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
41		P86		TIOCA0	PIXD1		
42		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/ TMCI2/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ PIXD0	IRQ5	
43		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
44		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
45		P12		TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
46	VCC_USB						
47					USB0_DM		
48					USB0_DP		
49	VSS_USB						
50		P56	EDACK1	MTIOC3C/TIOCA1			
51	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET_EXOUT	IRQ10	
52	TRDATA2	P54	ALE/EDACK0	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX1/ET_LINKSTA		
53		P53*1	BCLK				
54		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
55		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
56		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
57	VSS						
58	TRCLK	P83	EDACK1	MTIOC4C	CTS10#/RTS10#/ SS10#/ET_CRS/ RMII_CRS_DV		
59	VCC						
60		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA/ET_COL	IRQ14	
61		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TIOCA6/TMCI2/PO30	RXD8/SMISO8/SSCL8/ MOSIA/ET_ETXD3	IRQ13	
62		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/ TMRI2/PO29	SCK8/RSPCKA/ ET_ETXD2		
63	TRSYNC	P82	EDREQ1	MTIOC4A/PO28	TXD10/SMOSI10/ SSDA10/ET_ETXD1/ RMII_TXD1		

Table 1.11 List of Pins and Pin Functions (64-Pin TFLGA) (2/2)

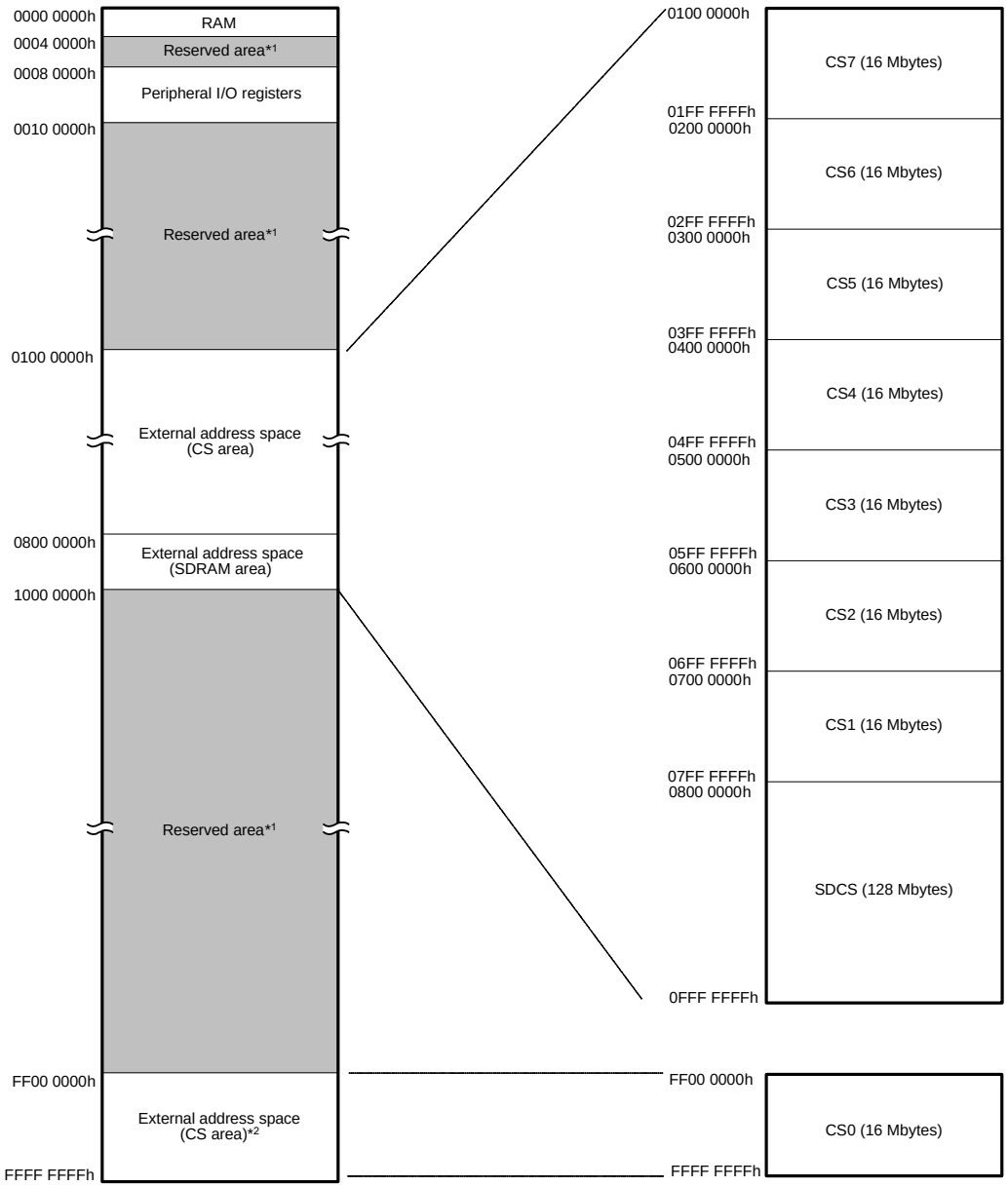
Pin No. 64-pin TFLGA	Power Supply Clock System Control	I/O Port	Timers (MTU2a, TPUa, TMR, PPG, RTCa, POE2a)	Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
E4	TMS	P16	MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ RTCOUT	TXD1/SMOSI1/SSDA1/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
E5		PC4	MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#	SCK5/SSLA0/ USB0_DPRPD		
E6	VCC					
E7	VSS					
E8		PB0	MTIC5W/TIOCA3/PO24	RXD6/SMISO6/SSCL6/ RSPCKA	IRQ12	
F1	VCC					
F2		P35			NMI	
F3		P31	MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
F4		PC5	MTIOC3B/MTCLKD/TMRI2/ PO29	RSPCKA/USB0_ID		
F5		P15	MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2	RXD1/SMISO1/SSCL1/ CRX1-DS/USB1_DPUPE	IRQ5	
F6		PB1	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD6/SMOSI6/SSDA6	IRQ4-DS	
F7		PB5	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	SCK9		
F8		PB3	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	SCK6		
G1	EXTAL	P36				
G2	TDO	P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ MOSIB/USB0_VBUSEN		
G3	VCC_USB					
G4	VSS_USB					
G5	VCC_USB					
G6		PC6	MTIOC3C/MTCLKA/TMCI2/ PO30	MOSIA/USB0_EXICEN	IRQ13	
G7		PC3	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ SDA2/IETXD		
G8		PB6	MTIOC3D/TIOCA5/PO30	RXD9/SMISO9/SSCL9		
H1	XTAL	P37				
H2	TRST#	P17	MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ POE8#	SCK1/MISOA/SDA2-DS/ IETXD/USB1_VBUS	IRQ7	
H3				USB0_DM		
H4				USB0_DP		
H5				USB1_DM		
H6				USB1_DP		
H7		PC2	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/SCL2/IERXD		
H8		PB7	MTIOC3B/TIOCB5/PO31	TXD9/SMOSI9/SSDA9		

Table 1.13 List of Pins and Pin Functions (48-Pin LQFP) (2/2)

Pin Number 48-Pin LQFP	Power Supply Clock System Control	I/O Port	Timer (MTU2a, TPUa, TMR, PPG, POE2a)	Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
29		PB0/ PC0	MTIC5W/TIOCA3/PO24	RXD6/SMISO6/SSCL6/ RSPCKA	IRQ12	
30	VSS					
31		PA6	MTIC5V/MTCLKB/TIOCA2/ TMCI3/PO22/POE2#	CTS5#/RTS5#/SS5#/ MOSIA		
32		PA4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS	
33		PA3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/SSCL5	IRQ6-DS	
34		PA1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2	IRQ11	
35		PE4	MTIOC4D/MTIOC1A/ PO28	SSLB0		AN012
36		PE3	MTIOC4B/PO26/POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN011
37		PE2	MTIOC4A/PO23	RXD12/SMISO12/SSCL12/ RXDX12/ SSLB3/MOSIB	IRQ7-DS	AN010
38		PE1	MTIOC4C/PO18	TXD12/SMISO12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB		AN009
39	VREFL					
40		P46			IRQ14-DS	AN006
41	VREFH					
42		P42			IRQ10-DS	AN002
43		P41			IRQ9-DS	AN001
44	VREFL0					
45		P40			IRQ8-DS	AN000
46	VREFH0					
47	AVCC0					
48	AVSS0					

3.2 External Address Space

The external address space is classified into CS areas (CS0 to CS7) and SDRAM area (SDCS). CS areas can be divided into up to eight areas (CS0 to SC7) corresponding to the CSn# signal to be output from the CSn# pin.
Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) and SDRAM area (SDCS) in on-chip ROM disabled extended mode.



Note 1. Reserved areas should not be accessed.
Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode.
In this mode, the address space for addresses above 1000 0000h is as shown in figure on this section, Memory Map in Each Operating Mode.

Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

Table 4.1 List of I/O Registers (Address Order) (6/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK		ICUb
0008 7048h	ICU	Interrupt request register 072	IR072	8	8	2 ICLK		
0008 7049h	ICU	Interrupt request register 073	IR073	8	8	2 ICLK		
0008 704Ah	ICU	Interrupt request register 074	IR074	8	8	2 ICLK		
0008 704Bh	ICU	Interrupt request register 075	IR075	8	8	2 ICLK		
0008 704Ch	ICU	Interrupt request register 076	IR076	8	8	2 ICLK		
0008 704Dh	ICU	Interrupt request register 077	IR077	8	8	2 ICLK		
0008 704Eh	ICU	Interrupt request register 078	IR078	8	8	2 ICLK		
0008 704Fh	ICU	Interrupt request register 079	IR079	8	8	2 ICLK		
0008 705Ah	ICU	Interrupt request register 090	IR090	8	8	2 ICLK		
0008 705Bh	ICU	Interrupt request register 091	IR091	8	8	2 ICLK		
0008 705Ch	ICU	Interrupt request register 092	IR092	8	8	2 ICLK		
0008 705Dh	ICU	Interrupt request register 093	IR093	8	8	2 ICLK		
0008 7062h	ICU	Interrupt request register 098	IR098	8	8	2 ICLK		
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK		
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2 ICLK		
0008 706Bh	ICU	Interrupt request register 107	IR107	8	8	2 ICLK		
0008 706Ch	ICU	Interrupt request register 108	IR108	8	8	2 ICLK		
0008 706Dh	ICU	Interrupt request register 109	IR109	8	8	2 ICLK		
0008 706Eh	ICU	Interrupt request register 110	IR110	8	8	2 ICLK		
0008 706Fh	ICU	Interrupt request register 111	IR111	8	8	2 ICLK		
0008 7070h	ICU	Interrupt request register 112	IR112	8	8	2 ICLK		
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK		
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8	2 ICLK		
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8	2 ICLK		
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8	2 ICLK		
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8	2 ICLK		
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8	2 ICLK		
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8	2 ICLK		
0008 7080h	ICU	Interrupt request register 128	IR128	8	8	2 ICLK		
0008 7081h	ICU	Interrupt request register 129	IR129	8	8	2 ICLK		
0008 7082h	ICU	Interrupt request register 130	IR130	8	8	2 ICLK		
0008 7083h	ICU	Interrupt request register 131	IR131	8	8	2 ICLK		
0008 7084h	ICU	Interrupt request register 132	IR132	8	8	2 ICLK		
0008 7085h	ICU	Interrupt request register 133	IR133	8	8	2 ICLK		
0008 7086h	ICU	Interrupt request register 134	IR134	8	8	2 ICLK		
0008 7087h	ICU	Interrupt request register 135	IR135	8	8	2 ICLK		
0008 7088h	ICU	Interrupt request register 136	IR136	8	8	2 ICLK		
0008 7089h	ICU	Interrupt request register 137	IR137	8	8	2 ICLK		
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8	2 ICLK		
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8	2 ICLK		
0008 708Ch	ICU	Interrupt request register 140	IR140	8	8	2 ICLK		
0008 708Dh	ICU	Interrupt request register 141	IR141	8	8	2 ICLK		
0008 708Eh	ICU	Interrupt request register 142	IR142	8	8	2 ICLK		
0008 708Fh	ICU	Interrupt request register 143	IR143	8	8	2 ICLK		
0008 7090h	ICU	Interrupt request register 144	IR144	8	8	2 ICLK		
0008 7091h	ICU	Interrupt request register 145	IR145	8	8	2 ICLK		
0008 7092h	ICU	Interrupt request register 146	IR146	8	8	2 ICLK		
0008 7093h	ICU	Interrupt request register 147	IR147	8	8	2 ICLK		
0008 7094h	ICU	Interrupt request register 148	IR148	8	8	2 ICLK		
0008 7095h	ICU	Interrupt request register 149	IR149	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (35/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C344h	ICU	Group 1 interrupt enable register	GEN01	32	32	1 to 2PCLKB	2 ICLK	ICUb
0008 C348h	ICU	Group 2 interrupt enable register	GEN02	32	32	1 to 2PCLKB	2 ICLK	
0008 C34Ch	ICU	Group 3 interrupt enable register	GEN03	32	32	1 to 2PCLKB	2 ICLK	
0008 C350h	ICU	Group 4 interrupt enable register	GEN04	32	32	1 to 2PCLKB	2 ICLK	
0008 C354h	ICU	Group 5 interrupt enable register	GEN05	32	32	1 to 2PCLKB	2 ICLK	
0008 C358h	ICU	Group 6 interrupt enable register	GEN06	32	32	1 to 2PCLKB	2 ICLK	
0008 C370h	ICU	Group 12 interrupt enable register	GEN12	32	32	1 to 2PCLKB	2 ICLK	
0008 C380h	ICU	Group 0 interrupt clear register	GCR00	32	32	1 to 2PCLKB	2 ICLK	
0008 C384h	ICU	Group 1 interrupt clear register	GCR01	32	32	1 to 2PCLKB	2 ICLK	
0008 C388h	ICU	Group 2 interrupt clear register	GCR02	32	32	1 to 2PCLKB	2 ICLK	
0008 C38Ch	ICU	Group 3 interrupt clear register	GCR03	32	32	1 to 2PCLKB	2 ICLK	
0008 C390h	ICU	Group 4 interrupt clear register	GCR04	32	32	1 to 2PCLKB	2 ICLK	
0008 C394h	ICU	Group 5 interrupt clear register	GCR05	32	32	1 to 2PCLKB	2 ICLK	
0008 C398h	ICU	Group 6 interrupt clear register	GCR06	32	32	1 to 2PCLKB	2 ICLK	
0008 C3C0h	ICU	Unit select register	SEL	32	32	1 to 2PCLKB	2 ICLK	
0008 C400h	RTC	64-Hz counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK	RTCa
0008 C402h	RTC	Second counter	RSECCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C404h	RTC	Minute counter	RMINCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C406h	RTC	Hour counter	RHRCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C408h	RTC	Day-of-week counter	RWKCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Ah	RTC	Date counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Ch	RTC	Month counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Eh	RTC	Year counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 C410h	RTC	Second alarm register	RSECAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C412h	RTC	Minute alarm register	RMINAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C414h	RTC	Hour alarm register	RHRAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C416h	RTC	Day-of-week alarm register	RWKAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C418h	RTC	Date alarm register	RDAYAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C41Ah	RTC	Month alarm register	RMONAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C41Ch	RTC	Year alarm register	RYRAR	16	16	2, 3 PCLKB	2 ICLK	
0008 C41Eh	RTC	Year alarm enable register	RYRAREN	8	8	2, 3 PCLKB	2 ICLK	
0008 C422h	RTC	RTC control register 1	RCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C424h	RTC	RTC control register 2	RCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 C426h	RTC	RTC control register 3	RCR3	8	8	2, 3 PCLKB	2 ICLK	
0008 C428h	RTC	RTC control register 4	RCR4	8	8	2, 3 PCLKB	2 ICLK	
0008 C42Ah	RTC	Frequency register H	RFRH	16	16	2, 3 PCLKB	2 ICLK	
0008 C42Ch	RTC	Frequency register L	RFRL	16	16	2, 3 PCLKB	2 ICLK	
0008 C42Eh	RTC	Time error adjustment register	RADJ	8	8	2, 3 PCLKB	2 ICLK	
0008 C440h	RTC	Time capture control register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK	
0008 C442h	RTC	Time capture control register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C444h	RTC	Time capture control register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 C452h	RTC	Second capture register 0	RSECCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C454h	RTC	Minute capture register 0	RMINCP0	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (45/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 024Eh	USB1	Device state changing register	DVCHGR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0250h	USB1	USB address register	USBADDR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0254h	USB1	USB request type register	USBREQ	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0256h	USB1	USB request value register	USBVAL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0258h	USB1	USB request index register	USBINDX	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 025Ah	USB1	USB request length register	USBLENG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	USBa
000A 025Ch	USB1	DCP configuration register	DCPCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 025Eh	USB1	DCP maximum packet size register	DCPMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0260h	USB1	DCP control register	DCPCTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0264h	USB1	Pipe window select register	PIPESEL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	

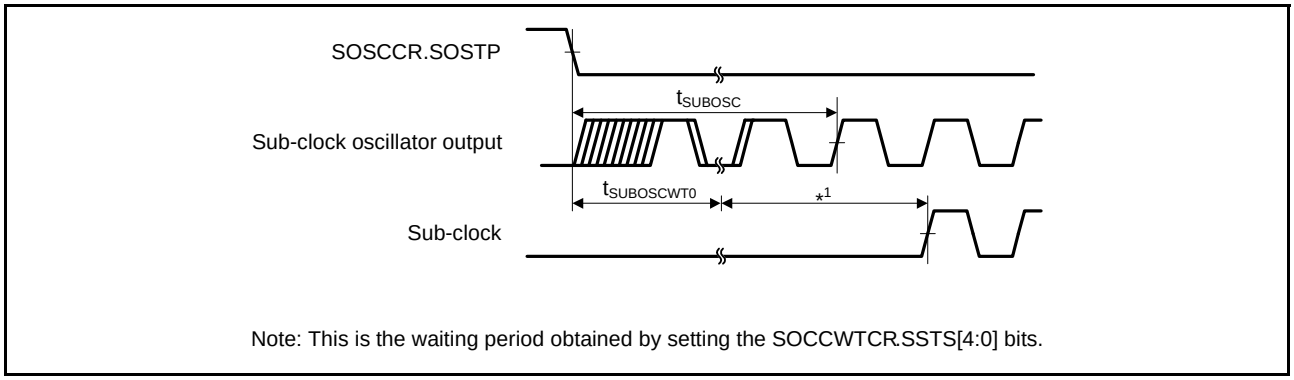


Figure 5.12 Sub-Clock Oscillation Start Timing

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.14 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	10	—	—	ms	Figure 5.13
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	10	—	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	1	—	—	ms	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	1	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2	—	—	s	
	High-speed on-chip oscillator operating		t_{SBYHO}	—	—	2	ms	
	Low-speed on-chip oscillator or IWDT-dedicated on-chip oscillator operating		t_{SBYLO}	—	—	800	µs	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	1.0	ms	Figure 5.14
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	45	—	46	t_{cyc}	

Note: The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator which requires the longest time of all operating oscillators to recover is operating alone.

Table 5.21 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V*1, VREFH0 = 2.7 V to AVCC0*1,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V,
PCLK = 8 to 50 MHz,
$T_a = T_{opr}$
High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit*2	Test Conditions
RSPI	Data output delay time	Master	Packages with 177 to 144 pins	t_{OD}	—	18	ns	Figure 5.43 to Figure 5.46 C = 30pF
			Packages with 100 pins or less		—	30		
		Slave	Packages with 177 to 144 pins		—	$3 \times t_{Pcyc} + 40$		
			Packages with 100 pins or less		—	$3 \times t_{Pcyc} + 50$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	Packages with 177 to 144 pins	t_{Dr}, t_{Df}	—	5	ns	
			Packages with 100 pins or less		—	10		
		Input			—	1	µs	
	SSL rise/fall time	Output	Packages with 177 to 144 pins	t_{SSLr}, t_{SSLf}	—	5	ns	
			Packages with 100 pins or less		—	10		
		Input			—	1	µs	
	Slave access time			t_{SA}	—	4	t_{Pcyc}	Figure 5.45 and Figure 5.46 C = 30pF
	Slave output release time			t_{REL}	—	3	t_{Pcyc}	

Note 1. When operation at 3.0 V or a lower voltage is needed, please contact a Renesas sales office.
Note 2. t_{Pcyc}: PCLK cycle

5.6 D/A Conversion Characteristics

Table 5.31 D/A Conversion Characteristics

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to VCC
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
$T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time	—	—	3.0	µs	20-pF capacitive load
Absolute accuracy	—	±2.0	±4.0	LSB	2-MΩ resistive load
	—	—	±3.0	LSB	4-MΩ resistive load
	—	—	±2.0	LSB	10-MΩ resistive load
RO output resistance	—	3.6	—	kΩ	

5.7 Temperature Sensor Characteristics

Table 5.32 Temperature Sensor Characteristics

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to VCC
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
$T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	
Temperature slope	—	4.1	—	mV/°C	
Output voltage (@25°C)	—	1.26	—	V	
Temperature sensor start time	—	—	30	µs	
Sampling time	—	—	5	µs	

5.13 Boundary Scan

Table 5.40 Boundary Scan

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 5.70
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TRST# pulse width	t_{TRSTW}	20	—	—	t_{TCKcyc}	Figure 5.71
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 5.72
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	40	ns	

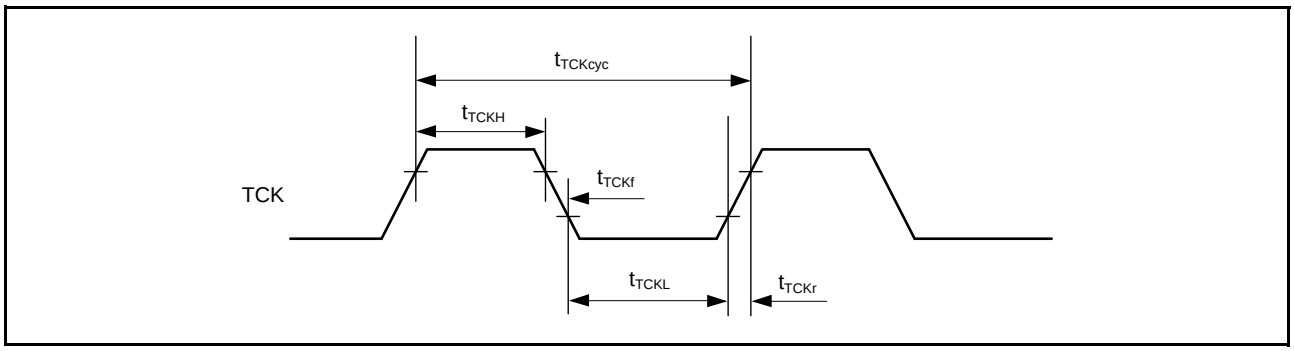


Figure 5.70 Boundary Scan TCK Timing

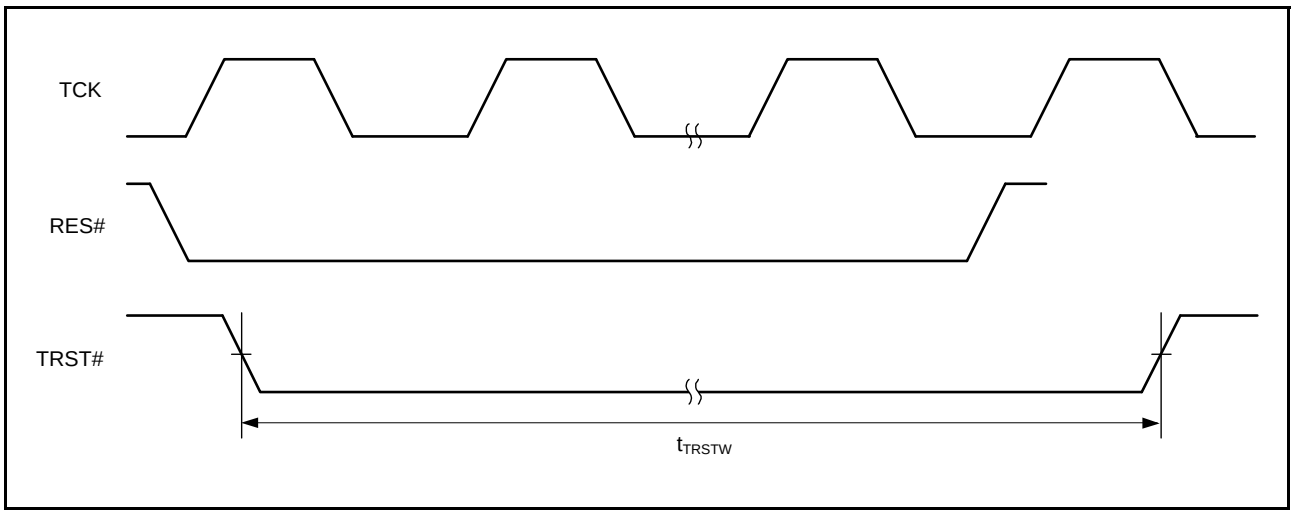
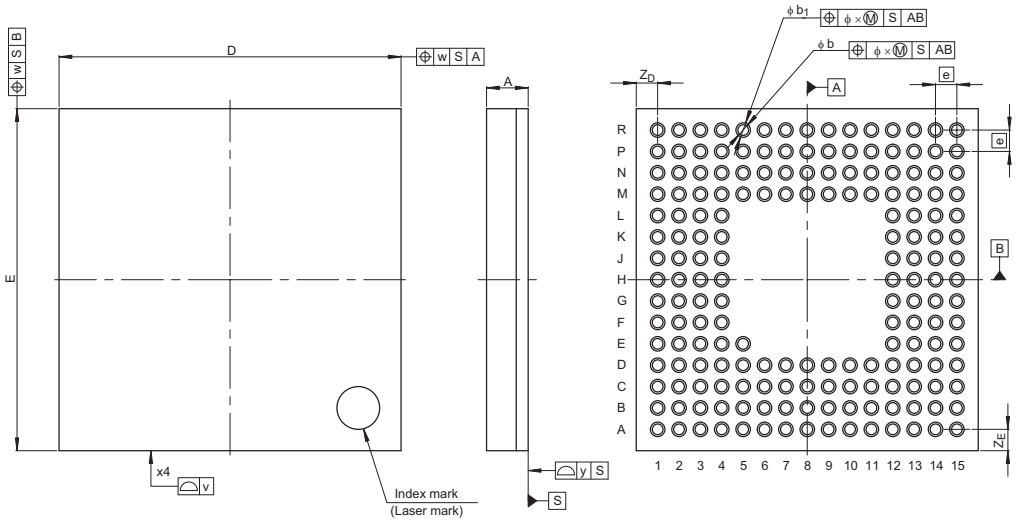


Figure 5.71 Boundary Scan TRST# Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

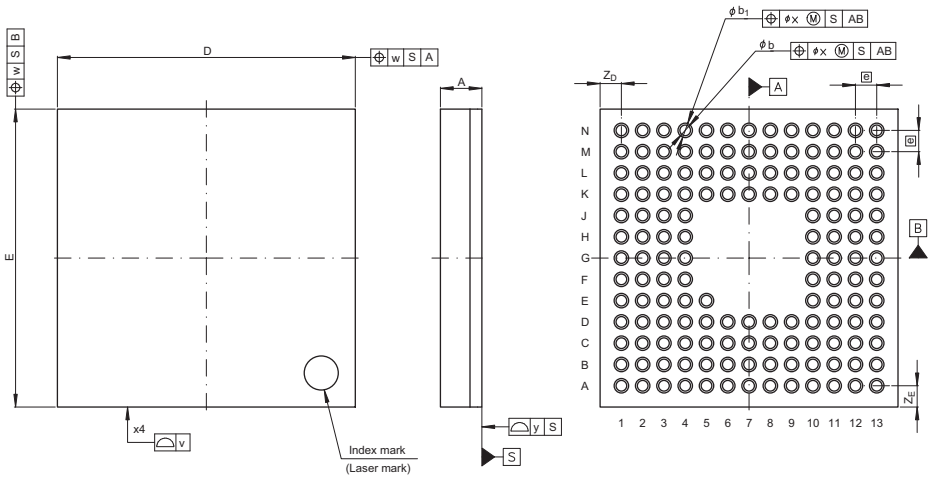
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA177-8x8-0.50	PTLG0177KA-A	177F0E-A	0.2g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	8.0	—
E	—	8.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure A 177-pin TFLGA (PTLG0177KA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA145-7x7-0.50	PTLG0145KA-A	145F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure D 145-pin TFLGA (PTLG0145KA-A)