# Renesas Electronics America Inc - R5F56318DDFB#V0 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

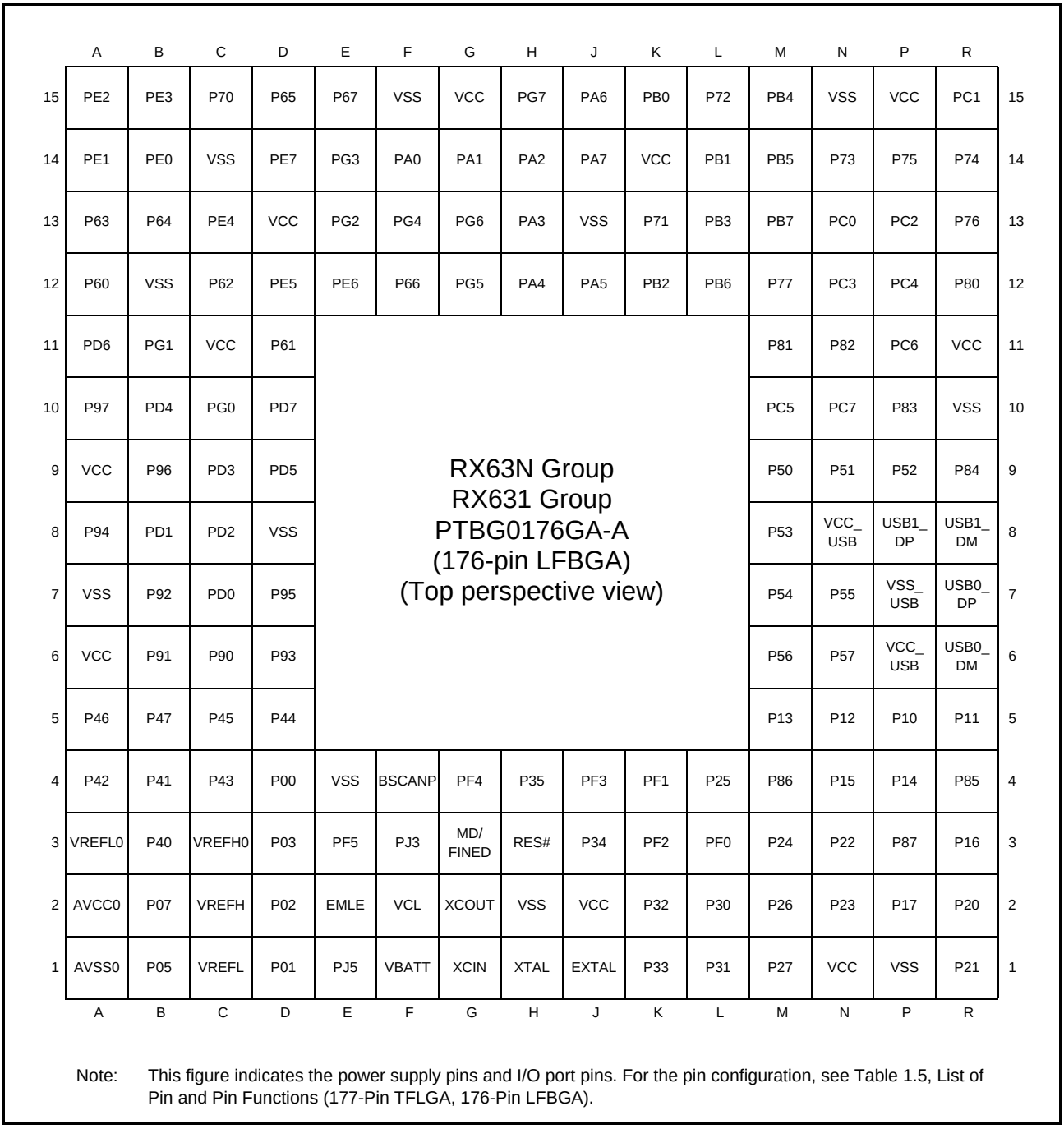
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 111 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 32K x 8 |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x10b, 21x12b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LFQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f56318ddfb-v0 |

**Table 1.1 Outline of Specifications (6/6)**

| Classification | Module/Function | Description |
|---|---|---|
| Communication function | Parallel data capture unit (PDC) | • 1 channel<br>• Communicates with an image sensor or other external I/Os and transfer parallel data such as an image output from those devices to internal RAM or external address spaces (CS space and SDRAM space) through DTC or DMAC. |
| 12-bit A/D converter (S12ADa) | | • 1 unit (1 unit x 21 channels)<br>• 12-bit resolution<br>• Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz)<br>• Operating mode<br>Scan mode (single scan mode or continuous scan mode)<br>• Sample-and-hold function<br>• Reference voltage generation<br>• Three ways to start A/D conversion<br>Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal.<br>• A/D conversion of the temperature sensor output |
| 10-bit A/D converter (ADb) | | • 1 unit (1 unit x 8 channels)<br>• 10-bit resolution<br>• Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz)<br>• Operating mode<br>Scan mode (single scan mode or continuous scan mode)<br>External amplifier connection mode<br>• Sample-and-hold function<br>• Three ways to start A/D conversion<br>Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal. |
| D/A converter (DAa) | | • 2 channels<br>• 10-bit resolution<br>• Output voltage: 0 V to VREFH |
| Temperature sensor | | • 1 channel<br>• Precision: ±1ºC<br>• The voltage of the temperature is converted into a digital value by the 12-bit A/D converter. |
| CRC calculator (CRC) | | • CRC code generation for arbitrary amounts of data in 8-bit units<br>• Select any of three generating polynomials:<br>$X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$.<br>• Generation of CRC codes for use with LSB-first or MSB-first communications is selectable |
| Unique ID | | A 16-byte device-specific ID (only for the G version) |
| Data encryption unit (DEU)*1 | | • AES encryption and decryption functions<br>• 128/192/256-bit key length<br>• ECB/CBC mode |
| Operating frequency | | Up to 100 MHz |
| Power supply voltage | | VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,<br>$V_{BATT}$ = 2.0 V to 3.6 V (for products with 100 or more pins),<br>$V_{BATT}$ = 2.3 V to 3.6 V (for the 64-pin product) |
| Operating temperature | | D version: -40 to +85°C,<br>G version: -40 to +105°C*2 |
| Package | | 177-pin TFLGA (PTLG0177KA-A)<br>176-pin LFBGA (PLBG0176GA-A)<br>176-pin LQFP (PLQP0176KB-A)<br>145-pin TFLGA (PTLG0145KA-A)<br>144-pin LQFP (PLQP0144KA-A)<br>100-pin TFLGA (PTLG0100JA-A) (in the planning stage)<br>100-pin LQFP (PLQP0100KB-A)<br>64-pin TFLGA (PTLG0064JA-A)<br>64-pin LQFP (PLQP0064KB-A)<br>48-pin LQFP (PLQP0048KB-A) |
| On-chip debugging system | | • E1 emulator (JTAG and FINE interfaces)<br>• E20 emulator (JTAG interface) |

Note 1. Please contact our sales office for more information.
Note 2. Please contact us if you are using a G version.




| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | PE2 | PE3 | P70 | P65 | P67 | VSS | VCC | PG7 | PA6 | PB0 | P72 | PB4 | VSS | VCC | PC1 | 15 |
| 14 | PE1 | PE0 | VSS | PE7 | PG3 | PA0 | PA1 | PA2 | PA7 | VCC | PB1 | PB5 | P73 | P75 | P74 | 14 |
| 13 | P63 | P64 | PE4 | VCC | PG2 | PG4 | PG6 | PA3 | VSS | P71 | PB3 | PB7 | PC0 | PC2 | P76 | 13 |
| 12 | P60 | VSS | P62 | PE5 | PE6 | P66 | PG5 | PA4 | PA5 | PB2 | PB6 | P77 | PC3 | PC4 | P80 | 12 |
| 11 | PD6 | PG1 | VCC | P61 | | | | | | | | P81 | P82 | PC6 | VCC | 11 |
| 10 | P97 | PD4 | PG0 | PD7 | | | | | | | | PC5 | PC7 | P83 | VSS | 10 |
| 9 | VCC | P96 | PD3 | PD5 | | | | | | | | P50 | P51 | P52 | P84 | 9 |
| 8 | P94 | PD1 | PD2 | VSS | | | | | | | | P53 | VCC_ USB | USB1_ DP | USB1_ DM | 8 |
| 7 | VSS | P92 | PD0 | P95 | | | | | | | | P54 | P55 | VSS_ USB | USB0_ DP | 7 |
| 6 | VCC | P91 | P90 | P93 | | | | | | | | P56 | P57 | VCC_ USB | USB0_ DM | 6 |
| 5 | P46 | P47 | P45 | P44 | | | | | | | | P13 | P12 | P10 | P11 | 5 |
| 4 | P42 | P41 | P43 | P00 | VSS | BSCANP | PF4 | P35 | PF3 | PF1 | P25 | P86 | P15 | P14 | P85 | 4 |
| 3 | VREFL0 | P40 | VREFH0 | P03 | PF5 | PJ3 | MD/ FINED | RES# | P34 | PF2 | PF0 | P24 | P22 | P87 | P16 | 3 |
| 2 | AVCC0 | P07 | VREFH | P02 | EMLE | VCL | XCOUT | VSS | VCC | P32 | P30 | P26 | P23 | P17 | P20 | 2 |
| 1 | AVSS0 | P05 | VREFL | P01 | PJ5 | VBATT | XCIN | XTAL | EXTAL | P33 | P31 | P27 | VCC | VSS | P21 | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

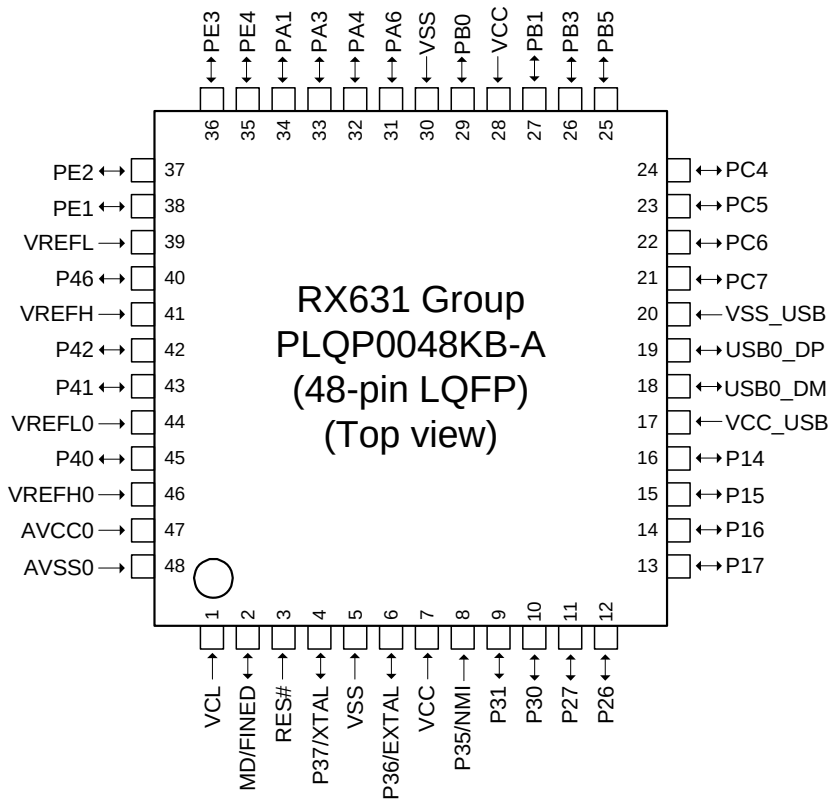
**Figure 1.4 Pin Assignment (176-Pin LFBGA)**

RX63N Group, RX631 Group
PTLG0100JA-A (100-pin TFLGA)
(Top view)

| | A | B | C | D | E | F | G | H | J | K | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | PE2 | PE3 | PE4 | PA0 | PA3 | VSS | VCC | PB7 | PC1 | PC2 | 10 |
| 9 | PE1 | PD7 | PE5 | PA1 | PA5 | PA7 | PB1 | PB6 | PC0 | PC3 | 9 |
| 8 | PE0 | PD6 | PD5 | PE7 | PA4 | PB0 | PB4 | PC6 | PC4 | PC5 | 8 |
| 7 | PD4 | PD3 | PD2 | PE6 | PA6 | PB2 | PB5 | PC7 | P50 | P51 | 7 |
| 6 | PD0 | PD1 | P47 | P46 | PA2 | PB3 | P52 | P54 | VCC_ USB | USB0_ DP | 6 |
| 5 | P43 | P44 | P42 | P45 | P41 | P12 | P53 | P55 | VSS_ USB | USB0_ DM | 5 |
| 4 | VREFL0 | P40 | VREFH0 | VBATT | P34 | P32 | P27 | P15 | P13 | P14 | 4 |
| 3 | P07 | AVCC0 | PJ3 | MD/ FINED | RES# | P35 | P30 | P16 | P17 | P20 | 3 |
| 2 | VREFH | AVSS0 | VREFL | XCOUT | VSS | VCC | P31 | P25 | P21 | P22 | 2 |
| 1 | P05 | EMLE | VCL | XCIN | XTAL | EXTAL | P33 | P26 | P24 | P23 | 1 |
| | A | B | C | D | E | F | G | H | J | K | |

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pins and Pin Functions (100-Pin LQFP).

**Figure 1.8 Pin Assignment (100-Pin TFLGA)**




Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.13, List of Pins and Pin Functions (48-Pin LQFP).

**Figure 1.12 Pin Assignment (48-Pin LQFP)**

**Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (4/5)**

| Pin Number 176-Pin LQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD, AD, DA |
|---|---|---|---|---|---|---|---|
| 100 | | PB1 | A9 | MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25 | ET_ERXD0/RMII_RXD0/ TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6 | IRQ4-DS | |
| 101 | | P72 | CS2# | | ET_MDC | | |
| 102 | | P71 | CS1# | | ET_MDIO | | |
| 103 | VCC | | | | | | |
| 104 | | PB0 | A8 | MTIC5W/TIOCA3/PO24 | ET_ERXD1/RMII_RXD1/ RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA | IRQ12 | |
| 105 | VSS | | | | | | |
| 106 | | PA7 | A7 | TIOCB2/PO23 | ET_WOL/MISOA | | |
| 107 | | PA6 | A6 | MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2# | ET_EXOUT/CTS5#/ RTS5#/SS5#/MOSIA | | |
| 108 | | PA5 | A5 | TIOCB1/PO21 | ET_LINKSTA/RSPCKA | | |
| 109 | | PA4 | A4 | MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20 | ET_MDC/TXD5/SMOSI5/ SSDA5/SSLA0 | IRQ5-DS | |
| 110 | | PA3 | A3 | MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19 | ET_MDIO/RXD5/SMISO5/ SSCL5 | IRQ6-DS | |
| 111 | TRDATA3 | PG7 | D31 | | | | |
| 112 | | PA2 | A2 | PO18 | RXD5/SMISO5/SSCL5/ SSLA3 | | |
| 113 | TRDATA2 | PG6 | D30 | | | | |
| 114 | | PA1 | A1/DQM3 | MTIOC0B/MTCLKC/ TIOCB0/PO17 | ET_WOL/SCK5/SSLA2 | IRQ11 | |
| 115 | VCC | | | | | | |
| 116 | TRCLK | PG5 | D29 | | | | |
| 117 | VSS | | | | | | |
| 118 | | PA0 | A0/BC0#/DQM2 | MTIOC4A/TIOCA0/PO16 | ET_TX_EN/ RMII_TXD_EN/SSLA1 | | |
| 119 | TRSYNC | PG4 | D28 | | | | |
| 120 | | P67 | CS7#/DQM1 | | CRX2*2 | IRQ15 | |
| 121 | TRDATA1 | PG3 | D27 | | | | |
| 122 | | P66 | CS6#/DQM0 | | CTX2*2 | | |
| 123 | TRDATA0 | PG2 | D26 | | | | |
| 124 | | P65 | CS5#/CKE | | | | |
| 125 | | PE7 | D15[A15/D15] | TIOCB11 | MISOB | IRQ7 | AN5 |
| 126 | | PE6 | D14[A14/D14] | TIOCA11 | MOSIB | IRQ6 | AN4 |
| 127 | VCC | | | | | | |
| 128 | SDCLK | P70 | | | | | |
| 129 | VSS | | | | | | |
| 130 | | PE5 | D13[A13/D13] | MTIOC4C/MTIOC2B/ TIOCB10 | ET_RX_CLK/REF50CK/ RSPCKB | IRQ5 | AN3 |
| 131 | | PE4 | D12[A12/D12] | MTIOC4D/MTIOC1A/ TIOCA10/PO28 | ET_ERXD2/SSLB0 | | AN2 |
| 132 | | PE3 | D11[A11/D11] | MTIOC4B/TIOCB9/PO26/ POE8# | ET_ERXD3/CTS12#/ RTS12#/SS12#/MISOB | | AN1 |
| 133 | | PE2 | D10[A10/D10] | MTIOC4A/TIOCA9/PO23 | RXD12/SMISO12/ SSCL12/RXDX12/SSLB3/ MOSIB | IRQ7-DS | AN0 |
| 134 | | PE1 | D9[A9/D9] | MTIOC4C/TIOCD9/PO18 | TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/RSPCKB | | ANEX1 |
| 135 | | PE0 | D8[A8/D8] | TIOCC9 | SCK12/SSLB1 | | ANEX0 |

**Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (1/5)**

| Pin No. 144-pin LQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD AD DA |
|---|---|---|---|---|---|---|---|
| 1 | AVSS0 | | | | | | |
| 2 | | P05 | | | | IRQ13 | DA1 |
| 3 | VREFH | | | | | | |
| 4 | | P03 | | | | IRQ11 | DA0 |
| 5 | VREFL | | | | | | |
| 6 | | P02 | | TMCI1 | SCK6 | IRQ10 | AN020 |
| 7 | | P01 | | TMCI0 | RXD6/SMISO6/SSCL6 | IRQ9 | AN019 |
| 8 | | P00 | | TMRI0 | TXD6/SMOSI6/SSDA6 | IRQ8 | AN018 |
| 9 | | PF5 | | | | IRQ4 | |
| 10 | EMLE | | | | | | |
| 11 | | PJ5 | | | | | |
| 12 | VSS | | | | | | |
| 13 | | PJ3 | | MTIOC3C | CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0# | | |
| 14 | VCL | | | | | | |
| 15 | VBATT | | | | | | |
| 16 | MD/FINED | | | | | | |
| 17 | XCIN | | | | | | |
| 18 | XCOUT | | | | | | |
| 19 | RES# | | | | | | |
| 20 | XTAL | P37 | | | | | |
| 21 | VSS | | | | | | |
| 22 | EXTAL | P36 | | | | | |
| 23 | VCC | | | | | | |
| 24 | | P35 | | | | NMI | |
| 25 | TRST# | P34 | | MTIOC0A/TMCI3/ PO12/POE2# | SCK6/SCK0/ USB0_DPRPD | IRQ4 | |
| 26 | | P33 | | MTIOC0D/TIOCD0/ TMRI3/PO11/POE3# | RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0/PCKO | IRQ3-DS | |
| 27 | | P32 | | MTIOC0C/TIOCC0/ TMO3/PO10/RTCOUT/ RTCIC2 | TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN/ VSYNC | IRQ2-DS | |
| 28 | TMS | P31 | | MTIOC4D/TMCI2/PO9/ RTCIC1 | CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE | IRQ1-DS | |
| 29 | TDI | P30 | | MTIOC4B/TMRI3/PO8/ RTCIC0/POE8# | RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD | IRQ0-DS | |
| 30 | TCK/FINEC | P27 | CS7# | MTIOC2B/TMCI3/PO7 | SCK1/RSPCKB | | |
| 31 | TDO | P26 | CS6# | MTIOC2A/TMO1/PO6 | TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB | | |
| 32 | | P25 | CS5#/EDACK1 | MTIOC4C/MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC | | ADTRG0# |
| 33 | | P24 | CS4#/EDREQ1 | MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4 | SCK3/USB0_VBUSEN/ PIXCLK | | |
| 34 | | P23 | EDACK0 | MTIOC3D/MTCLKD/ TIOCD3/PO3 | TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7 | | |
| 35 | | P22 | EDREQ0 | MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2 | SCK0/USB0_DRPD/ PIXD6 | | |

# 4. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below. Notes on writing to registers are also given at the end.

## (1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

## (2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

**[Examples of cases requiring special care]**

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

**Table 4.1 List of I/O Registers (Address Order) (7/50)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 7096h | ICU | Interrupt request register 150 | IR150 | 8 | 8 | 2 ICLK | | ICUb |
| 0008 7097h | ICU | Interrupt request register 151 | IR151 | 8 | 8 | 2 ICLK | | |
| 0008 7098h | ICU | Interrupt request register 152 | IR152 | 8 | 8 | 2 ICLK | | |
| 0008 7099h | ICU | Interrupt request register 153 | IR153 | 8 | 8 | 2 ICLK | | |
| 0008 709Ah | ICU | Interrupt request register 154 | IR154 | 8 | 8 | 2 ICLK | | |
| 0008 709Bh | ICU | Interrupt request register 155 | IR155 | 8 | 8 | 2 ICLK | | |
| 0008 709Ch | ICU | Interrupt request register 156 | IR156 | 8 | 8 | 2 ICLK | | |
| 0008 709Dh | ICU | Interrupt request register 157 | IR157 | 8 | 8 | 2 ICLK | | |
| 0008 709Eh | ICU | Interrupt request register 158 | IR158 | 8 | 8 | 2 ICLK | | |
| 0008 709Fh | ICU | Interrupt request register 159 | IR159 | 8 | 8 | 2 ICLK | | |
| 0008 70A0h | ICU | Interrupt request register 160 | IR160 | 8 | 8 | 2 ICLK | | |
| 0008 70A1h | ICU | Interrupt request register 161 | IR161 | 8 | 8 | 2 ICLK | | |
| 0008 70A2h | ICU | Interrupt request register 162 | IR162 | 8 | 8 | 2 ICLK | | |
| 0008 70A3h | ICU | Interrupt request register 163 | IR163 | 8 | 8 | 2 ICLK | | |
| 0008 70A4h | ICU | Interrupt request register 164 | IR164 | 8 | 8 | 2 ICLK | | |
| 0008 70A5h | ICU | Interrupt request register 165 | IR165 | 8 | 8 | 2 ICLK | | |
| 0008 70A6h | ICU | Interrupt request register 166 | IR166 | 8 | 8 | 2 ICLK | | |
| 0008 70A7h | ICU | Interrupt request register 167 | IR167 | 8 | 8 | 2 ICLK | | |
| 0008 70AAh | ICU | Interrupt request register 170 | IR170 | 8 | 8 | 2 ICLK | | |
| 0008 70ABh | ICU | Interrupt request register 171 | IR171 | 8 | 8 | 2 ICLK | | |
| 0008 70ACh | ICU | Interrupt request register 172 | IR172 | 8 | 8 | 2 ICLK | | |
| 0008 70ADh | ICU | Interrupt request register 173 | IR173 | 8 | 8 | 2 ICLK | | |
| 0008 70AEh | ICU | Interrupt request register 174 | IR174 | 8 | 8 | 2 ICLK | | |
| 0008 70AFh | ICU | Interrupt request register 175 | IR175 | 8 | 8 | 2 ICLK | | |
| 0008 70B0h | ICU | Interrupt request register 176 | IR176 | 8 | 8 | 2 ICLK | | |
| 0008 70B1h | ICU | Interrupt request register 177 | IR177 | 8 | 8 | 2 ICLK | | |
| 0008 70B2h | ICU | Interrupt request register 178 | IR178 | 8 | 8 | 2 ICLK | | |
| 0008 70B3h | ICU | Interrupt request register 179 | IR179 | 8 | 8 | 2 ICLK | | |
| 0008 70B4h | ICU | Interrupt request register 180 | IR180 | 8 | 8 | 2 ICLK | | |
| 0008 70B5h | ICU | Interrupt request register 181 | IR181 | 8 | 8 | 2 ICLK | | |
| 0008 70B6h | ICU | Interrupt request register 182 | IR182 | 8 | 8 | 2 ICLK | | |
| 0008 70B7h | ICU | Interrupt request register 183 | IR183 | 8 | 8 | 2 ICLK | | |
| 0008 70B8h | ICU | Interrupt request register 184 | IR184 | 8 | 8 | 2 ICLK | | |
| 0008 70B9h | ICU | Interrupt request register 185 | IR185 | 8 | 8 | 2 ICLK | | |
| 0008 70BAh | ICU | Interrupt request register 186 | IR186 | 8 | 8 | 2 ICLK | | |
| 0008 70BBh | ICU | Interrupt request register 187 | IR187 | 8 | 8 | 2 ICLK | | |
| 0008 70BCh | ICU | Interrupt request register 188 | IR188 | 8 | 8 | 2 ICLK | | |
| 0008 70BDh | ICU | Interrupt request register 189 | IR189 | 8 | 8 | 2 ICLK | | |
| 0008 70BEh | ICU | Interrupt request register 190 | IR190 | 8 | 8 | 2 ICLK | | |
| 0008 70BFh | ICU | Interrupt request register 191 | IR191 | 8 | 8 | 2 ICLK | | |
| 0008 70C0h | ICU | Interrupt request register 192 | IR192 | 8 | 8 | 2 ICLK | | |
| 0008 70C1h | ICU | Interrupt request register 193 | IR193 | 8 | 8 | 2 ICLK | | |
| 0008 70C2h | ICU | Interrupt request register 194 | IR194 | 8 | 8 | 2 ICLK | | |
| 0008 70C3h | ICU | Interrupt request register 195 | IR195 | 8 | 8 | 2 ICLK | | |
| 0008 70C4h | ICU | Interrupt request register 196 | IR196 | 8 | 8 | 2 ICLK | | |
| 0008 70C5h | ICU | Interrupt request register 197 | IR197 | 8 | 8 | 2 ICLK | | |
| 0008 70C6h | ICU | Interrupt request register 198 | IR198 | 8 | 8 | 2 ICLK | | |
| 0008 70C7h | ICU | Interrupt request register 199 | IR199 | 8 | 8 | 2 ICLK | | |
| 0008 70C8h | ICU | Interrupt request register 200 | IR200 | 8 | 8 | 2 ICLK | | |
| 0008 70C9h | ICU | Interrupt request register 201 | IR201 | 8 | 8 | 2 ICLK | | |
| 0008 70CAh | ICU | Interrupt request register 202 | IR202 | 8 | 8 | 2 ICLK | | |

**Table 4.1 List of I/O Registers (Address Order) (12/50)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 7322h | ICU | Interrupt source priority register 034 | IPR034 | 8 | 8 | 2 ICLK | | ICUb |
| 0008 7323h | ICU | Interrupt source priority register 035 | IPR035 | 8 | 8 | 2 ICLK | | |
| 0008 7324h | ICU | Interrupt source priority register 036 | IPR036 | 8 | 8 | 2 ICLK | | |
| 0008 7325h | ICU | Interrupt source priority register 037 | IPR037 | 8 | 8 | 2 ICLK | | |
| 0008 7326h | ICU | Interrupt source priority register 038 | IPR038 | 8 | 8 | 2 ICLK | | |
| 0008 7327h | ICU | Interrupt source priority register 039 | IPR039 | 8 | 8 | 2 ICLK | | |
| 0008 732Ah | ICU | Interrupt source priority register 042 | IPR042 | 8 | 8 | 2 ICLK | | |
| 0008 732Dh | ICU | Interrupt source priority register 045 | IPR045 | 8 | 8 | 2 ICLK | | |
| 0008 7330h | ICU | Interrupt source priority register 048 | IPR048 | 8 | 8 | 2 ICLK | | |
| 0008 7334h | ICU | Interrupt source priority register 052 | IPR052 | 8 | 8 | 2 ICLK | | |
| 0008 7338h | ICU | Interrupt source priority register 056 | IPR056 | 8 | 8 | 2 ICLK | | |
| 0008 733Eh | ICU | Interrupt source priority register 062 | IPR062 | 8 | 8 | 2 ICLK | | |
| 0008 7340h | ICU | Interrupt source priority register 064 | IPR064 | 8 | 8 | 2 ICLK | | |
| 0008 7341h | ICU | Interrupt source priority register 065 | IPR065 | 8 | 8 | 2 ICLK | | |
| 0008 7342h | ICU | Interrupt source priority register 066 | IPR066 | 8 | 8 | 2 ICLK | | |
| 0008 7343h | ICU | Interrupt source priority register 067 | IPR067 | 8 | 8 | 2 ICLK | | |
| 0008 7344h | ICU | Interrupt source priority register 068 | IPR068 | 8 | 8 | 2 ICLK | | |
| 0008 7345h | ICU | Interrupt source priority register 069 | IPR069 | 8 | 8 | 2 ICLK | | |
| 0008 7346h | ICU | Interrupt source priority register 070 | IPR070 | 8 | 8 | 2 ICLK | | |
| 0008 7347h | ICU | Interrupt source priority register 071 | IPR071 | 8 | 8 | 2 ICLK | | |
| 0008 7348h | ICU | Interrupt source priority register 072 | IPR072 | 8 | 8 | 2 ICLK | | |
| 0008 7349h | ICU | Interrupt source priority register 073 | IPR073 | 8 | 8 | 2 ICLK | | |
| 0008 734Ah | ICU | Interrupt source priority register 074 | IPR074 | 8 | 8 | 2 ICLK | | |
| 0008 734Bh | ICU | Interrupt source priority register 075 | IPR075 | 8 | 8 | 2 ICLK | | |
| 0008 734Ch | ICU | Interrupt source priority register 076 | IPR076 | 8 | 8 | 2 ICLK | | |
| 0008 734Dh | ICU | Interrupt source priority register 077 | IPR077 | 8 | 8 | 2 ICLK | | |
| 0008 734Eh | ICU | Interrupt source priority register 078 | IPR078 | 8 | 8 | 2 ICLK | | |
| 0008 734Fh | ICU | Interrupt source priority register 079 | IPR079 | 8 | 8 | 2 ICLK | | |
| 0008 735Ah | ICU | Interrupt source priority register 090 | IPR090 | 8 | 8 | 2 ICLK | | |
| 0008 735Bh | ICU | Interrupt source priority register 091 | IPR091 | 8 | 8 | 2 ICLK | | |
| 0008 735Ch | ICU | Interrupt source priority register 092 | IPR092 | 8 | 8 | 2 ICLK | | |
| 0008 735Dh | ICU | Interrupt source priority register 093 | IPR093 | 8 | 8 | 2 ICLK | | |
| 0008 7362h | ICU | Interrupt source priority register 098 | IPR098 | 8 | 8 | 2 ICLK | | |
| 0008 7366h | ICU | Interrupt source priority register 102 | IPR102 | 8 | 8 | 2 ICLK | | |
| 0008 736Ah | ICU | Interrupt source priority register 106 | IPR106 | 8 | 8 | 2 ICLK | | |
| 0008 736Bh | ICU | Interrupt source priority register 107 | IPR107 | 8 | 8 | 2 ICLK | | |
| 0008 736Ch | ICU | Interrupt source priority register 108 | IPR108 | 8 | 8 | 2 ICLK | | |
| 0008 736Dh | ICU | Interrupt source priority register 109 | IPR109 | 8 | 8 | 2 ICLK | | |
| 0008 736Eh | ICU | Interrupt source priority register 110 | IPR110 | 8 | 8 | 2 ICLK | | |
| 0008 736Fh | ICU | Interrupt source priority register 111 | IPR111 | 8 | 8 | 2 ICLK | | |
| 0008 7370h | ICU | Interrupt source priority register 112 | IPR112 | 8 | 8 | 2 ICLK | | |
| 0008 7372h | ICU | Interrupt source priority register 114 | IPR114 | 8 | 8 | 2 ICLK | | |
| 0008 737Ah | ICU | Interrupt source priority register 122 | IPR122 | 8 | 8 | 2 ICLK | | |
| 0008 737Eh | ICU | Interrupt source priority register 126 | IPR126 | 8 | 8 | 2 ICLK | | |
| 0008 7382h | ICU | Interrupt source priority register 130 | IPR130 | 8 | 8 | 2 ICLK | | |
| 0008 7384h | ICU | Interrupt source priority register 132 | IPR132 | 8 | 8 | 2 ICLK | | |
| 0008 7386h | ICU | Interrupt source priority register 134 | IPR134 | 8 | 8 | 2 ICLK | | |
| 0008 738Ah | ICU | Interrupt source priority register 138 | IPR138 | 8 | 8 | 2 ICLK | | |
| 0008 738Ch | ICU | Interrupt source priority register 140 | IPR140 | 8 | 8 | 2 ICLK | | |
| 0008 738Eh | ICU | Interrupt source priority register 142 | IPR142 | 8 | 8 | 2 ICLK | | |
| 0008 7392h | ICU | Interrupt source priority register 146 | IPR146 | 8 | 8 | 2 ICLK | | |

**Table 4.1 List of I/O Registers (Address Order) (14/50)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 7400h | ICU | DMAC activation request select register 0 | DMRSR0 | 8 | 8 | 2 ICLK | | ICUb |
| 0008 7404h | ICU | DMAC activation request select register 1 | DMRSR1 | 8 | 8 | 2 ICLK | | |
| 0008 7408h | ICU | DMAC activation request select register 2 | DMRSR2 | 8 | 8 | 2 ICLK | | |
| 0008 740Ch | ICU | DMAC activation request select register 3 | DMRSR3 | 8 | 8 | 2 ICLK | | |
| 0008 7500h | ICU | IRQ control register 0 | IRQCR0 | 8 | 8 | 2 ICLK | | |
| 0008 7501h | ICU | IRQ control register 1 | IRQCR1 | 8 | 8 | 2 ICLK | | |
| 0008 7502h | ICU | IRQ control register 2 | IRQCR2 | 8 | 8 | 2 ICLK | | |
| 0008 7503h | ICU | IRQ control register 3 | IRQCR3 | 8 | 8 | 2 ICLK | | |
| 0008 7504h | ICU | IRQ control register 4 | IRQCR4 | 8 | 8 | 2 ICLK | | |
| 0008 7505h | ICU | IRQ control register 5 | IRQCR5 | 8 | 8 | 2 ICLK | | |
| 0008 7506h | ICU | IRQ control register 6 | IRQCR6 | 8 | 8 | 2 ICLK | | |
| 0008 7507h | ICU | IRQ control register 7 | IRQCR7 | 8 | 8 | 2 ICLK | | |
| 0008 7508h | ICU | IRQ control register 8 | IRQCR8 | 8 | 8 | 2 ICLK | | |
| 0008 7509h | ICU | IRQ control register 9 | IRQCR9 | 8 | 8 | 2 ICLK | | |
| 0008 750Ah | ICU | IRQ control register 10 | IRQCR10 | 8 | 8 | 2 ICLK | | |
| 0008 750Bh | ICU | IRQ control register 11 | IRQCR11 | 8 | 8 | 2 ICLK | | |
| 0008 750Ch | ICU | IRQ control register 12 | IRQCR12 | 8 | 8 | 2 ICLK | | |
| 0008 750Dh | ICU | IRQ control register 13 | IRQCR13 | 8 | 8 | 2 ICLK | | |
| 0008 750Eh | ICU | IRQ control register 14 | IRQCR14 | 8 | 8 | 2 ICLK | | |
| 0008 750Fh | ICU | IRQ control register 15 | IRQCR15 | 8 | 8 | 2 ICLK | | |
| 0008 7510h | ICU | IRQ pin digital filter enable register 0 | IRQFLTE0 | 8 | 8 | 2 ICLK | | |
| 0008 7511h | ICU | IRQ pin digital filter enable register 1 | IRQFLTE1 | 8 | 8 | 2 ICLK | | |
| 0008 7514h | ICU | IRQ pin digital filter setting register 0 | IRQFLTC0 | 16 | 16 | 2 ICLK | | |
| 0008 7516h | ICU | IRQ pin digital filter setting register 1 | IRQFLTC1 | 16 | 16 | 2 ICLK | | |
| 0008 7580h | ICU | Non-maskable interrupt status register | NMISR | 8 | 8 | 2 ICLK | | |
| 0008 7581h | ICU | Non-maskable interrupt enable register | NMIER | 8 | 8 | 2 ICLK | | |
| 0008 7582h | ICU | Non-maskable interrupt status clear register | NMICLR | 8 | 8 | 2 ICLK | | |
| 0008 7583h | ICU | NMI pin interrupt control register | NMICR | 8 | 8 | 2 ICLK | | |
| 0008 7590h | ICU | NMI pin digital filter enable register | NMIFLTE | 8 | 8 | 2 ICLK | | |
| 0008 7594h | ICU | NMI pin digital filter setting register | NMIFLTC | 16 | 16 | 2 ICLK | | |
| 0008 8000h | CMT | Compare match timer start register 0 | CMSTR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8002h | CMT0 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8004h | CMT0 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8006h | CMT0 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8008h | CMT1 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 800Ah | CMT1 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 800Ch | CMT1 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8010h | CMT | Compare match timer start register 1 | CMSTR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8012h | CMT2 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8014h | CMT2 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8016h | CMT2 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8018h | CMT3 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 801Ah | CMT3 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 801Ch | CMT3 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8020h | WDT | WDT refresh register | WDTRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | WDTA |
| 0008 8022h | WDT | WDT control register | WDTCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8024h | WDT | WDT status register | WDTSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8026h | WDT | WDT reset control register | WDTRCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8030h | IWDT | IWDT refresh register | IWDTRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8032h | IWDT | IWDT control register | IWDTCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8034h | IWDT | IWDT status register | IWDTSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |

**Table 4.1 List of I/O Registers (Address Order) (34/50)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 C1B1h | MPC | PE1 pin function control register | PE1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B2h | MPC | PE2 pin function control register | PE2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1B3h | MPC | PE3 pin function control register | PE3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1B4h | MPC | PE4 pin function control register | PE4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1B5h | MPC | PE5 pin function control register | PE5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1B6h | MPC | PE6 pin function control register | PE6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1B7h | MPC | PE7 pin function control register | PE7PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1B8h | MPC | PF0 pin function control register | PF0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1B9h | MPC | PF1 pin function control register | PF1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1BAh | MPC | PF2 pin function control register | PF2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1BDh | MPC | PF5 pin function control register | PF5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1D3h | MPC | PJ3 pin function control register | PJ3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C280h | SYSTEM | Deep standby control register | DPSBYCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C282h | SYSTEM | Deep standby interrupt enable register 0 | DPSIER0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C283h | SYSTEM | Deep standby interrupt enable register 1 | DPSIER1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C284h | SYSTEM | Deep standby interrupt enable register 2 | DPSIER2 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C285h | SYSTEM | Deep standby interrupt enable register 3 | DPSIER3 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C286h | SYSTEM | Deep standby interrupt flag register 0 | DPSIFR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C287h | SYSTEM | Deep standby interrupt flag register 1 | DPSIFR1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C288h | SYSTEM | Deep standby interrupt flag register 2 | DPSIFR2 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C289h | SYSTEM | Deep standby interrupt flag register 3 | DPSIFR3 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C28Ah | SYSTEM | Deep standby interrupt edge register 0 | DPSIEGR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C28Bh | SYSTEM | Deep standby interrupt edge register 1 | DPSIEGR1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C28Ch | SYSTEM | Deep standby interrupt edge register 2 | DPSIEGR2 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C28Dh | SYSTEM | Deep standby interrupt edge register 3 | DPSIEGR3 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C290h | SYSTEM | Reset status register 0 | RSTSR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Resets |
| 0008 C291h | SYSTEM | Reset status register 1 | RSTSR1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C293h | SYSTEM | Main clock oscillator forced oscillation control register | MOFCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Clock Generation Circuit |
| 0008 C294h | SYSTEM | High-speed on-chip oscillator power supply control register | HOCOPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C296h | FLASH | Flash write erase protection register | FWEPROR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | ROM |
| 0008 C297h | SYSTEM | Voltage monitoring circuit control register | LVCMPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | LVDA |
| 0008 C298h | SYSTEM | Voltage detection level select register | LVDLVLR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C29Ah | SYSTEM | Voltage monitoring 1 circuit control register 0 | LVD1CR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C29Bh | SYSTEM | Voltage monitoring 2 circuit control register 0 | LVD2CR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C2A0h to 0008 C2BFh | SYSTEM | Deep standby backup register 0 to 31 | DPSBKR0 to 31 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C300h | ICU | Group 0 interrupt source register | GRP00 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | ICUb |
| 0008 C304h | ICU | Group 1 interrupt source register | GRP01 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C308h | ICU | Group 2 interrupt source register | GRP02 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C30Ch | ICU | Group 3 interrupt source register | GRP03 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C310h | ICU | Group 4 interrupt source register | GRP04 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C314h | ICU | Group 5 interrupt source register | GRP05 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C318h | ICU | Group 6 interrupt source register | GRP06 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C330h | ICU | Group 12 interrupt source register | GRP12 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C340h | ICU | Group 0 interrupt enable register | GEN00 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |

**Table 4.1 List of I/O Registers (Address Order) (39/50)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 000A 003Ah | USB0 | BEMP interrupt enable register | BEMPENB | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | USBa |
| 000A 003Ch | USB0 | SOF output configuration register | SOFCFG | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | |
| 000A 0040h | USB0 | Interrupt status register 0 | INTSTS0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | |
| 000A 0042h | USB0 | Interrupt status register 1 | INTSTS1 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | |
| 000A 0046h | USB0 | BRDY interrupt status register | BRDYSTS | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | |
| 000A 0048h | USB0 | NRDY interrupt status register | NRDYSTS | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | |
| 000A 004Ah | USB0 | BEMP interrupt status register | BEMPSTS | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | |
| 000A 004Ch | USB0 | Frame number register | FRMNUM | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | |
| 000A 004Eh | USB0 | Device state changing register | DVCHGR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | USBa |
| 000A 0050h | USB0 | USB address register | USBADDR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | |

**Table 4.1 List of I/O Registers (Address Order) (49/50)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 000C 0100h | ETHERC | ETHERC mode register | ECMR | 32 | 32 | 5, 6 PCLKA | — | ETHERC |
| 000C 0108h | ETHERC | Receive frame length register | RFLR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0110h | ETHERC | ETHERC status register | ECSR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0118h | ETHERC | ETHERC interrupt permission register | ECSIPR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0120h | ETHERC | PHY interface register | PIR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0128h | ETHERC | PHY status register | PSR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0140h | ETHERC | Random number generation counter upper limit setting register | RDMLR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0150h | ETHERC | IPG register | IPGR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0154h | ETHERC | Automatic PAUSE frame register | APR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0158h | ETHERC | Manual PAUSE frame register | MPR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0160h | ETHERC | PAUSE Frame receive counter register | RFCF | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0164h | ETHERC | Automatic PAUSE frame retransmit count register | TPAUSER | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0168h | ETHERC | PAUSE frame retransmit counter register | TPAUSECR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 016Ch | ETHERC | Broadcast frame receive count setting register | BCFRR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01C0h | ETHERC | MAC address high register | MAHR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01C8h | ETHERC | MAC address low register | MALR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01D0h | ETHERC | Transmit retry over counter register | TROCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01D4h | ETHERC | Delayed collision detect counter register | CDCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01D8h | ETHERC | Lost carrier counter register | LCCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01DCh | ETHERC | Carrier not detect counter register | CNDCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01E4h | ETHERC | CRC error frame receive counter register | CEFCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01E8h | ETHERC | Frame receive error counter register | FRECR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01ECh | ETHERC | Too-short frame receive counter register | TSFRCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01F0h | ETHERC | Too-long frame receive counter register | TLFRCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01F4h | ETHERC | Residual-bit frame receive counter register | RFCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01F8h | ETHERC | Multicast address frame receive counter register | MAFCR | 32 | 32 | 5, 6 PCLKA | — | |

**Table 5.5 DC Characteristics (4) (for G Version (+85 < Ta ≤ +105°C))**

Conditions: VCC = AVCC0 = VREFH = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

| Item | | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Supply current*1 | High-speed operating mode | Max.*2 | | $I_{CC}$*3 | — | — | 115 | mA | ICLK = 100 MHz<br>PCLKA = 100MHz<br>PCLKB = 50 MHz<br>FCLK = 50 MHz<br>BCLK = 100MHz |
| | | Normal *4 | Peripheral function: clock signal supplied*4 | | — | 52 | — | | |
| | | | Peripheral function: clock signal stopped*4 | | — | 40 | — | | |
| | | Sleep mode | | | — | 25 | 80 | | |
| | | All-module-clock-stop mode (reference value) | | | — | 20 | 53 | | |
| | | Increased by BGO operation*5 | | | — | 15 | — | | |
| | Low-speed operating mode 1*6 | | | | — | 4 | — | | ICLK = 1 MHz |
| | Low-speed operating mode 2 | | | | — | 1 | — | | ICLK = 32.768 kHz |
| | Software standby mode | | | | — | 0.2 | 9 | | |
| | Deep software standby mode | Power supplied to RAM and USB resume detecting unit | | | — | 22 | 200 | µA | |
| | | Power not supplied to RAM and USB resume detecting unit | Power-on reset circuit and low-power consumption function disabled | | — | 21 | 60 | | |
| | | | Power-on reset circuit and low-power consumption function enabled | | — | 6.2 | 28 | | |
| | Increase when the RTC is operating | | When a crystal oscillator for low clock loads is in use | | — | 1.0 | — | | |
| | | | When a crystal oscillator for standard clock loads is in use | | — | 3.0 | — | | |
| | RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate) | | When a crystal oscillator for low clock loads is in use | | — | 0.9 | — | | $V_{BATT}$ = 2.0 V, VCC = 0V |
| | | | | | — | 1.6 | — | | $V_{BATT}$ = 3.3 V, VCC = 0V |
| | | | When a crystal oscillator for standard clock loads is in use | | — | 1.7 | — | | $V_{BATT}$ = 2.0 V(for products with 100 pins or more), VBATT = 2.3 V (for the 64-pin product), VCC = 0V |
| | | | | | — | 3.3 | — | | $V_{BATT}$ = 3.3 V, VCC = 0V |
| Analog power supply current*7 | During 12-bit A/D conversion (including temperature sensor) | | | $I_{AVCC0}$ | — | 2.3 | 3.2 | mA | |
| | During 10-bit A/D conversion | | | $I_{VREFH}$*9 | — | 1.0 | 1.65 | mA | |
| | During D/A conversion (per unit) | | | | — | 0.7 | 1.0 | mA | |
| | Waiting for A/D, D/A conversion (all units)*10 | | | — | — | 25 | 35 | µA | |
| | A/D, D/A converter in standby mode (all units)*10 | | | | — | 0.1 | 5 | µA | |
| Reference power supply current | During 12-bit A/D conversion | | | $I_{VREFH0}$ | — | 0.6 | 0.7 | mA | |
| | Waiting for 12-bit A/D conversion (per unit) | | | | — | 0.5 | 0.6 | mA | |
| | 12-bit A/D converter in standby mode (per unit) | | | | — | 0.1 | 2.0 | µA | |
| RAM standby voltage | | | | $V_{RAM}$ | 2.7 | — | — | V | |
| VCC rising gradient | | | | SrVCC | 8.4 | — | 20000 | µs/V | |
| VCC falling gradient*8 | | | | SfVCC | 8.4 | — | — | µs/V | |

**Table 5.17 Bus Timing (packages with 100 pins or less)**

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V,
ICLK = 8 to 100 MHz, BCLK pin = 8 to 50 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, $I_{OH}$ = –1.0 mA, $I_{OL}$ = 1.0 mA, C = 30 pF
High drive output is selected by the drive capacity control register.

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 20 | ns | Figure 5.17 to Figure 5.22 |
| Byte control delay time | $t_{BCD}$ | — | 20 | ns | |
| CS# delay time | $t_{CSD}$ | — | 20 | ns | |
| ALE delay time | $t_{ALED}$ | — | 20 | ns | |
| RD# delay time | $t_{RSD}$ | — | 20 | ns | |
| Read data setup time | $t_{RDS}$ | 15 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 20 | ns | |
| Write data delay time | $t_{WDD}$ | — | 20 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 15 | — | ns | Figure 5.23 |
| WAIT# hold time | $t_{WTH}$ | 0 | — | ns | |

## 5.3.6 EXDMAC Timing

**Table 5.18 EXDMAC Timing**

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz, BCLK pin = 8 to 100 MHz, SDCLK pin = 8 to 50 MHz, $T_a = T_{opr}$
High drive output is selected by the drive capacity control register

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| EXDMAC | EDREQ setup time | $t_{EDRQS}$ | 20 | — | ns | Figure 5.31 |
| | EDREQ hold time | $t_{EDRQH}$ | 5 | — | ns | Figure 5.32 and Figure 5.33 |
| | EDACK delay time | $t_{EDACD}$ | — | 15 | ns | |

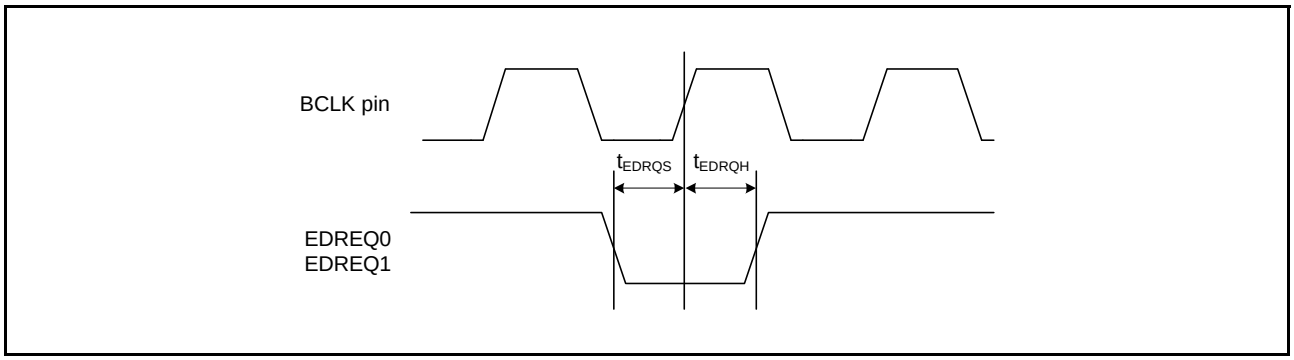



**Figure 5.31 EDREQ0 and EDREQ1 Input Timing**

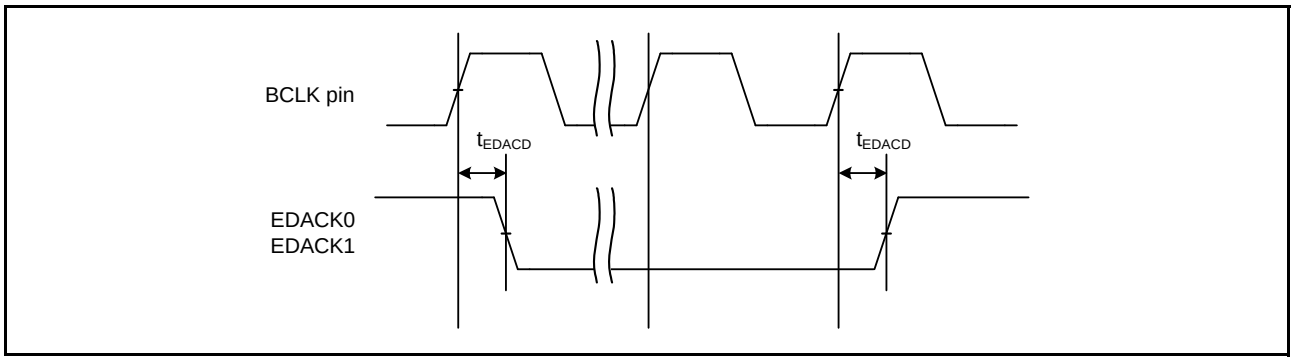



**Figure 5.32 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)**

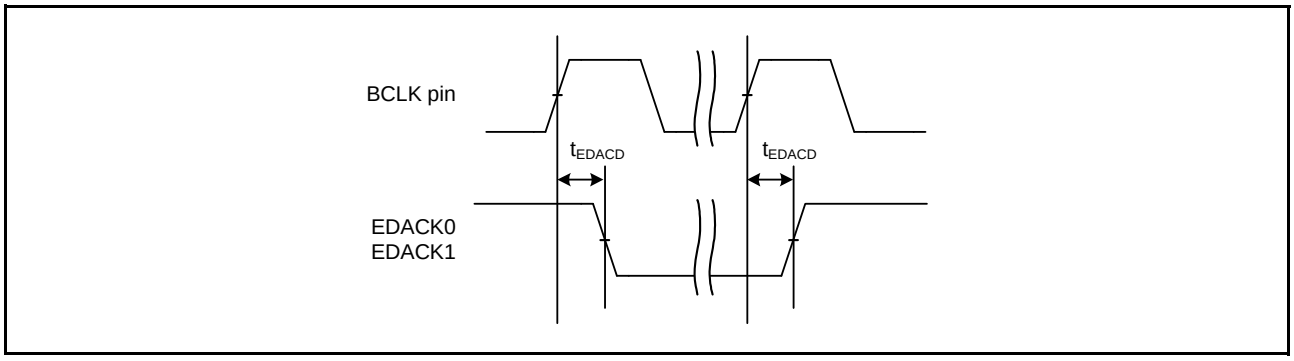



**Figure 5.33 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)**

### Table 5.23 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a = T_{opr}$
High drive output is selected by the drive capacity control register.

| Item | | Symbol | Min.*1,*2 | Max.* | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RIIC (Standard-mode, SMBus) ICFER.FMPE = 0 | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 1300 | — | ns | Figure 5.47 |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | — | 1000 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 1000 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 1000 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |
| RIIC (Fast-mode) | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 600 | — | ns | |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | 20 + 0.1$C_b$ | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | 20 + 0.1$C_b$ | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 300 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 300 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |

Note: $t_{IICcyc}$: RIIC internal reference clock (IICϕ) Cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. Cb is the total capacitance of the bus lines.

### Table 5.25 Timing of On-Chip Peripheral Modules (7)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
ICLK = 12.5 to 100 MHz, $T_a = T_{opr}$
High drive output is selected by the drive capacity control register.

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| ETHERC(RMII) | REF50CK cycle time | $T_{ck}$ | 20 | — | ns | Figure 5.48 to Figure 5.51 |
| | REF50CK frequency Typ. 50 MHz | — | — | 50 + 100ppm | MHz | |
| | REF50CK duty | — | 35 | 65 | % | |
| | REF50CK rise/fall time | $T_{ckr/ckf}$ | 0.5 | 3.5 | ns | |
| | RMII_xxxx*1 output delay time | $T_{co}$ | 2.5 | 15.0 | ns | |
| | RMII_xxxx*2 setup time | $T_{su}$ | 3 | — | ns | |
| | RMII_xxxx*2 hold time | $T_{hd}$ | 1 | — | ns | |
| | RMII_xxxx*1, *2 rise/fall time | Tr/Tf | 0.5 | 6 | ns | |
| | ET_WOL output delay time | $t_{WOLd}$ | 1 | 23.5 | ns | Figure 5.52 |
| ETHERC(MII) | ET_TX_CLK cycle time | $t_{Tcyc}$ | 40 | — | ns | — |
| | ET_TX_EN output delay time | $t_{TENd}$ | 1 | 20 | ns | Figure 5.53 |
| | ET_ETXD0 to ET_ETXD3 output delay time | $t_{MTDd}$ | 1 | 20 | ns | |
| | ET_CRS setup time | $t_{CRSs}$ | 10 | — | ns | |
| | ET_CRS hold time | $t_{CRSh}$ | 10 | — | ns | |
| | ET_COL setup time | $t_{COLs}$ | 10 | — | ns | Figure 5.54 |
| | ET_COL hold time | $t_{COLh}$ | 10 | — | ns | |
| | ET_RX_CLK cycle time | $t_{TRcyc}$ | 40 | — | ns | — |
| | ET_RX_DV setup time | $t_{RDVs}$ | 10 | | ns | Figure 5.55 |
| | ET_RX_DV hold time | $t_{RDVh}$ | 10 | — | ns | |
| | ET_ERXD0 to ET_ERXD3 setup time | $t_{MRDs}$ | 10 | — | ns | |
| | ET_ERXD0 to ET_ERXD3 hold time | $t_{MRDh}$ | 10 | — | ns | |
| | ET_RX_ER setup time | $t_{RERs}$ | 10 | — | ns | Figure 5.56 |
| | ET_RX_ER hold time | $t_{RESh}$ | 10 | — | ns | |
| | ET_WOL output delay time | $t_{WOLd}$ | 1 | 23.5 | ns | Figure 5.57 |

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0.
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

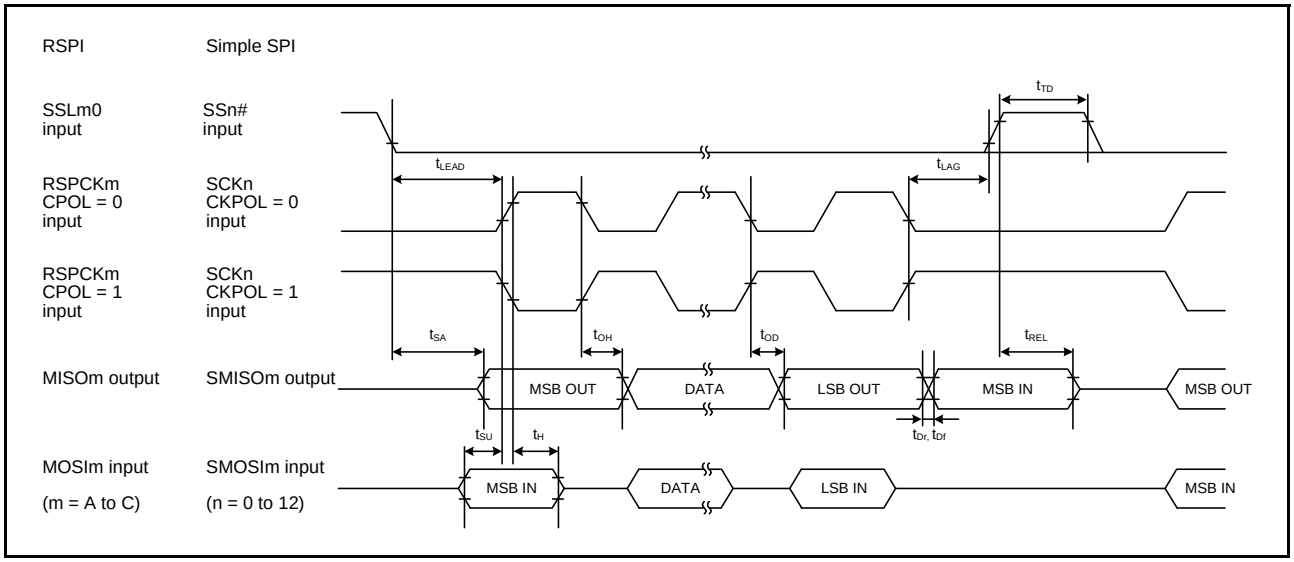



**Figure 5.45 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)**

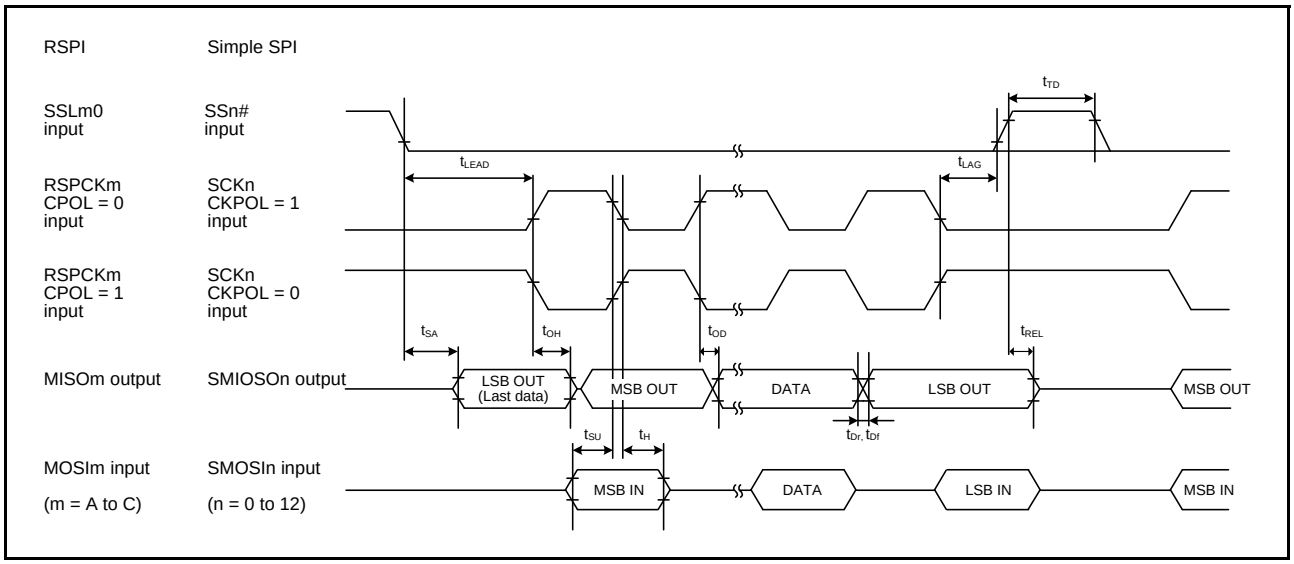
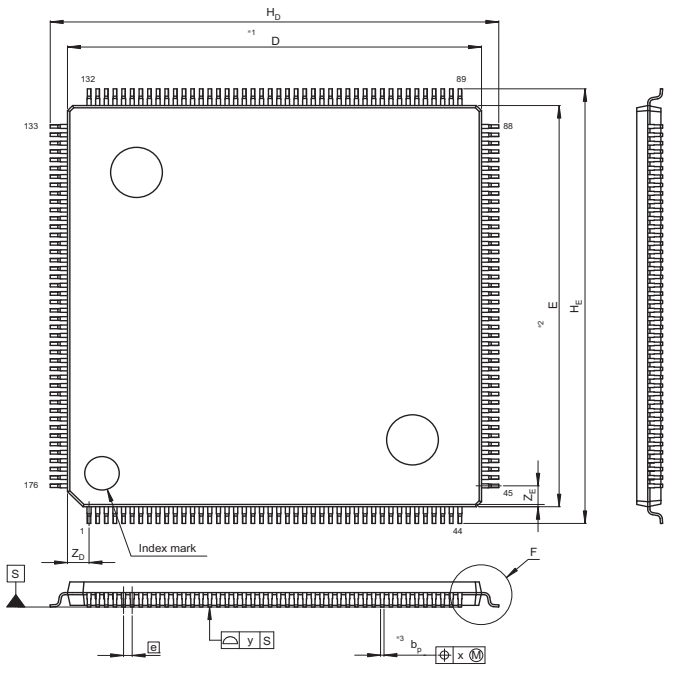
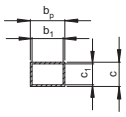


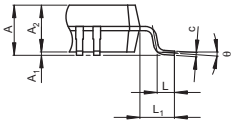

**Figure 5.46 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)**

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFQFP176-24x24-0.50 | PLQP0176KB-A | 176P6Q-A/FP-176E/FP-176EV | 1.8g |




Terminal cross section




Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 23.9 | 24.0 | 24.1 |
| E | 23.9 | 24.0 | 24.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 25.8 | 26.0 | 26.2 |
| $H_E$ | 25.8 | 26.0 | 26.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

Figure C 176-pin LQFP (PLQP0176KB-A)