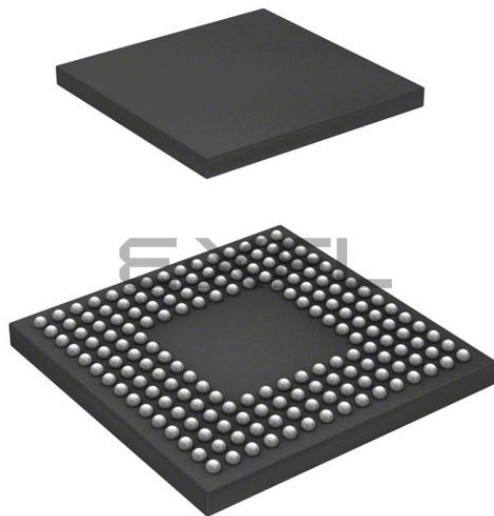




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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631acdbg-u0

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and table 1.2 gives a comparison of the functions of products in different packages.

Table 1.1 is for products with the greatest number of functions, so numbers of peripheral modules and channels will differ in accord with the package. For details, see Table 1.2, Comparison of Functions for Different Packages in the RX63N/RX631 Group.

Table 1.1 Outline of Specifications (1/6)

Classification	Module/Function	Description
CPU	CPU	- Maximum operating frequency: 100 MHz 32-bit RX CPU - Minimum instruction execution time: One instruction per state (cycle of the system clock) - Address space: 4-Gbyte linear - Register set of the CPU - General purpose: Sixteen 32-bit registers - Control: Nine 32-bit registers - Accumulator: One 64-bit register - Basic instructions: 73 - Floating-point instructions: 8 - DSP instructions: 9 - Addressing modes: 10 - Data arrangement - Instructions: Little endian - Data: Selectable as little endian or big endian - On-chip 32-bit multiplier: 32 x 32 → 64 bits - On-chip divider: 32 / 32 → 32 bits - Barrel shifter: 32 bits - Memory protection unit (MPU)
	FPU	- Single precision (32-bit) floating point - Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	- Capacity: ROMless, 256 Kbytes, 384 Kbytes, 512 Kbytes, 768 Kbytes, 1 Mbyte, 1.5 Mbytes, 2 Mbytes 100 MHz, no-wait access - On-board programming: Four types - Off-board programming (parallel programmer mode) (for products with 100 pins or more)
	RAM	- Capacity: 64 Kbytes, 128 Kbytes, 192 Kbytes, 256 Kbytes 100 MHz, no-wait access
	E2 data flash	Capacity: 32 Kbytes Programming/erasing: 100,000 times
MCU operating modes		Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	- Main clock oscillator, subclock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDG-dedicated on-chip oscillator - Main-clock oscillation stoppage detection - Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLK), FlashIF clock (FCLK) and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLK): Up to 50 MHz Flash IF run in synchronization with the flashIF clock (FCLK): Up to 50 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 50 MHz
Reset		RES# pin reset, power-on reset, voltage-monitoring reset, independent watchdog timer reset, watchdog timer reset, deep software standby reset, and software reset
Voltage detection circuit		When the voltage on VCC passes the voltage detection level (Vdet), an internal reset or internal interrupt is generated.

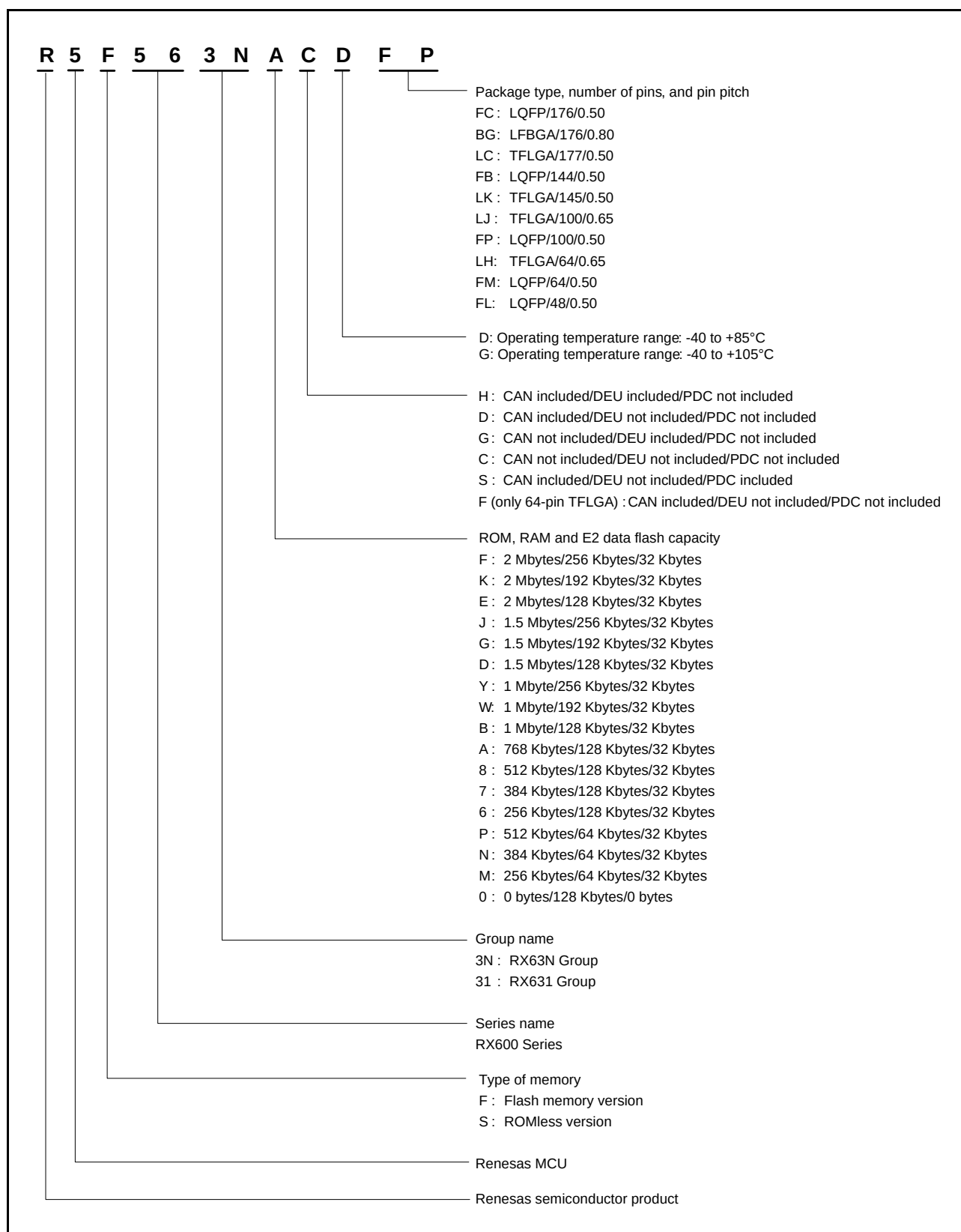


Figure 1.1 How to Read the Product Part No.

1.3 Block Diagram

Figure 1.2 shows a block diagram.

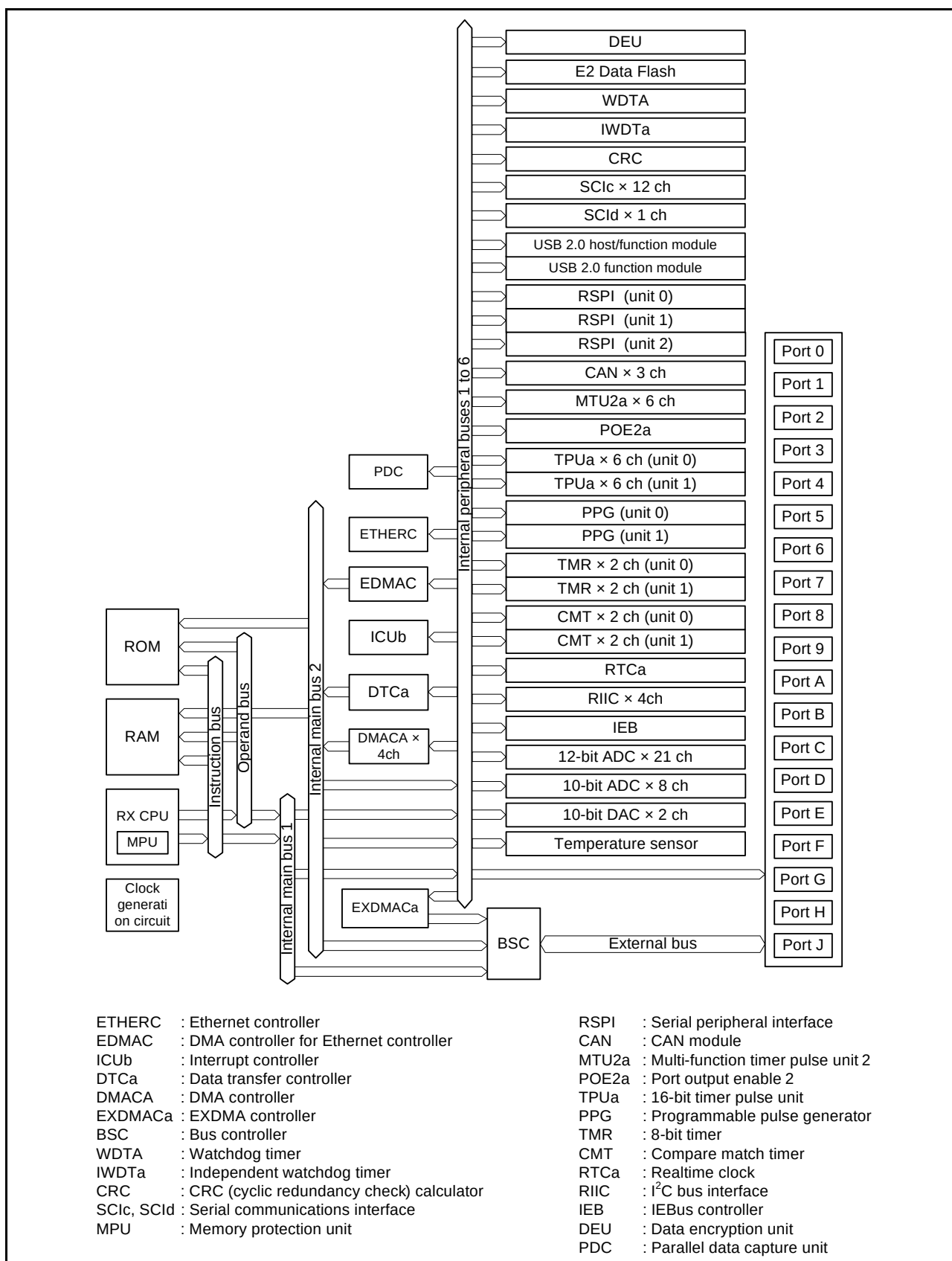


Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/6)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin. When the battery backup function is not to be used, connect it to the VCC pin.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the clock dedicated for the SDRAM.
	XCOUT	Output	Input/output pins for the subclock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCIN	Input	
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.
On-chip emulator	FINEC	Input	Fine interface clock pin
	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	This pin outputs the clock for synchronization with the trace data.
	TRCLK	Output	
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0 to TRDATA3	Output	These pins output the trace information.
Address bus	A0 to A23	Output	Output pins for the address.
Data bus	D0 to D31	I/O	Input and output pins for the bidirectional data bus.
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	PE3	PE4	VSS	PE6	P67	PA2	PA4	PA7	PB1	PB5	VSS	VCC	P74	13
12	PE1	PE2	P70	PE5	P65	PA1	VCC	PB0	PB2	PB6	P73	PC1	P75	12
11	P62	P61	PE0	VCC	P66	VSS	PA6	P71	PB4	PB7	PC2	PC0	PC3	11
10	VSS	VCC	P63	PE7	PA0	PA3	PA5	P72	PB3	P76	PC4	P77	P82	10
9	PD6	PD4	PD7	P64	RX63N Group RX631 Group PTLG0145KA-A (145-pin TFLGA) (Top perspective view)					P80	PC5	P81	PC7	9
8	PD2	PD0	PD3	P60						VCC	P83	PC6	VSS	8
7	P92	P91	PD1	PD5						P51	P52	P50	P55	7
6	P90	P47	VSS	P93						P53	P56	VSS_ USB	USB0_ DP	6
5	P45	P43	P46	VCC	P44					P54	P13	VCC_ USB	USB0_ DM	5
4	P42	VREFL0	P41	P01	EMLE	VBATT	BSCANP	P35	P30	P15	P24	P12	P14	4
3	P40	P05	VREFH0	P03	PJ5	PJ3	MD/ FINED	VSS	P32	P31	P16	P86	P87	3
2	P07	AVCC0	P02	PF5	VCL	XCOUT	RES#	VCC	P33	P26	P23	P17	P20	2
1	AVSS0	VREFH	VREFL	P00	VSS	XCIN	XTAL	EXTAL	P34	P27	P25	P22	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pins and Pin Functions (145-Pin TFLGA).

Figure 1.6 Pin Assignment (145-Pin TFLGA)

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (3/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
H12		PB0	A8	MTIOC5W/TIOCA3/PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA/T_ERXD1/ RMII_RXD1	IRQ12	
H13		PA7	A7	TIOCB2/PO23	MISOA/ET_WOL		
J1	TRST#	P34		MTIOC0A/TMC13/PO12/ POE2#	SCK6/SCK0/ USB0_DPRPD	IRQ4	
J2		P33		MTIOC0D/TIOCD0/ TMR13/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0/PCKO	IRQ3-DS	
J3		P32		MTIOC0C/TIOCC0/ TMO3/PO10/RTCOU0/ RTIC12	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC	IRQ2-DS	
J4	TDI	P30		MTIOC4B/TMR13/PO8/ RTIC10/POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
J10		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	SCK4/SCK6/ET_RX_ER/ RMII_RX_ER		
J11		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/SS9#/ ET_TX_EN/RMII_TXD_EN		
J12		PB2	A10	TIOCC3/TCLKC/PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET_RX_CLK/REF50CK		
J13		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6/ ET_ERXD0/RMII_RXD0	IRQ4-DS	
K1	TCK/FINEC	P27	CS7#	MTIOC2B/TMC13/PO7	SCK1/RSPCKB		
K2	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
K3	TMS	P31		MTIOC4D/TMC12/PO9/ RTIC11	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
K4		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/PIXD0	IRQ5	
K5	TRDATA2	P54	ALE/EDACK0	MTIOC4B/TMC11	CTS2#/RTS2#/SS2#/ CTX1/ET_LINKSTA		
K6		P53*1	BCLK				
K7		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
K8	VCC						
K9	TRDATA0	P80	EDREQ0	MTIOC3B/PO26	SCK10/ET_TX_EN/ RMII_TXD_EN		
K10		P76	CS6#	PO22	RXD11/SMISO11/SSCL11/ ET_RX_CLK/REF50CK		
K11		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/SMOSI9/SSDA9/ ET_CRS/RMII_CRS_DV		
K12		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/SMISO9/SSCL9/ ET_ETXD1/RMII_TXD1		
K13		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1#	SCK9/ET_ETXD0/ RMII_TXD0		
L1		P25	CS5#/EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC		ADTRG0#
L2		P23	EDACK0	MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7		

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (4/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
H4		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13	RXD1/SCK3/ SMISO1/SSCL1/ CRX1-DS	IRQ5	
H5		P55	WAIT#/ EDREQ0	MTIOC4D/ TMO3	CRX1/ET_EXOUT	IRQ10	
H6		P54	ALE/EDACK0	MTIOC4B/ TMCI1	CTS2#/RTS2#/ SS2#/CTX1/ ET_LINKSTA		
H7		PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31	TXD8/SMOSI8/ SSDA8/MISOA/ ET_COL	IRQ14	
H8		PC6	A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/PO30	RXD8/SMISO8/ SSCL8/MOSIA/ ET_ETXD3	IRQ13	
H9		PB6	A14	MTIOC3D/ TIOCA5/PO30	RXD9/SMISO9/ SSCL9/ET_ETXD1/ RMII_TXD1		
H10		PB7	A15	MTIOC3B/ TIOCB5/PO31	TXD9/SMOSI9/ SSDA9/ET_CRS/ RMII_CRS_DV		
J1		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN		
J2		P21		MTIOC1B/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN	IRQ9	
J3		P17		MTIOC3A/ MTIOC3B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ MISOA/SDA2-DS/ IETXD	IRQ7	ADTRG#
J4		P13		MTIOC0B/ TIOCA5/TMO3/ PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]	IRQ3	ADTRG#
J5	VSS_USB						
J6	VCC_USB						
J7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1		
J8		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	SCK5/CTS8#/ RTS8#/SS8#/ SSLA0/ET_TX_CLK		
J9		PC0	A16	MTIOC3C/ TCLKC/PO17	CTS5#/RTS5#/ SS5#/SSLA1/ ET_ERXD3	IRQ14	
J10		PC1	A17	MTIOC3A/ TCLKD/PO18	SCK5/SSLA2/ ET_ERXD2	IRQ12	
K1		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/ RTS0#/SMOSI3/ SS0#/SSDA3/ USB0_DPUPE		

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

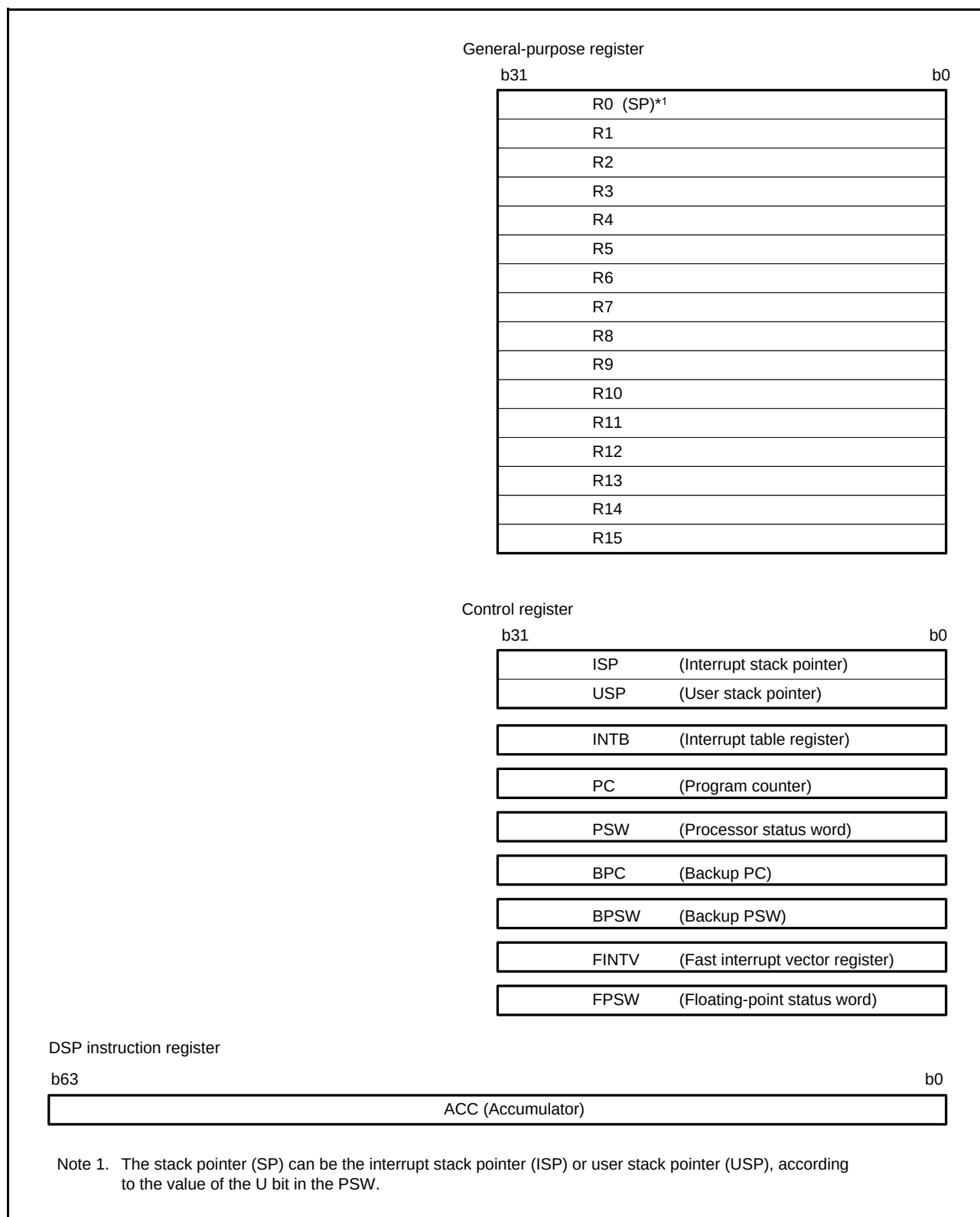


Figure 2.1 Register Set of the CPU

Table 4.1 List of I/O Registers (Address Order) (12/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7322h	ICU	Interrupt source priority register 034	IPR034	8	8	2	ICLK	ICUb
0008 7323h	ICU	Interrupt source priority register 035	IPR035	8	8	2	ICLK	
0008 7324h	ICU	Interrupt source priority register 036	IPR036	8	8	2	ICLK	
0008 7325h	ICU	Interrupt source priority register 037	IPR037	8	8	2	ICLK	
0008 7326h	ICU	Interrupt source priority register 038	IPR038	8	8	2	ICLK	
0008 7327h	ICU	Interrupt source priority register 039	IPR039	8	8	2	ICLK	
0008 732Ah	ICU	Interrupt source priority register 042	IPR042	8	8	2	ICLK	
0008 732Dh	ICU	Interrupt source priority register 045	IPR045	8	8	2	ICLK	
0008 7330h	ICU	Interrupt source priority register 048	IPR048	8	8	2	ICLK	
0008 7334h	ICU	Interrupt source priority register 052	IPR052	8	8	2	ICLK	
0008 7338h	ICU	Interrupt source priority register 056	IPR056	8	8	2	ICLK	
0008 733Eh	ICU	Interrupt source priority register 062	IPR062	8	8	2	ICLK	
0008 7340h	ICU	Interrupt source priority register 064	IPR064	8	8	2	ICLK	
0008 7341h	ICU	Interrupt source priority register 065	IPR065	8	8	2	ICLK	
0008 7342h	ICU	Interrupt source priority register 066	IPR066	8	8	2	ICLK	
0008 7343h	ICU	Interrupt source priority register 067	IPR067	8	8	2	ICLK	
0008 7344h	ICU	Interrupt source priority register 068	IPR068	8	8	2	ICLK	
0008 7345h	ICU	Interrupt source priority register 069	IPR069	8	8	2	ICLK	
0008 7346h	ICU	Interrupt source priority register 070	IPR070	8	8	2	ICLK	
0008 7347h	ICU	Interrupt source priority register 071	IPR071	8	8	2	ICLK	
0008 7348h	ICU	Interrupt source priority register 072	IPR072	8	8	2	ICLK	
0008 7349h	ICU	Interrupt source priority register 073	IPR073	8	8	2	ICLK	
0008 734Ah	ICU	Interrupt source priority register 074	IPR074	8	8	2	ICLK	
0008 734Bh	ICU	Interrupt source priority register 075	IPR075	8	8	2	ICLK	
0008 734Ch	ICU	Interrupt source priority register 076	IPR076	8	8	2	ICLK	
0008 734Dh	ICU	Interrupt source priority register 077	IPR077	8	8	2	ICLK	
0008 734Eh	ICU	Interrupt source priority register 078	IPR078	8	8	2	ICLK	
0008 734Fh	ICU	Interrupt source priority register 079	IPR079	8	8	2	ICLK	
0008 735Ah	ICU	Interrupt source priority register 090	IPR090	8	8	2	ICLK	
0008 735Bh	ICU	Interrupt source priority register 091	IPR091	8	8	2	ICLK	
0008 735Ch	ICU	Interrupt source priority register 092	IPR092	8	8	2	ICLK	
0008 735Dh	ICU	Interrupt source priority register 093	IPR093	8	8	2	ICLK	
0008 7362h	ICU	Interrupt source priority register 098	IPR098	8	8	2	ICLK	
0008 7366h	ICU	Interrupt source priority register 102	IPR102	8	8	2	ICLK	
0008 736Ah	ICU	Interrupt source priority register 106	IPR106	8	8	2	ICLK	
0008 736Bh	ICU	Interrupt source priority register 107	IPR107	8	8	2	ICLK	
0008 736Ch	ICU	Interrupt source priority register 108	IPR108	8	8	2	ICLK	
0008 736Dh	ICU	Interrupt source priority register 109	IPR109	8	8	2	ICLK	
0008 736Eh	ICU	Interrupt source priority register 110	IPR110	8	8	2	ICLK	
0008 736Fh	ICU	Interrupt source priority register 111	IPR111	8	8	2	ICLK	
0008 7370h	ICU	Interrupt source priority register 112	IPR112	8	8	2	ICLK	
0008 7372h	ICU	Interrupt source priority register 114	IPR114	8	8	2	ICLK	
0008 737Ah	ICU	Interrupt source priority register 122	IPR122	8	8	2	ICLK	
0008 737Eh	ICU	Interrupt source priority register 126	IPR126	8	8	2	ICLK	
0008 7382h	ICU	Interrupt source priority register 130	IPR130	8	8	2	ICLK	
0008 7384h	ICU	Interrupt source priority register 132	IPR132	8	8	2	ICLK	
0008 7386h	ICU	Interrupt source priority register 134	IPR134	8	8	2	ICLK	
0008 738Ah	ICU	Interrupt source priority register 138	IPR138	8	8	2	ICLK	
0008 738Ch	ICU	Interrupt source priority register 140	IPR140	8	8	2	ICLK	
0008 738Eh	ICU	Interrupt source priority register 142	IPR142	8	8	2	ICLK	
0008 7392h	ICU	Interrupt source priority register 146	IPR146	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (49/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000C 0100h	ETHERC	ETHERC mode register	ECMR	32	32	5, 6 PCLKA	—	ETHERC
000C 0108h	ETHERC	Receive frame length register	RFLR	32	32	5, 6 PCLKA	—	
000C 0110h	ETHERC	ETHERC status register	ECSR	32	32	5, 6 PCLKA	—	
000C 0118h	ETHERC	ETHERC interrupt permission register	ECSIPR	32	32	5, 6 PCLKA	—	
000C 0120h	ETHERC	PHY interface register	PIR	32	32	5, 6 PCLKA	—	
000C 0128h	ETHERC	PHY status register	PSR	32	32	5, 6 PCLKA	—	
000C 0140h	ETHERC	Random number generation counter upper limit setting register	RDMLR	32	32	5, 6 PCLKA	—	
000C 0150h	ETHERC	IPG register	IPGR	32	32	5, 6 PCLKA	—	
000C 0154h	ETHERC	Automatic PAUSE frame register	APR	32	32	5, 6 PCLKA	—	
000C 0158h	ETHERC	Manual PAUSE frame register	MPR	32	32	5, 6 PCLKA	—	
000C 0160h	ETHERC	PAUSE Frame receive counter register	RFCF	32	32	5, 6 PCLKA	—	
000C 0164h	ETHERC	Automatic PAUSE frame retransmit count register	TPAUSER	32	32	5, 6 PCLKA	—	
000C 0168h	ETHERC	PAUSE frame retransmit counter register	TPAUSECR	32	32	5, 6 PCLKA	—	
000C 016Ch	ETHERC	Broadcast frame receive count setting register	BCFR	32	32	5, 6 PCLKA	—	
000C 01C0h	ETHERC	MAC address high register	MAHR	32	32	5, 6 PCLKA	—	
000C 01C8h	ETHERC	MAC address low register	MALR	32	32	5, 6 PCLKA	—	
000C 01D0h	ETHERC	Transmit retry over counter register	TROCR	32	32	5, 6 PCLKA	—	
000C 01D4h	ETHERC	Delayed collision detect counter register	CDCR	32	32	5, 6 PCLKA	—	
000C 01D8h	ETHERC	Lost carrier counter register	LCCR	32	32	5, 6 PCLKA	—	
000C 01DCh	ETHERC	Carrier not detect counter register	CNDCR	32	32	5, 6 PCLKA	—	
000C 01E4h	ETHERC	CRC error frame receive counter register	CEFCR	32	32	5, 6 PCLKA	—	
000C 01E8h	ETHERC	Frame receive error counter register	FRECR	32	32	5, 6 PCLKA	—	
000C 01ECh	ETHERC	Too-short frame receive counter register	TSFRCR	32	32	5, 6 PCLKA	—	
000C 01F0h	ETHERC	Too-long frame receive counter register	TLFRCR	32	32	5, 6 PCLKA	—	
000C 01F4h	ETHERC	Residual-bit frame receive counter register	RFCR	32	32	5, 6 PCLKA	—	
000C 01F8h	ETHERC	Multicast address frame receive counter register	MAFCR	32	32	5, 6 PCLKA	—	

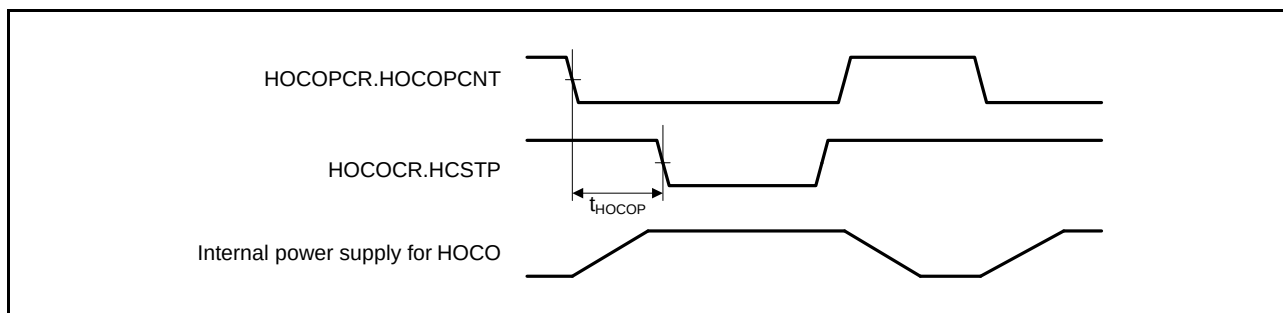


Figure 5.9 HOCO Power Supply Control Timing

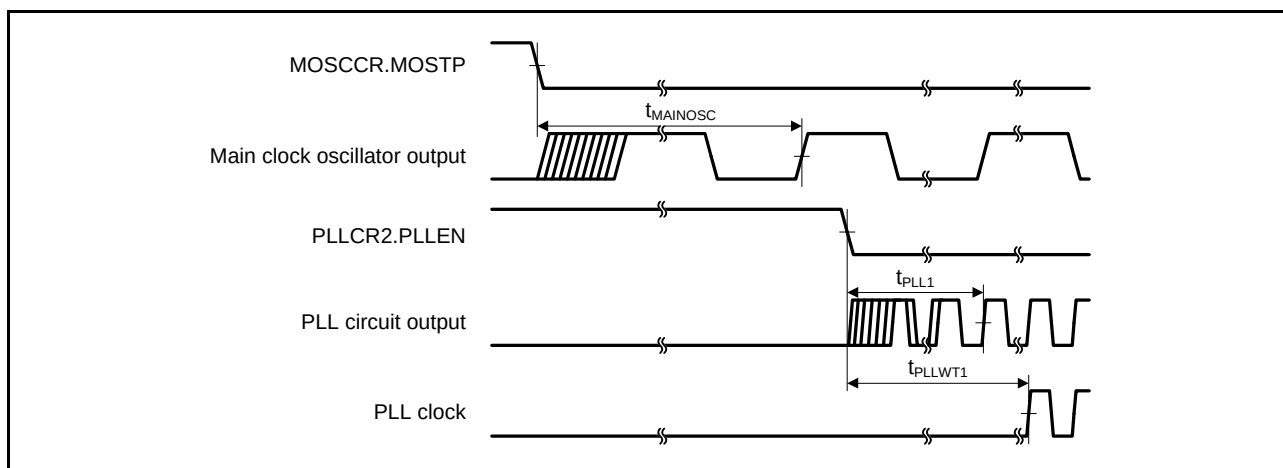


Figure 5.10 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

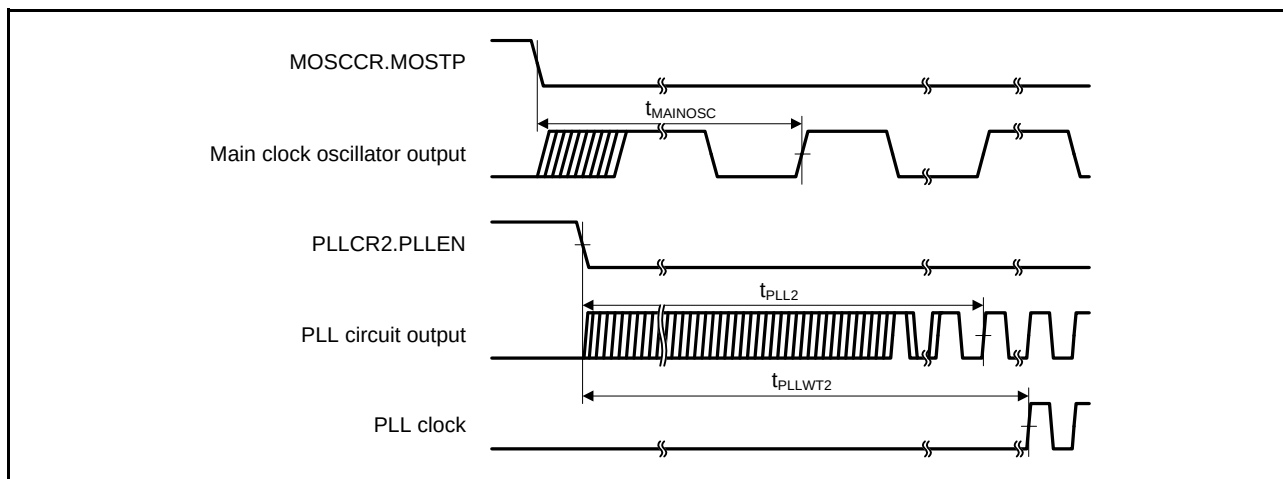


Figure 5.11 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

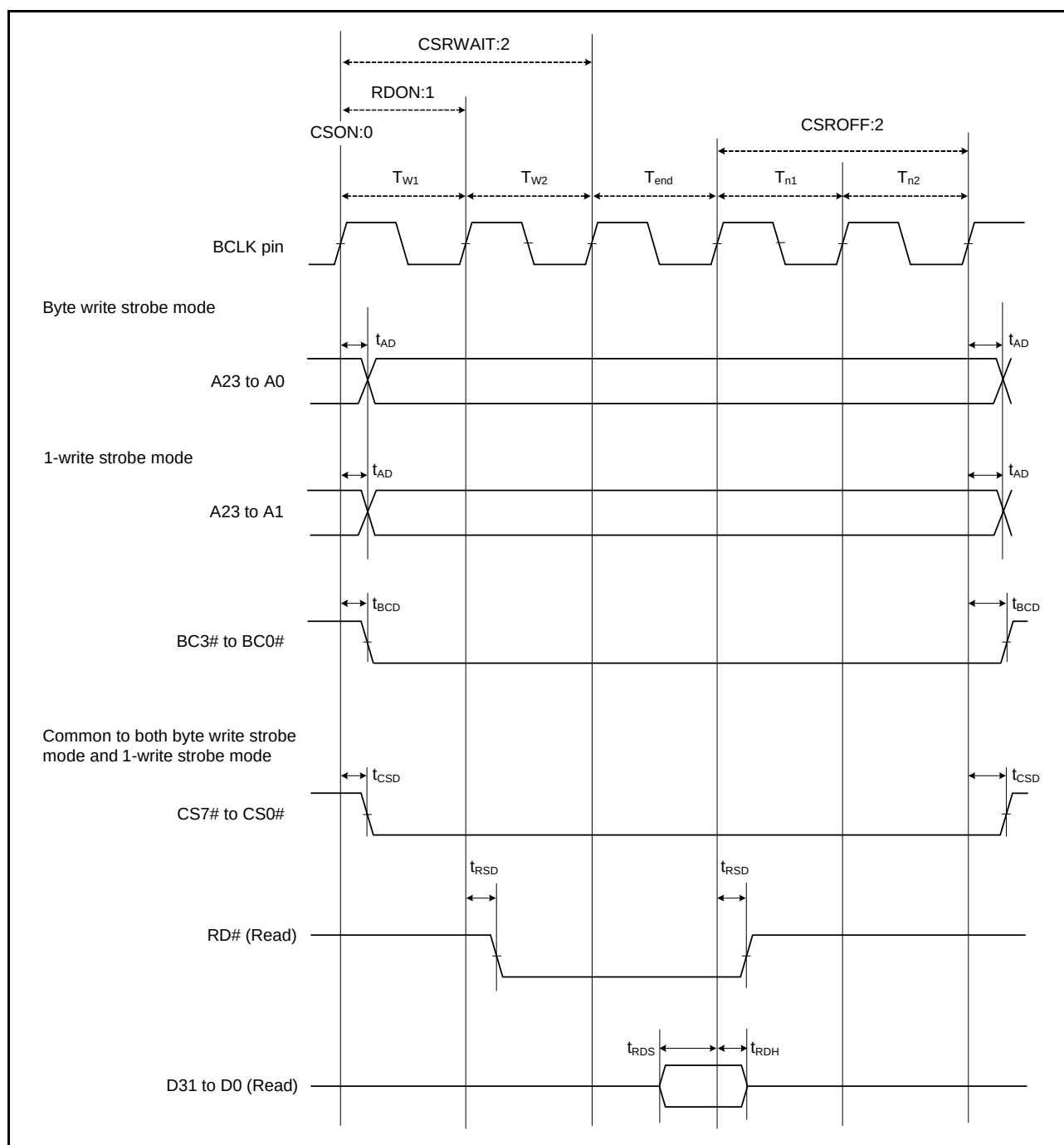
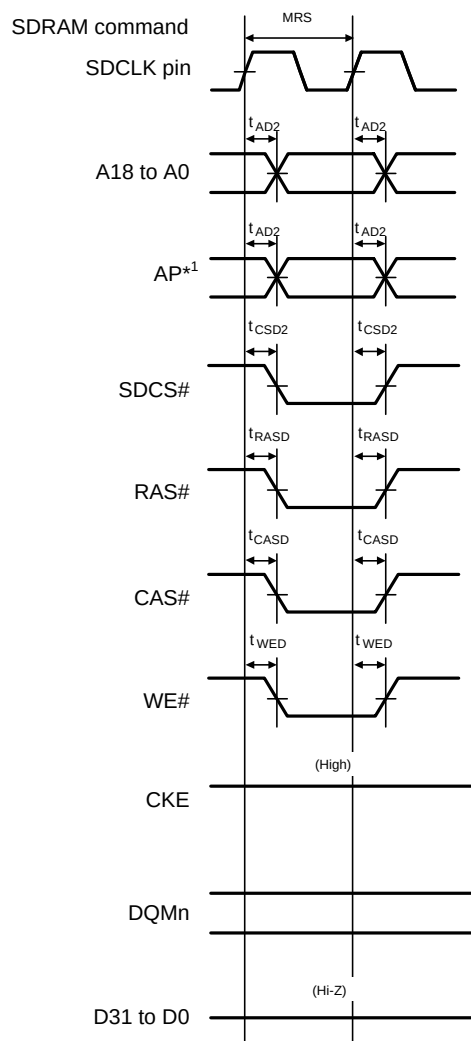


Figure 5.19 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.29 SDRAM Space Mode Register Set Bus Timing

Table 5.24 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

PCLK = 8 to 50 MHz

 $T_a = T_{opr}$

High drive output is selected by the drive capacity control register.

Item		Symbol	Min.*1, *2	Max.*1	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 240$	—	ns	Figure 5.47
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	120	ns	
	SCL, SDA input fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 120$	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 120$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	
Simple IIC (Standard-mode)	SDA input rise time	t_{Sr}	—	1000	ns	
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) Cycle, t_{Pcyc} : PCLK cycle

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

Note 2. C_b indicates the total capacity of the bus line.

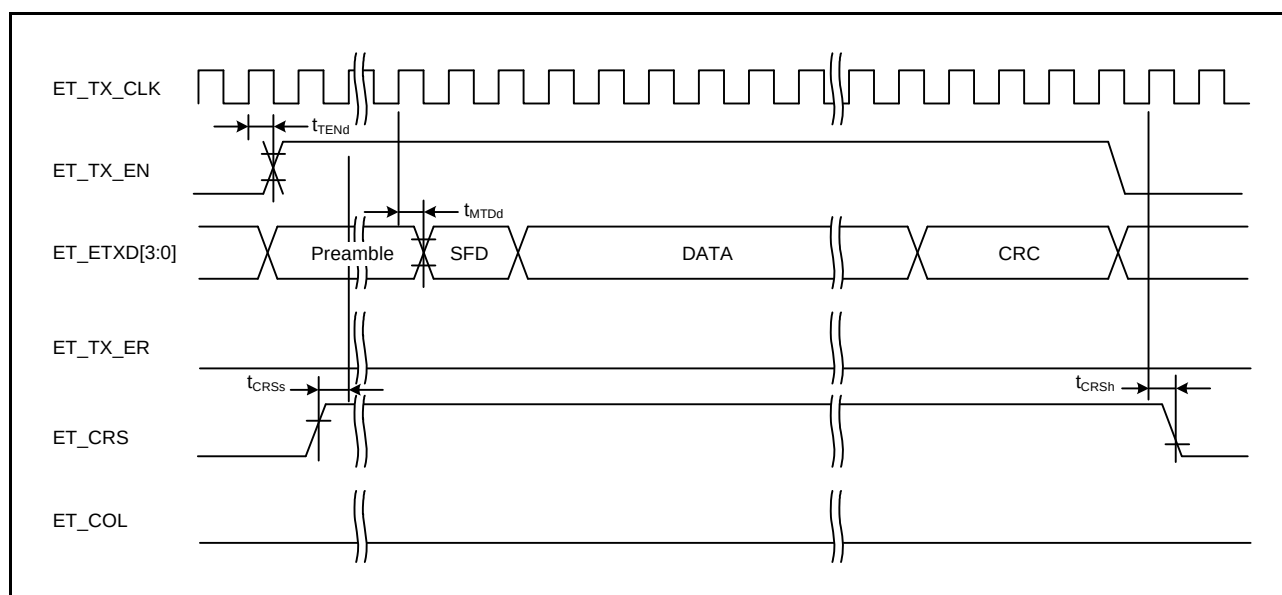


Figure 5.53 MII Transmission Timing (Normal Operation)

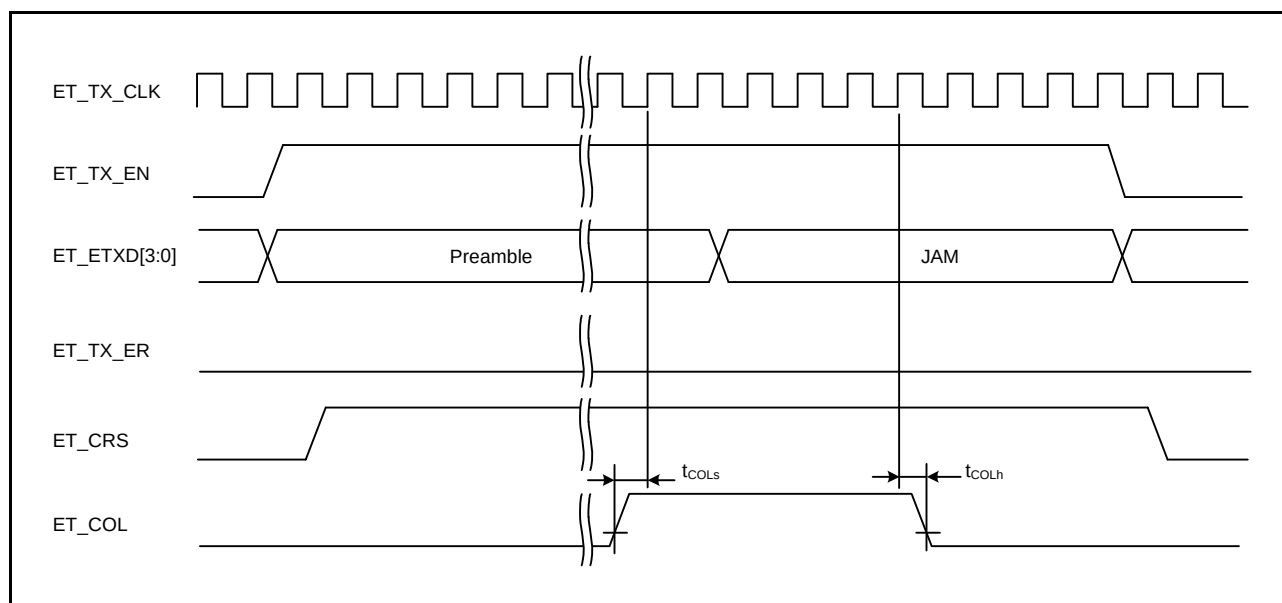


Figure 5.54 MII Transmission Timing (Conflict Occurrence)

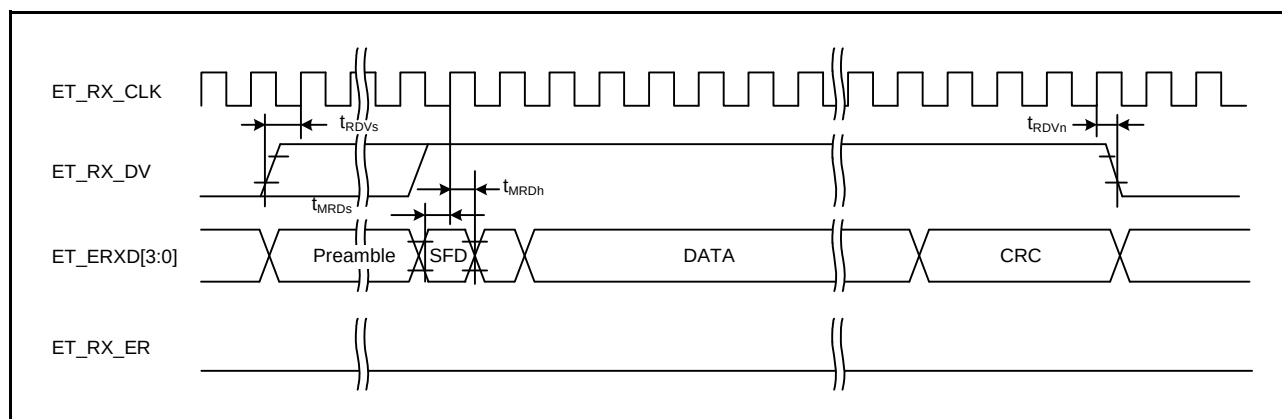
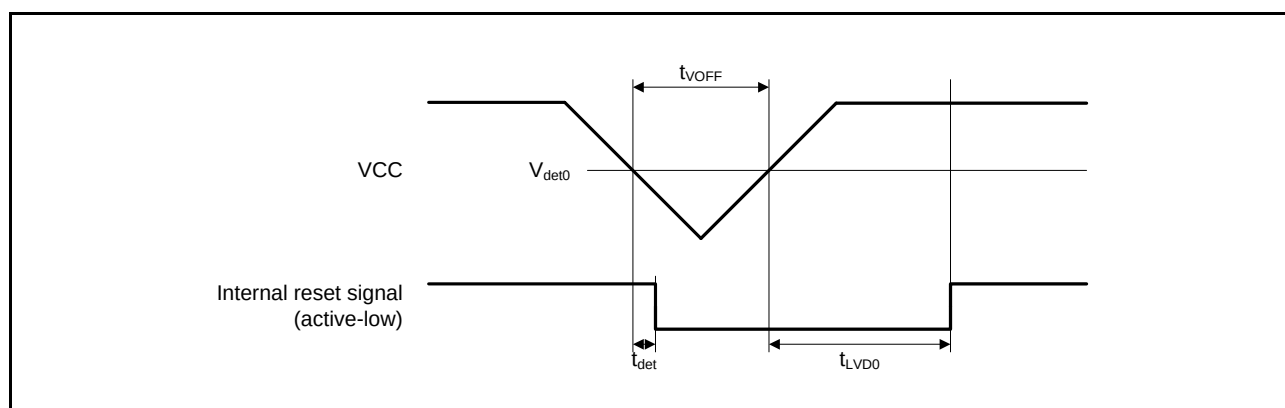
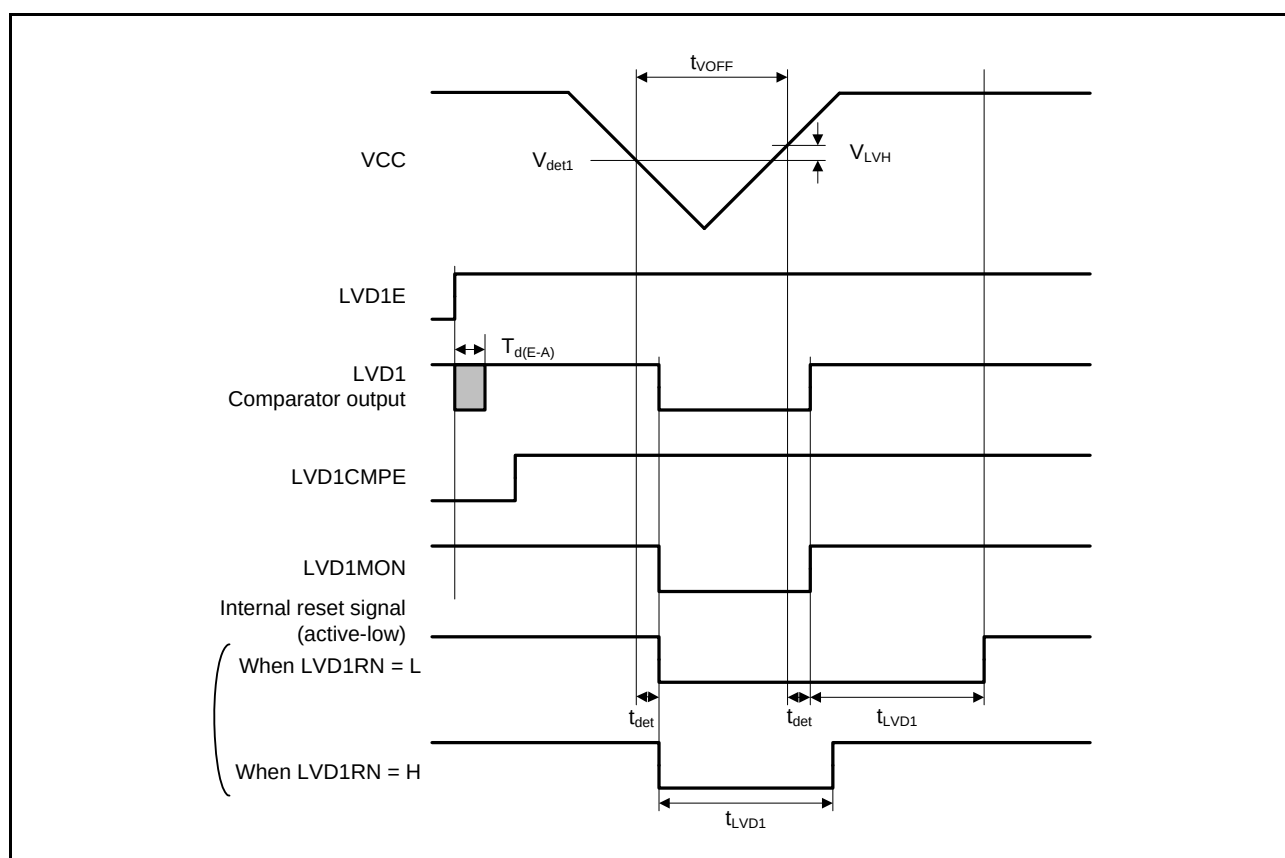


Figure 5.55 MII Reception Timing (Normal Operation)

Figure 5.64 Voltage Detection Circuit Timing (V_{det0})Figure 5.65 Voltage Detection Circuit Timing (V_{det1})

5.10 Battery Backup Function Characteristics

Table 5.35 Battery Backup Function Characteristics

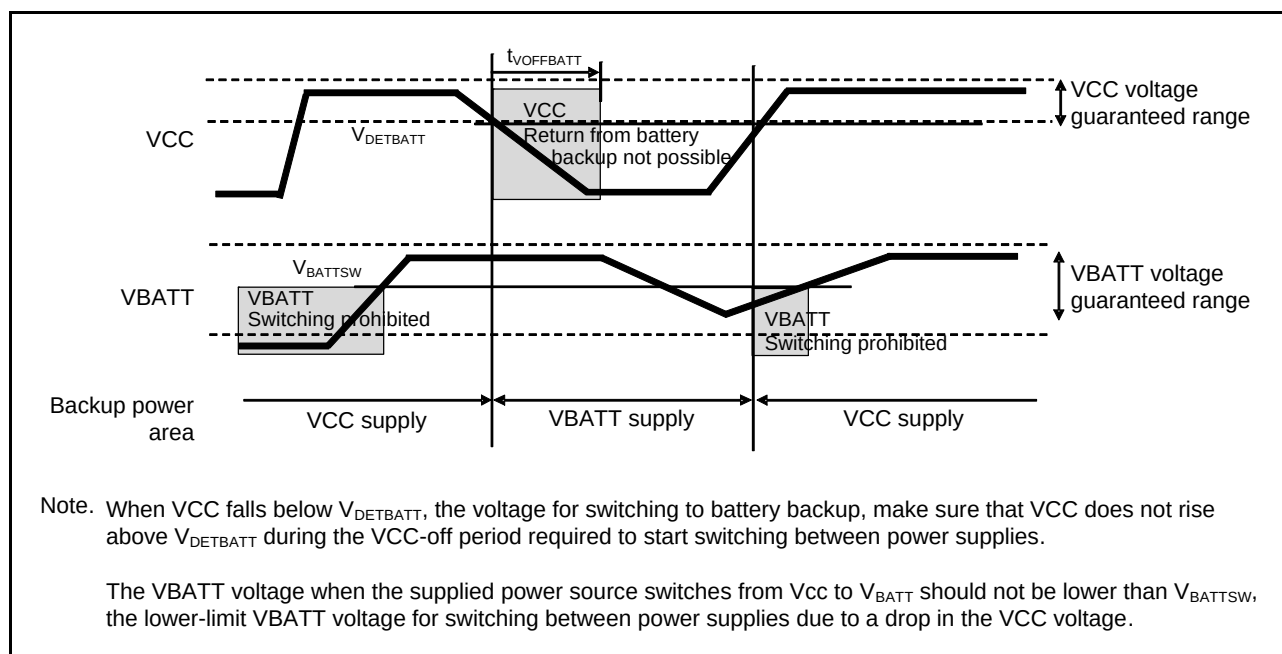
Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$, $V_{BATT} = 2.0$ to 3.6 V (for products with 100 pins or more), $V_{BATT} = 2.3$ to 3.6 V (for the 64-pin product)

$VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V

$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 5.68
Lower-limit V_{BATT} voltage for power supply switching due to VCC voltage drop	V_{BATTSW}	2.70	—	—		
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	—	—	μs	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

**Figure 5.68 Battery Backup Function Characteristics**

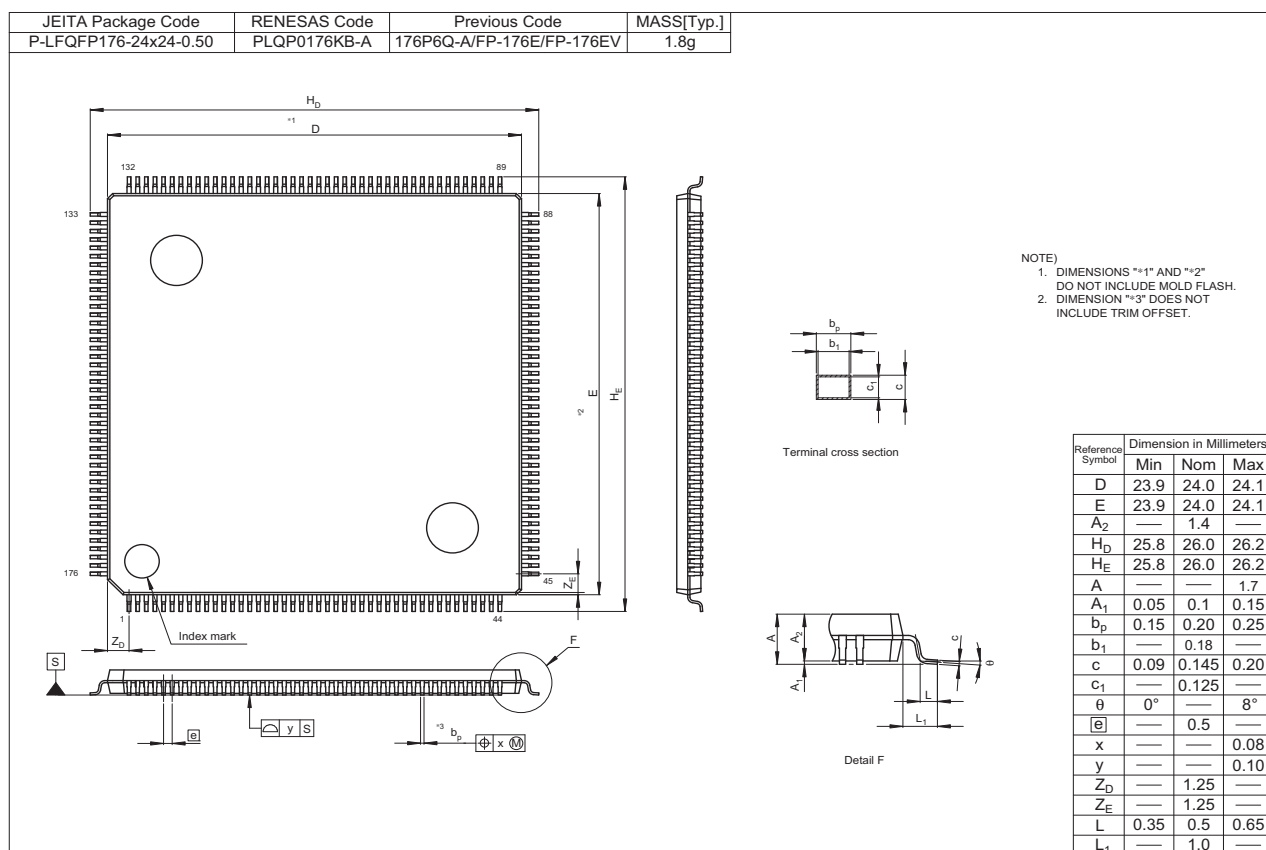


Figure C 176-pin LQFP (PLQP0176KB-A)

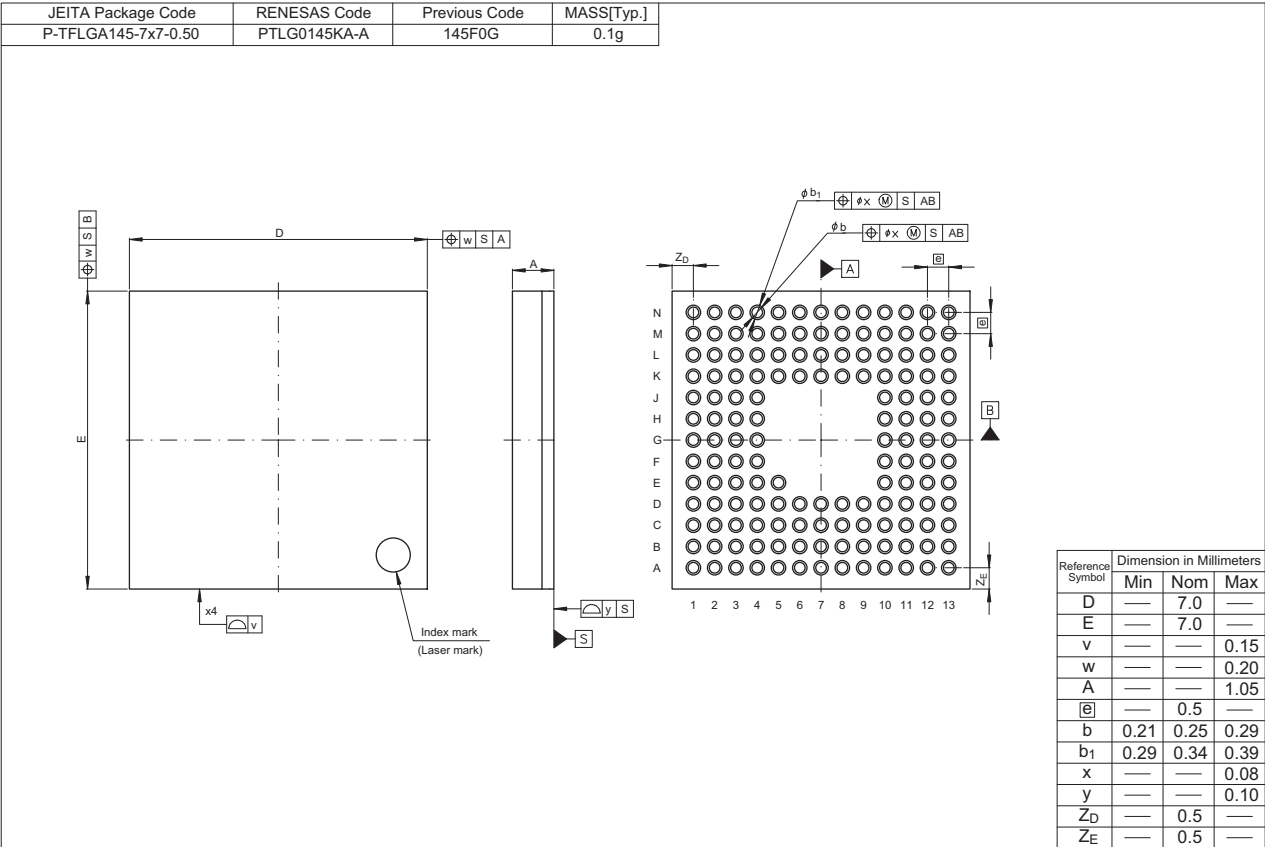


Figure D 145-pin TFLGA (PTLG0145KA-A)

Rev.	Date	Description	
		Page	Summary
1.70	Oct 08. 2013	80 to 127	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics	
		131, 132	Table 5.4 DC Characteristics (3), changed, Note. 9, Note. 10, added
		133	Table 5.6 Permissible Output Currents, changed
		139	Table 5.12 Clock Timing (Sub-Clock Related), Note 3, added
		167	Table 5.25 Timing of On-Chip Peripheral Modules (8), added
		175	Figure 5.58 PDC Timing, added
		175	Figure 5.59 PDC Input Clock Characteristic, added
		176	Figure 5.60 PDC Output Clock Characteristic, added
		178	Table 5.27 10-Bit A/D Conversion Characteristics, changed
		179	Table 5.28 12-Bit A/D Conversion Characteristics, changed
		185	Table 5.35 ROM (Flash Memory for Code Storage) Characteristics (1), added
		185	Table 5.36 ROM (Flash Memory for Code Storage) Characteristics (2), changed
		186	Table 5.37 E2 Flash Characteristics (1), added
		186	Table 5.38 E2 Flash Characteristics (2), changed
		Appendix 1.Package Dimensions	
		197	Figure H 64-pin TFLGA (PTLG0064JA-A), added