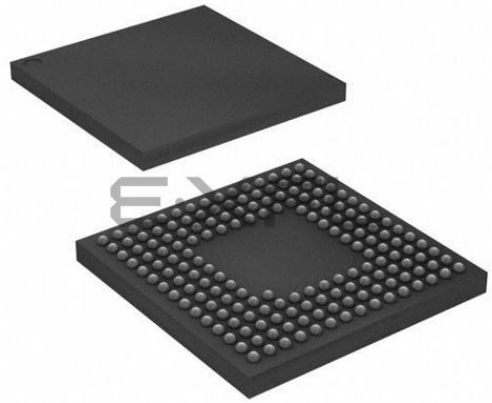
Renesas Electronics America Inc - R5F5631ACDLC#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	177-TFLGA
Supplier Device Package	177-TFLGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631acdlc-u0

Note 3. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (5/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
N7	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET_EXOUT	IRQ10	
N8	VSS						
N9		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA/ET_COL	IRQ14	
N10	TRSYNC	P82	EDREQ1	MTIOC4A/PO28	TXD10/SMOSI10/SSDA10/ ET_ETXD1/RMII_TXD1		
N11		PC3	A19	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ IETXD/ET_TX_ER		
N12		P75	CS5#	PO20	SCK11/ET_ERXD0/ RMII_RXD0		
N13		P74	CS4#	PO19	CTS11#/RTS11#/SS11#/ ET_ERXD1/RMII_RXD1		

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (2/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
D2	XCOUT						
D3	MD/FINED						
D4	VBATT						
D5		P45				IRQ13-DS	AN005
D6		P46				IRQ14-DS	AN006
D7		PE6	D14[A14/D14]		MOSIB	IRQ6	AN4
D8		PE7	D15[A15/D15]		MISOB	IRQ7	AN5
D9		PA1	A1	MTIOC0B/ MTCLKC/ TIOCB0/PO17	SCK5/SSLA2/ ET_WOL	IRQ11	
D10		PA0	A0/BC0#	MTIOC4A/ TIOCA0/PO16	SSLA1/ET_TX_EN/ RMII_TXD_EN		
E1	XTAL	P37					
E2	VSS						
E3	RES#						
E4	TRST#	P34		MTIOC0A/ TMCI3/PO12/ POE2#	SCK6/SCK0/ USB0_DPRPD	IRQ4	
E5		P41				IRQ9-DS	AN001
E6		PA2	A2	PO18	RXD5/SMISO5/ SSCL5/SSLA3		
E7		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE2#	CTS5#/RTS5#/ SS5#/MOSIA/ ET_EXOUT		
E8		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0/ ET_MDC	IRQ5-DS	
E9		PA5	A5	TIOCB1/PO21	RSPCKA/ ET_LINKSTA		
E10		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET_MDIO	IRQ6-DS	
F1	EXTAL	P36					
F2	VCC						
F3		P35				NMI	
F4		P32		MTIOC0C/ TIOCC0/TMO3/ PO10/ RTCOUT/ RTCIC2	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0*1/ USB0_VBUSEN	IRQ2-DS	
F5		P12		TMCI1	RXD2/SMISO2/ SSCL2/SCL0[FM+]	IRQ2	
F6		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE3#	SCK6/ET_RX_ER/ RMII_RX_ER		

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (4/4)

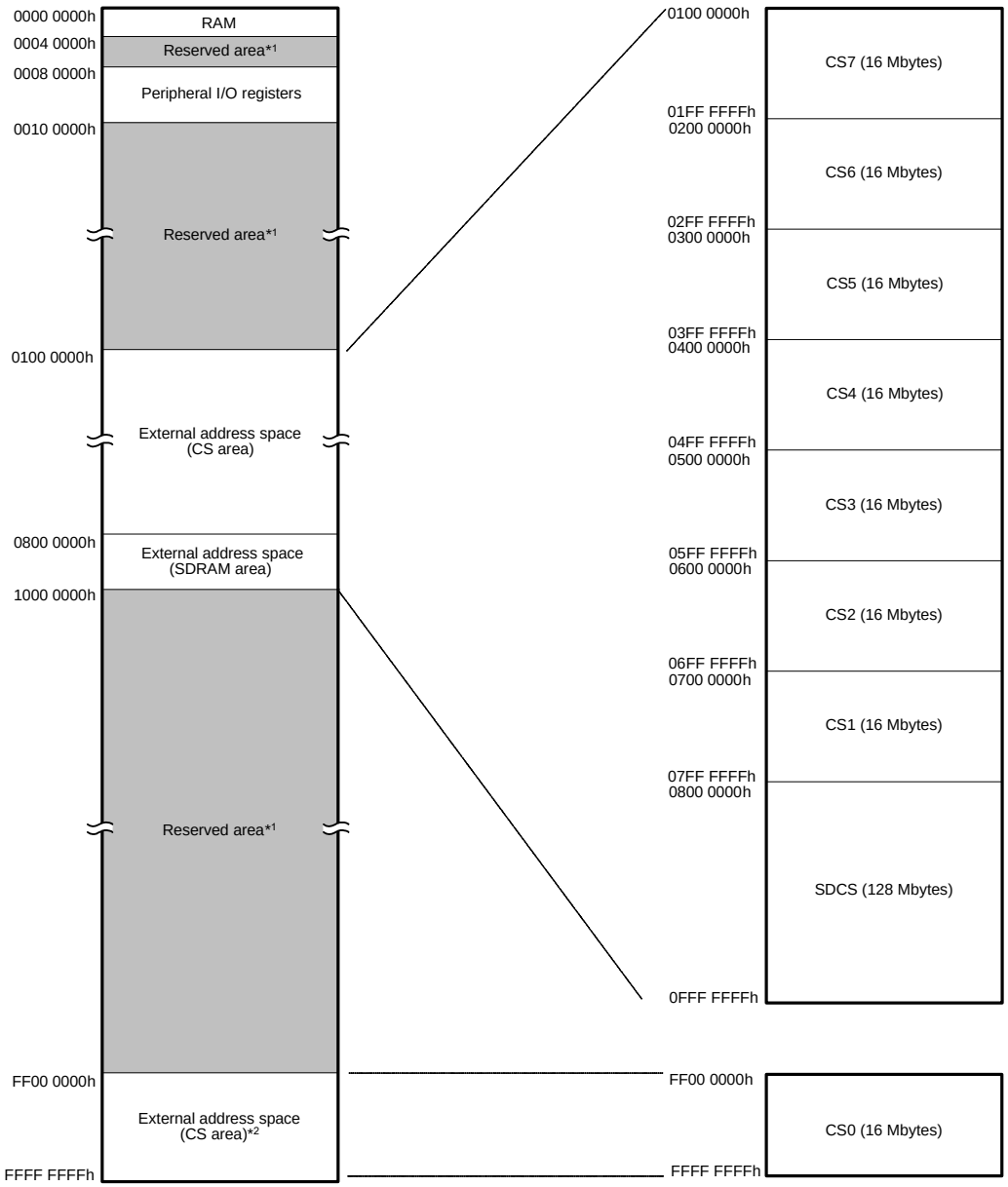
Pin No. 100-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
94	VREFL0						
95		P40				IRQ8-DS	AN000
96	VREFH0						
97	AVCC0						
98		P07				IRQ15	ADTRG0#
99	AVSS0						
100		P05				IRQ13	DA1

Note 1. Enabled only for the ROM capacity of 768 Kbytes or more

Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

3.2 External Address Space

The external address space is classified into CS areas (CS0 to CS7) and SDRAM area (SDCS). CS areas can be divided into up to eight areas (CS0 to SC7) corresponding to the CSn# signal to be output from the CSn# pin.
Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) and SDRAM area (SDCS) in on-chip ROM disabled extended mode.



Note 1. Reserved areas should not be accessed.
Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode.
In this mode, the address space for addresses above 1000 0000h is as shown in figure on this section, Memory Map in Each Operating Mode.

Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

Table 4.1 List of I/O Registers (Address Order) (10/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 719Ch	ICU	DTC activation enable register 156	DTCER156	8	8	2 ICLK		ICUb
0008 719Dh	ICU	DTC activation enable register 157	DTCER157	8	8	2 ICLK		
0008 719Eh	ICU	DTC activation enable register 158	DTCER158	8	8	2 ICLK		
0008 719Fh	ICU	DTC activation enable register 159	DTCER159	8	8	2 ICLK		
0008 71A0h	ICU	DTC activation enable register 160	DTCER160	8	8	2 ICLK		
0008 71A1h	ICU	DTC activation enable register 161	DTCER161	8	8	2 ICLK		
0008 71A2h	ICU	DTC activation enable register 162	DTCER162	8	8	2 ICLK		
0008 71A3h	ICU	DTC activation enable register 163	DTCER163	8	8	2 ICLK		
0008 71A4h	ICU	DTC activation enable register 164	DTCER164	8	8	2 ICLK		
0008 71A5h	ICU	DTC activation enable register 165	DTCER165	8	8	2 ICLK		
0008 71AAh	ICU	DTC activation enable register 170	DTCER170	8	8	2 ICLK		
0008 71ABh	ICU	DTC activation enable register 171	DTCER171	8	8	2 ICLK		
0008 71ADh	ICU	DTC activation enable register 173	DTCER173	8	8	2 ICLK		
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8	2 ICLK		
0008 71B0h	ICU	DTC activation enable register 176	DTCER176	8	8	2 ICLK		
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8	2 ICLK		
0008 71B3h	ICU	DTC activation enable register 179	DTCER179	8	8	2 ICLK		
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8	2 ICLK		
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8	2 ICLK		
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8	2 ICLK		
0008 71BBh	ICU	DTC activation enable register 187	DTCER187	8	8	2 ICLK		
0008 71BCh	ICU	DTC activation enable register 188	DTCER188	8	8	2 ICLK		
0008 71BFh	ICU	DTC activation enable register 191	DTCER191	8	8	2 ICLK		
0008 71C0h	ICU	DTC activation enable register 192	DTCER192	8	8	2 ICLK		
0008 71C3h	ICU	DTC activation enable register 195	DTCER195	8	8	2 ICLK		
0008 71C4h	ICU	DTC activation enable register 196	DTCER196	8	8	2 ICLK		
0008 71C6h	ICU	DTC activation enable register 198	DTCER198	8	8	2 ICLK		
0008 71C7h	ICU	DTC activation enable register 199	DTCER199	8	8	2 ICLK		
0008 71C8h	ICU	DTC activation enable register 200	DTCER200	8	8	2 ICLK		
0008 71C9h	ICU	DTC activation enable register 201	DTCER201	8	8	2 ICLK		
0008 71CAh	ICU	DTC activation enable register 202	DTCER202	8	8	2 ICLK		
0008 71CBh	ICU	DTC activation enable register 203	DTCER203	8	8	2 ICLK		
0008 71CEh	ICU	DTC activation enable register 206	DTCER206	8	8	2 ICLK		
0008 71CFh	ICU	DTC activation enable register 207	DTCER207	8	8	2 ICLK		
0008 71D0h	ICU	DTC activation enable register 208	DTCER208	8	8	2 ICLK		
0008 71D6h	ICU	DTC activation enable register 214	DTCER214	8	8	2 ICLK		
0008 71D7h	ICU	DTC activation enable register 215	DTCER215	8	8	2 ICLK		
0008 71D9h	ICU	DTC activation enable register 217	DTCER217	8	8	2 ICLK		
0008 71DAh	ICU	DTC activation enable register 218	DTCER218	8	8	2 ICLK		
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8	2 ICLK		
0008 71DDh	ICU	DTC activation enable register 221	DTCER221	8	8	2 ICLK		
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8	2 ICLK		
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8	2 ICLK		
0008 71E2h	ICU	DTC activation enable register 226	DTCER226	8	8	2 ICLK		
0008 71E3h	ICU	DTC activation enable register 227	DTCER227	8	8	2 ICLK		
0008 71E5h	ICU	DTC activation enable register 229	DTCER229	8	8	2 ICLK		
0008 71E6h	ICU	DTC activation enable register 230	DTCER230	8	8	2 ICLK		
0008 71E8h	ICU	DTC activation enable register 232	DTCER232	8	8	2 ICLK		
0008 71E9h	ICU	DTC activation enable register 233	DTCER233	8	8	2 ICLK		
0008 71EBh	ICU	DTC activation enable register 235	DTCER235	8	8	2 ICLK		
0008 71ECh	ICU	DTC activation enable register 236	DTCER236	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (36/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C456h	RTC	Hour capture register 0	RHRCP0	8	8	2, 3 PCLKB	2 ICLK	RTCa
0008 C45Ah	RTC	Date capture register 0	RDAYCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C45Ch	RTC	Month capture register 0	RMONCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C462h	RTC	Second capture register 1	RSECCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C464h	RTC	Minute capture register 1	RMINCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C466h	RTC	Hour capture register 1	RHRCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C46Ah	RTC	Date capture register 1	RDAYCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C46Ch	RTC	Month capture register 1	RMONCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C472h	RTC	Second capture register 2	RSECCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C474h	RTC	Minute capture register 2	RMINCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C476h	RTC	Hour capture register 2	RHRCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C47Ah	RTC	Date capture register 2	RDAYCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C47Ch	RTC	Month capture register 2	RMONCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C500h	TEMPS	Temperature sensor control register	TSCR	8	8	2, 3 PCLKB	2 ICLK	Temperature Sensor
0008 C880h	SYSTEM	Counter-clock extension register 1	SCK1	8	8	2, 3 PCLKB	2 ICLK	MCK
0008 C890h	SYSTEM	Counter-clock extension register 2	SCK2	8	8	2, 3 PCLKB	2 ICLK	
0009 0200h to 0009 03FFh	CAN0	Mailbox registers 0 to 31	MB0 to 31	128	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 0400h to 0009 041Fh	CAN0	Mask registerer 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0420h	CAN0	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0424h	CAN0	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0428h	CAN0	Mask invalid register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 042Ch	CAN0	Mailbox interrupt enable register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0820h to 0009 083Fh	CAN0	Message control registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	
0009 0840h	CAN0	Control register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 0842h	CAN0	Status register	STR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 0844h	CAN0	Bit configuration register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0848h	CAN0	Receive FIFO control register	RFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 0849h	CAN0	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Ah	CAN0	Transmit FIFO control register	TFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Bh	CAN0	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Ch	CAN0	Error interrupt enable register	EIER	8	8	2, 3 PCLKB	2 ICLK	
0009 084Dh	CAN0	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Eh	CAN0	Receive error count register	RECR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Fh	CAN0	Transmit error count register	TECR	8	8	2, 3 PCLKB	2 ICLK	
0009 0850h	CAN0	Error code store register	ECSR	8	8	2, 3 PCLKB	2 ICLK	
0009 0851h	CAN0	Channel search support register	CSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 0852h	CAN0	Mailbox search status register	MSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 0853h	CAN0	Mailbox search mode register	MSMR	8	8	2, 3 PCLKB	2 ICLK	
0009 0854h	CAN0	Time stamp register	TSR	16	16	2, 3 PCLKB	2 ICLK	
0009 0856h	CAN0	Acceptance filter support register	AFSR	16	16	2, 3 PCLKB	2 ICLK	
0009 0858h	CAN0	Test control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0009 1200h to 0009 13FFh	CAN1	Mailbox registers 0 to 31	MB0 to 31	128	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1400h to 0009 141Fh	CAN1	Mask register 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1420h	CAN1	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1424h	CAN1	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (45/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 024Eh	USB1	Device state changing register	DVCHGR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0250h	USB1	USB address register	USBADDR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0254h	USB1	USB request type register	USBREQ	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0256h	USB1	USB request value register	USBVAL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0258h	USB1	USB request index register	USBINDX	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 025Ah	USB1	USB request length register	USBLENG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	USBa
000A 025Ch	USB1	DCP configuration register	DCPCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 025Eh	USB1	DCP maximum packet size register	DCPMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0260h	USB1	DCP control register	DCPCTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0264h	USB1	Pipe window select register	PIPESEL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	

Table 4.1 List of I/O Registers (Address Order) (46/50)

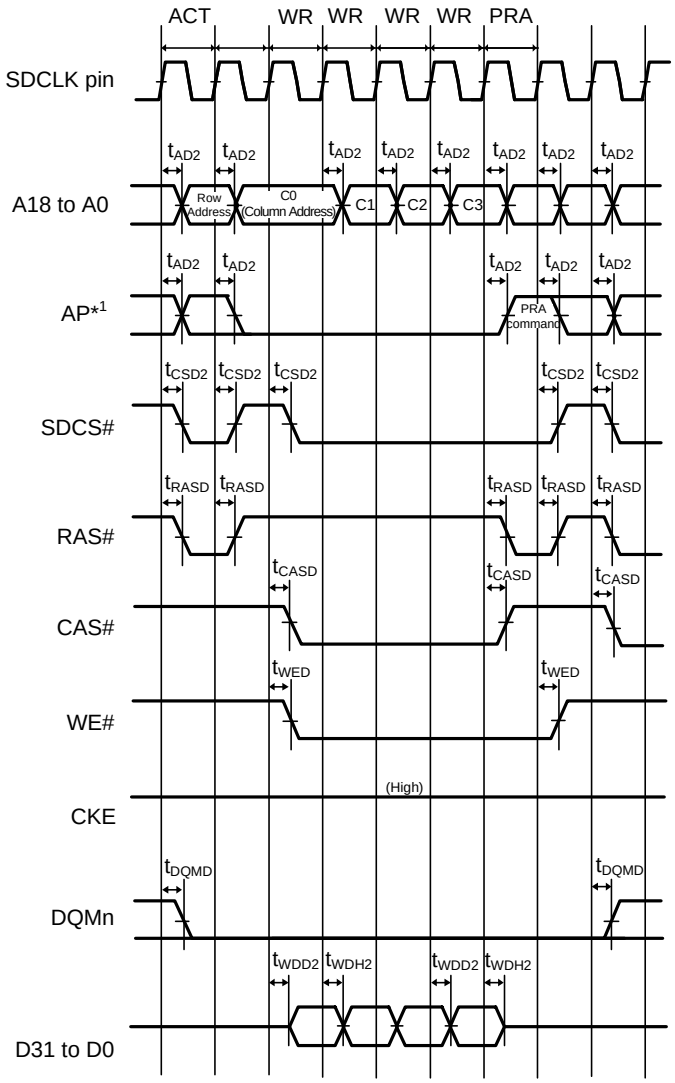
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 0268h	USB1	Pipe configuration register	PIPECFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 026Ch	USB1	Pipe maximum packet size register	PIPEMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 026Eh	USB1	Pipe cycle control register	PIPEPERI	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0270h	USB1	Pipe 1 control register	PIPE1CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	USBa
000A 0272h	USB1	Pipe 2 control register	PIPE2CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0274h	USB1	Pipe 3 control register	PIPE3CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0276h	USB1	Pipe 4 control register	PIPE4CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0278h	USB1	Pipe 5 control register	PIPE5CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 027Ah	USB1	Pipe 6 control register	PIPE6CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 027Ch	USB1	Pipe 7 control register	PIPE7CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	

5.3.5 Bus Timing

Table 5.16 Bus Timing (packages with 177 to 144 pins)

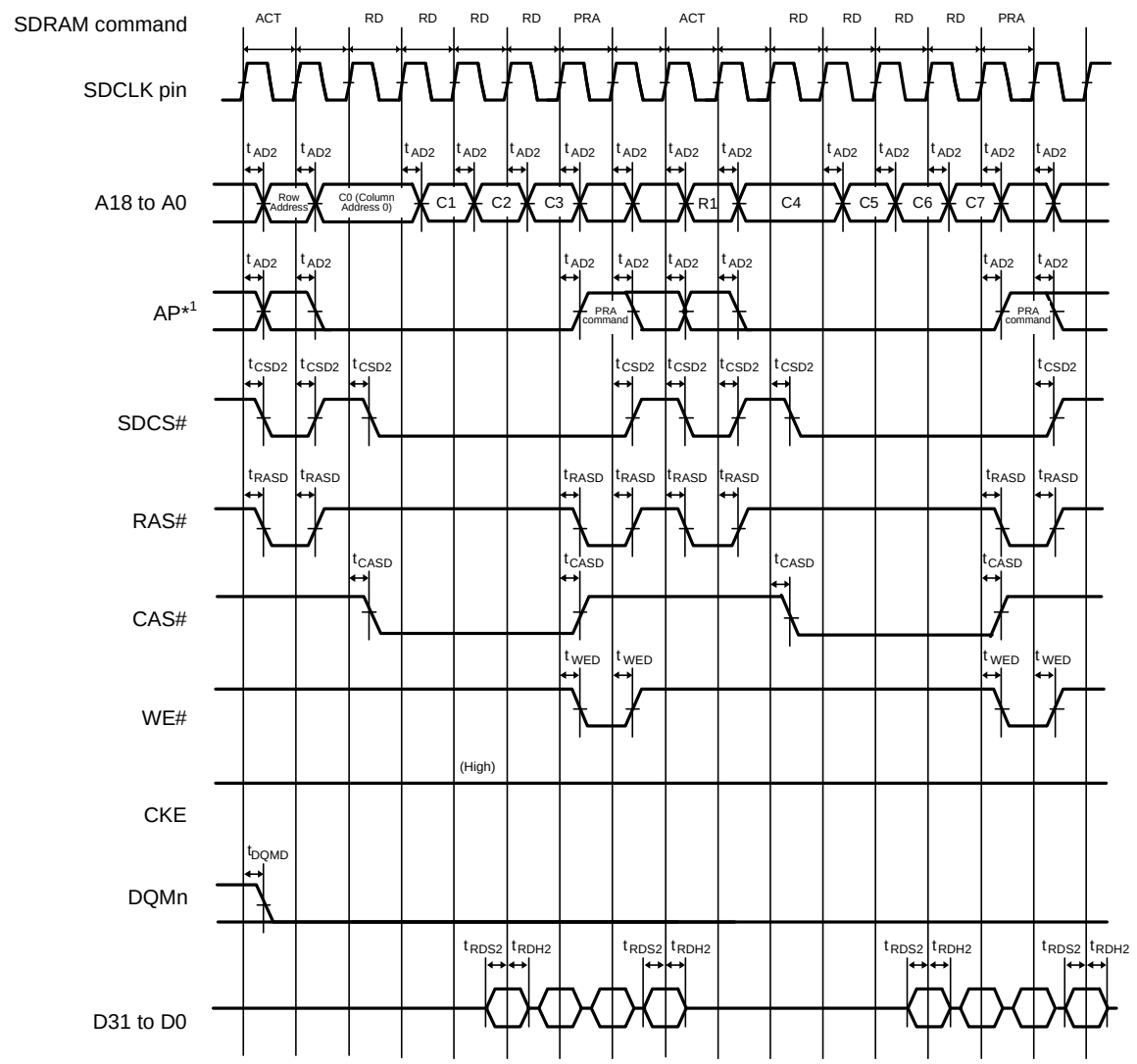
Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V,
ICLK = 8 to 100 MHz, BCLK pin = 8 to 50 MHz, SDCLK pin = 8 to 50MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF
High drive output is selected by the drive capacity control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	15	ns	Figure 5.17 to Figure 5.22
Byte control delay time	t_{BCD}	—	15	ns	
CS# delay time	t_{CSD}	—	15	ns	
ALE delay time	t_{ALED}	—	20	ns	
RD# delay time	t_{RSD}	—	15	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	15	ns	
Write data delay time	t_{WDD}	—	15	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.23
WAIT# hold time	t_{WTH}	0	—	ns	
Address delay time 2 (SDRAM)	t_{AD2}	1	15	ns	Figure 5.24 to Figure 5.30
CS# delay time 2 (SDRAM)	t_{CSD2}	1	15	ns	
DQM delay time (SDRAM)	t_{DQMD}	1	15	ns	
CKE delay time (SDRAM)	t_{CKED}	1	15	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	12	—	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	0	—	ns	
Write data delay time 2 (SDRAM)	t_{WDD2}	—	15	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	1	—	ns	
WE# delay time (SDRAM)	t_{WED}	1	15	ns	
RAS# delay time (SDRAM)	t_{RASD}	1	15	ns	
CAS# delay time (SDRAM)	t_{CASD}	1	15	ns	



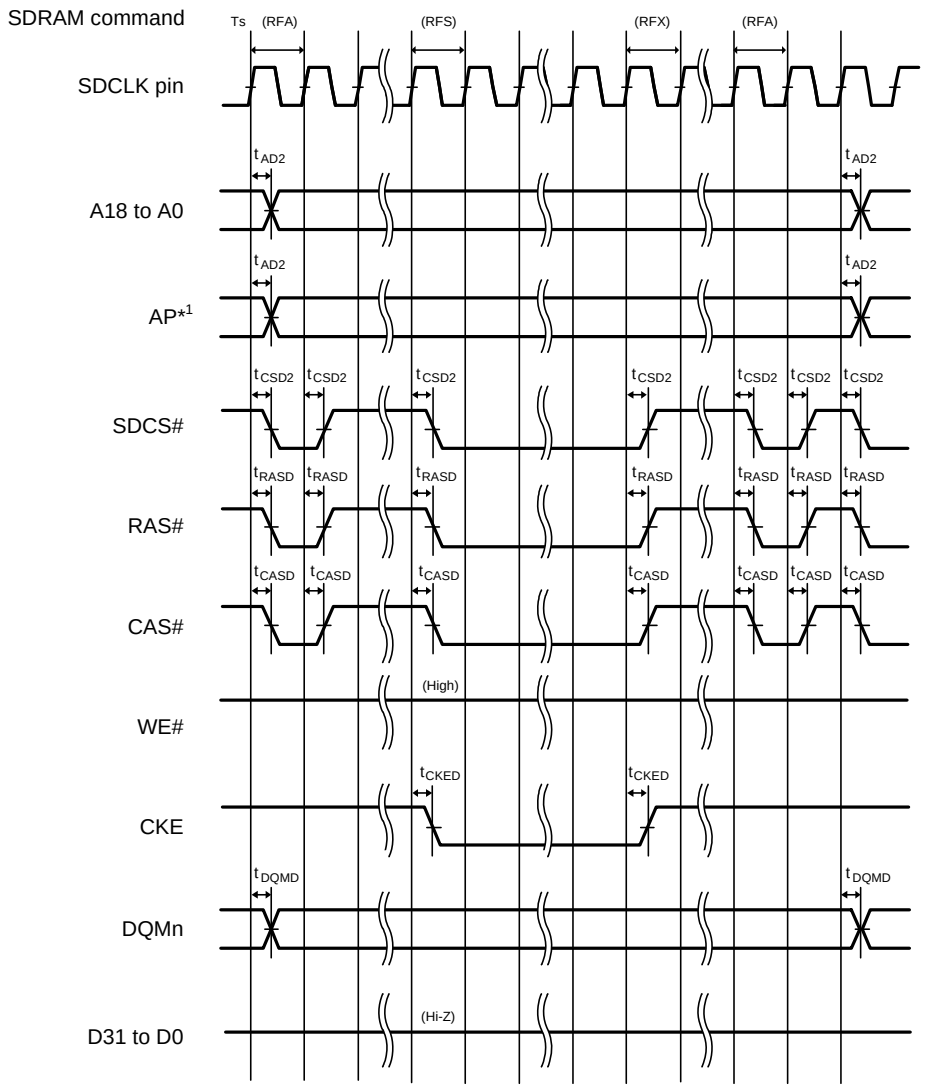
Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.27 SDRAM Space Multiple Write Bus Timing



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.28 SDRAM Space Multiple Read Line Stride Bus Timing



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.30 SDRAM Space Self-Refresh Bus Timing

Table 5.23 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a = T_{opr}$
High drive output is selected by the drive capacity control register.

Item		Symbol	Min.*1,*2	Max.*	Unit	Test Conditions
RIIC (Standard-mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 1300$	—	ns	Figure 5.47
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 600$	—	ns	
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICϕ) Cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. Cb is the total capacitance of the bus lines.

Table 5.24 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a = T_{opr}$
High drive output is selected by the drive capacity control register.

Item		Symbol	Min.*, *2	Max.*	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 240	—	ns	Figure 5.47
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	120	ns	
	SCL, SDA input fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 120	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 120	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 120	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	
Simple IIC (Standard-mode)	SDA input rise time	t_{Sr}	—	1000	ns	
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICϕ) Cycle, t_{Pcyc}: PCLK cycle
Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. Cb indicates the total capacity of the bus line.

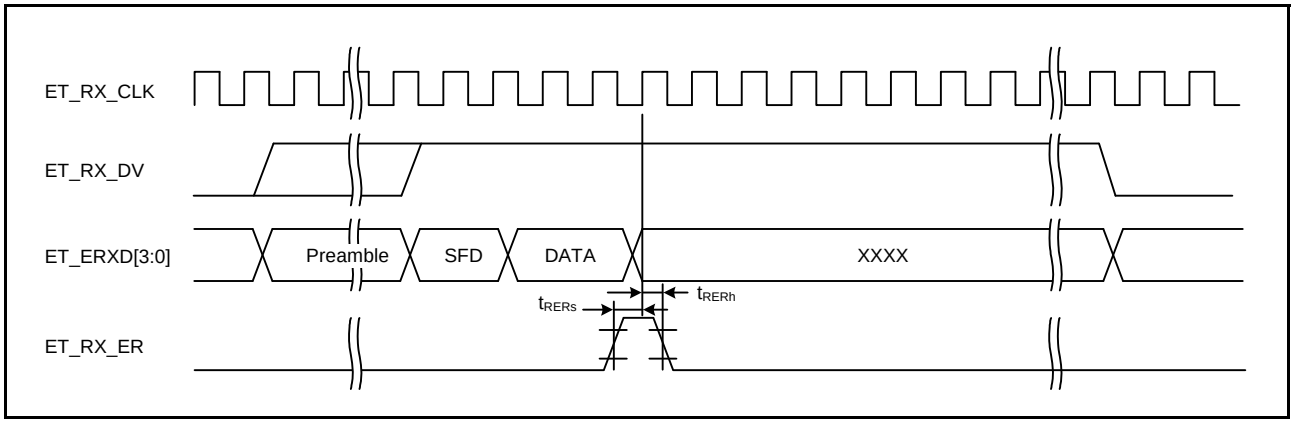


Figure 5.56 MII Reception Timing (Error Occurrence)

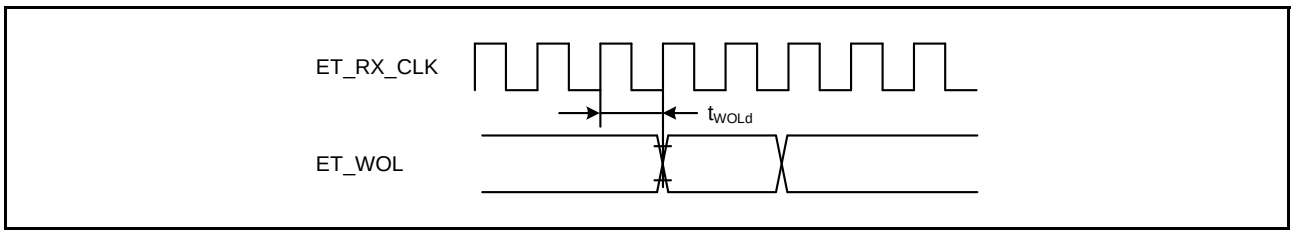


Figure 5.57 WOL Output Timing (MII)

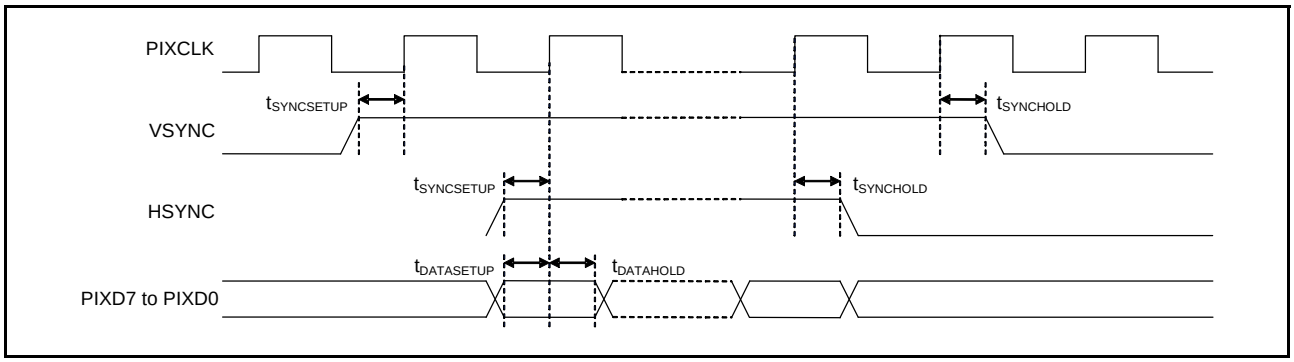


Figure 5.58 PDC Timing

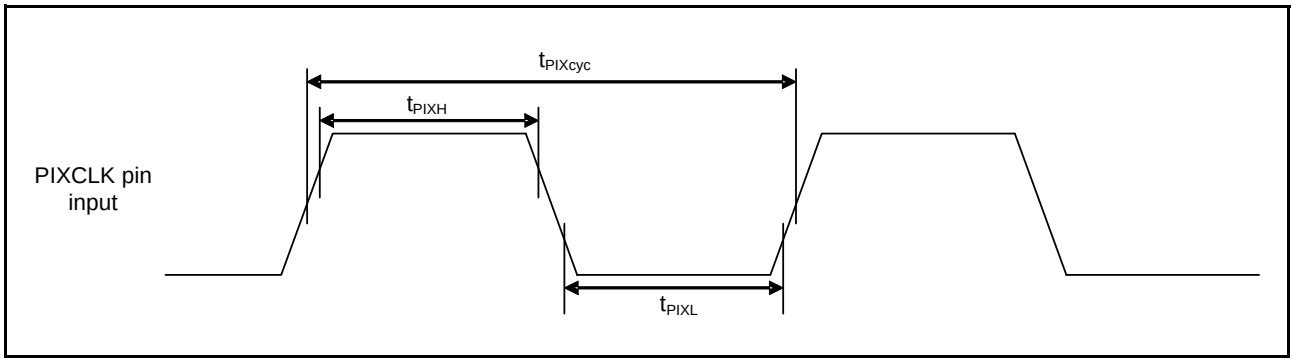


Figure 5.59 PDC Input Clock Characteristic

5.13 Boundary Scan

Table 5.40 Boundary Scan

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 5.70
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TRST# pulse width	t_{TRSTW}	20	—	—	t_{TCKcyc}	Figure 5.71
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 5.72
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	40	ns	

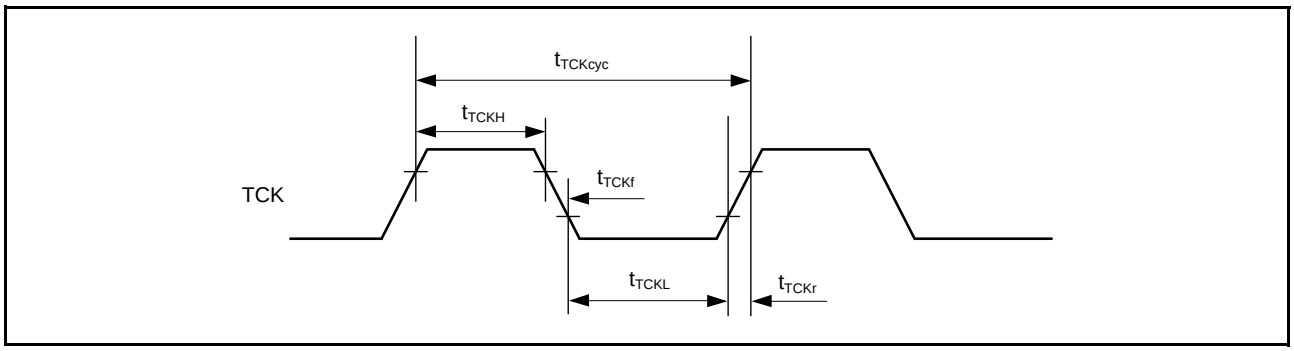


Figure 5.70 Boundary Scan TCK Timing

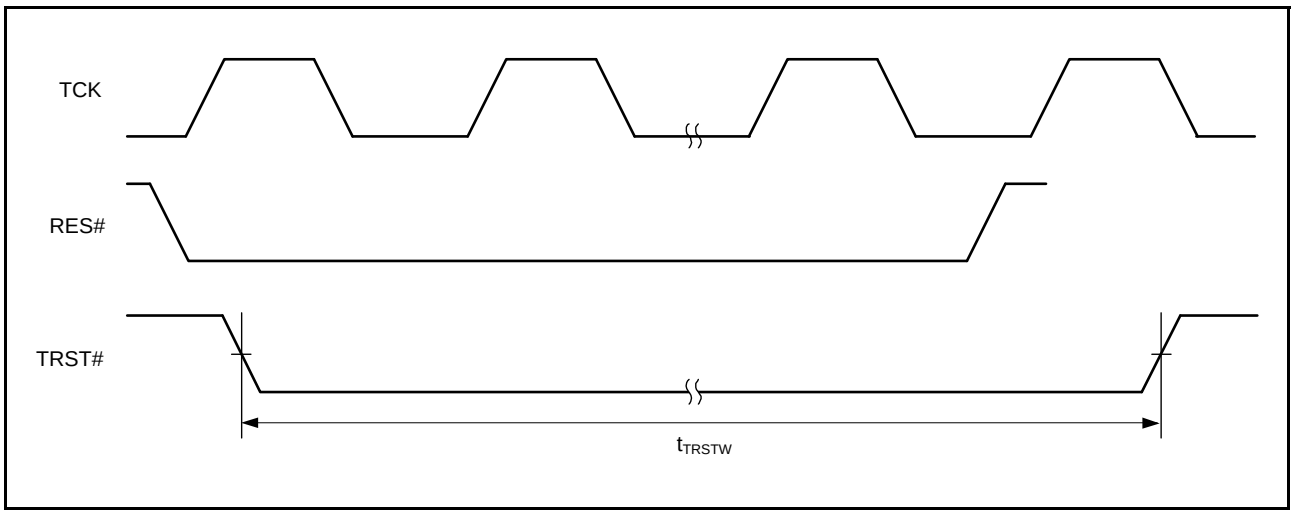
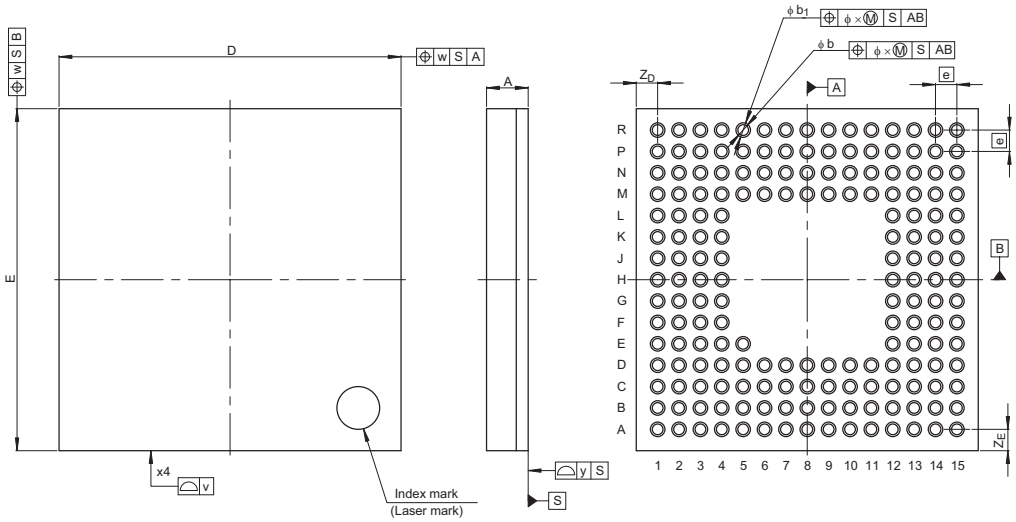


Figure 5.71 Boundary Scan TRST# Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

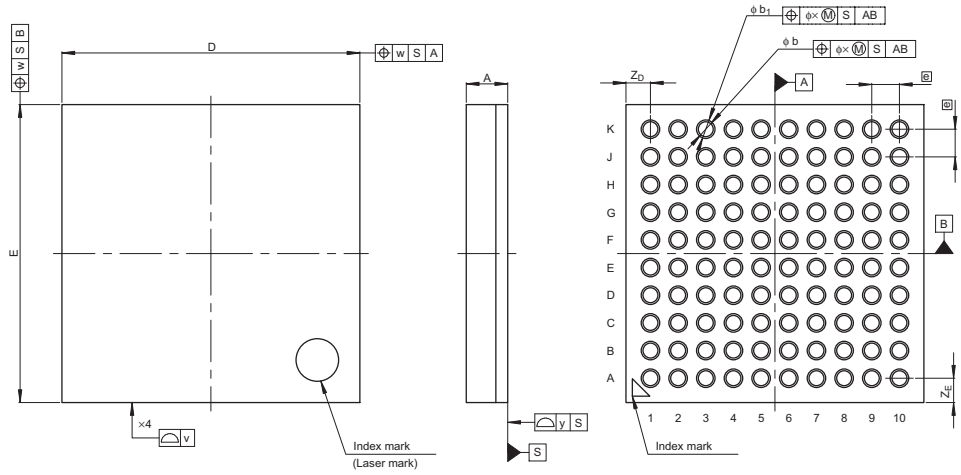
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA177-8x8-0.50	PTLG0177KA-A	177F0E-A	0.2g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	8.0	—
E	—	8.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure A 177-pin TFLGA (PTLG0177KA-A)

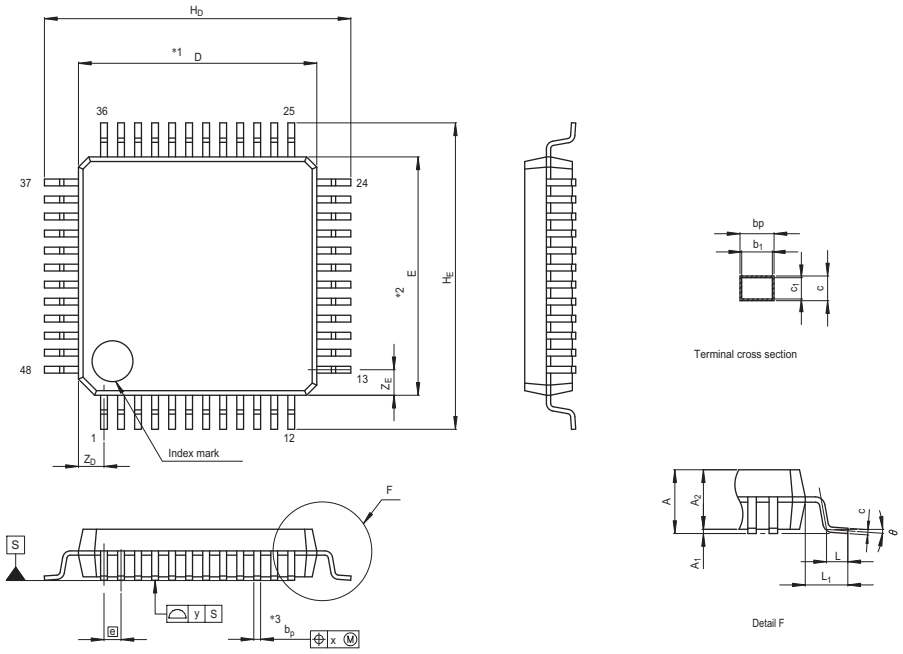
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-7x7-0.65	PTLG0100JA-A	100F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.385	0.435	0.485
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.575	—

Figure F 100-pin TFLGA (PTLG0100JA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure J 48-pin LQFP (PLQP0048KB-A)