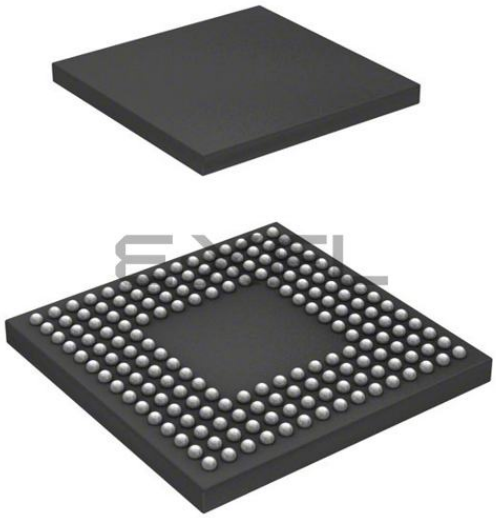
Renesas Electronics America Inc - R5F5631ADDBG#U0 Datasheet



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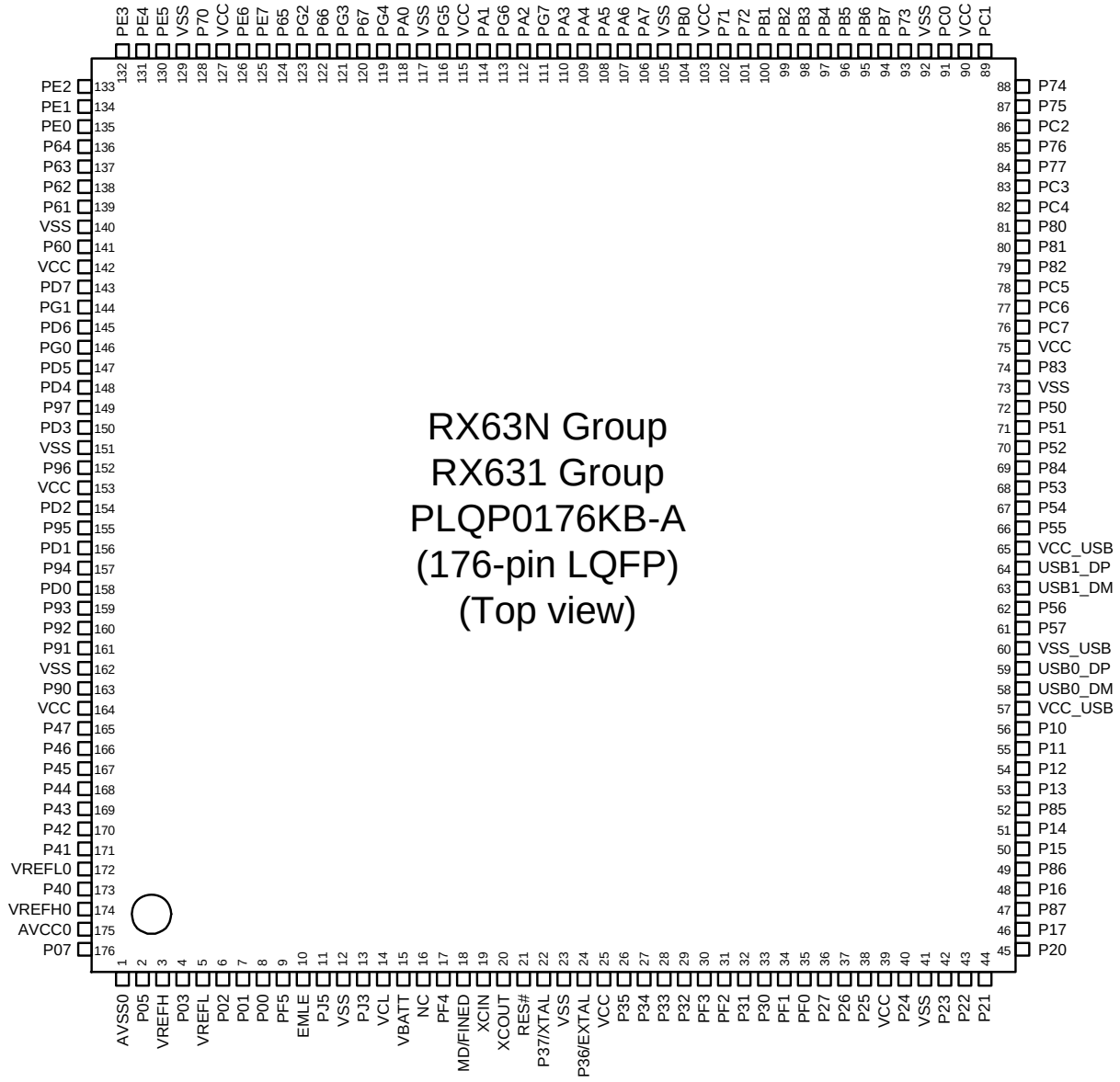
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631addbg-u0

Table 1.4 Pin Functions (2/6)

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode.
	WR0# to WR3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16, and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0# to BC3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16, and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
	CKE	Output	Output pin for SDRAM clock enable signals.
	SDCS#	Output	Output pin for SDRAM chip select signals.
	RAS#	Output	Output pin for SDRAM row address strobe signals.
	CAS#	Output	Output pin for SDRAM column address strobe signals.
	WE#	Output	Output pin for SDRAM write enable signals.
	DQM0 to DQM3	Output	Output pins for SDRAM I/O data mask enable signals.
	CS0# to CS7#	Output	Select signals for CS area.
	WAIT#	Input	Input pins for wait request signals in access to the external space.
EXDMA controller	EDREQ0, EDREQ1		Input pins for external DMA transfer requests.
	EDACK0, EDACK1		Output pins for single address transfer acknowledge signals.
Interrupt	NMI	Input	Non-maskable interrupt request signal.
	IRQ0 to IRQ15	Input	Maskable interrupt request signals.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins.
	MTCLKA, MTCLKB MTCLKC, MTCLKD	Input	Input pins for external clock signals.
Port output enable 2	POE0# to POE3# POE8#	Input	Input pins for request signals to place the MTU large-current pins in the high impedance state.



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pin and Pin Functions (176-Pin LQFP).

Figure 1.5 Pin Assignment (176-Pin LQFP)

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (5/5)

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
136		P64	CS4#/WE#				
137		P63	CS3#/CAS#				
138		P62	CS2#/RAS#				
139		P61	CS1#/SDCS#				
140	VSS						
141		P60	CS0#				
142	VCC						
143		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
144		PG1	D25				
145		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
146		PG0	D24				
147		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
148		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
149		P97	A23/D23				
150		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
151	VSS						
152		P96	A22/D22				
153	VCC						
154		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
155		P95	A21/D21				
156		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
157		P94	A20/D20				
158		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
159		P93	A19/D19		CTS7#/RTS7#/SS7#		AN017
160		P92	A18/D18		RXD7/SMISO7/SSCL7		AN016
161		P91	A17/D17		SCK7		AN015
162	VSS						
163		P90	A16/D16		TXD7/SMOSI7/SSDA7		AN014
164	VCC						
165		P47				IRQ15-DS	AN007
166		P46				IRQ14-DS	AN006
167		P45				IRQ13-DS	AN005
168		P44				IRQ12-DS	AN004
169		P43				IRQ11-DS	AN003
170		P42				IRQ10-DS	AN002
171		P41				IRQ9-DS	AN001
172	VREFL0						
173		P40				IRQ8-DS	AN000
174	VREFH0						
175	AVCC0						
176		P07				IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (4/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
L3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
L4		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/USB0_VBUSEN/ PIXCLK		
L5		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
L6		P56	EDACK1	MTIOC3C/TIOCA1			
L7		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
L8	TRCLK	P83	EDACK1	MTIOC4C	CTS10#/RTS10#/SS10#/ ET_CRS/RMII_CRS_DV		
L9		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	SCK8/RSPCKA/ ET_ETXD2		
L10		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TIOCC6/TCLKE/TMCI1/ PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0/ET_TX_CLK		
L11		PC2	A18	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD/ET_RX_DV		
L12		P73	CS3#	PO16	ET_WOL		
L13	VSS						
M1		P22	EDREQ0	MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0/USB0_DRPD/PIXD6		
M2		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/ IETXD/PIXD3	IRQ7	ADTRG#
M3		P86		TIOCA0	PIXD1		
M4		P12		TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
M5	VCC_USB						
M6	VSS_USB						
M7		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
M8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TIOCA6/TMCI2/PO30	RXD8/SMISO8/SSCL8/ MOSIA/ET_ETXD3	IRQ13	
M9	TRDATA1	P81	EDACK0	MTIOC3D/PO27	RXD10/SMISO10/SSCL10/ ET_ETXD0/RMII_TXD0		
M10		P77	CS7#	PO23	TXD11/SMOSI11/SSDA11/ ET_RX_ER/RMII_RX_ER		
M11		PC0	A16	MTIOC3C/TCLKC/PO17	CTS5#/RTS5#/SS5#/ SSLA1/SCL3/ET_ERXD3	IRQ14	
M12		PC1	A17	MTIOC3A/TCLKD/PO18	SCK5/SSLA2/SDA3/ ET_ERXD2	IRQ12	
M13	VCC						
N1		P21		MTIOC1B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/SSCL0/ SCL1/USB0_EXICEN/ PIXD5	IRQ9	
N2		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/SSDA0/ SDA1/USB0_ID/PIXD4	IRQ8	
N3		P87		TIOCA2	PIXD2		
N4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
N5					USB0_DM		
N6					USB0_DP		

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (2/5)

Pin No. 144-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
36		P21		MTIOC1B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/SSCL0/ SCL1/USB0_EXICEN/ PIXD5	IRQ9	
37		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/SSDA0/ SDA1/USB0_ID/PIXD4	IRQ8	
38		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/IETXD/PIXD3	IRQ7	ADTRG#
39		P87		TIOCA2	PIXD2		
40		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
41		P86		TIOCA0	PIXD1		
42		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/ TMCI2/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ PIXD0	IRQ5	
43		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
44		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
45		P12		TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
46	VCC_USB						
47					USB0_DM		
48					USB0_DP		
49	VSS_USB						
50		P56	EDACK1	MTIOC3C/TIOCA1			
51	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET_EXOUT	IRQ10	
52	TRDATA2	P54	ALE/EDACK0	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX1/ET_LINKSTA		
53		P53*1	BCLK				
54		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
55		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
56		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
57	VSS						
58	TRCLK	P83	EDACK1	MTIOC4C	CTS10#/RTS10#/ SS10#/ET_CRS/ RMII_CRS_DV		
59	VCC						
60		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA/ET_COL	IRQ14	
61		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TIOCA6/TMCI2/PO30	RXD8/SMISO8/SSCL8/ MOSIA/ET_ETXD3	IRQ13	
62		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/ TMRI2/PO29	SCK8/RSPCKA/ ET_ETXD2		
63	TRSYNC	P82	EDREQ1	MTIOC4A/PO28	TXD10/SMOSI10/ SSDA10/ET_ETXD1/ RMII_TXD1		

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (4/5)

Pin No. 144-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
89		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	CTS5#/RTS5#/SS5# MOSIA/ET_EXOUT		
90		PA5	A5	TIOCB1/PO21	RSPCKA/ET_LINKSTA		
91	VCC						
92		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0/ET_MDC	IRQ5-DS	
93	VSS						
94		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/SSCL5/ ET_MDIO	IRQ6-DS	
95		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
96		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2/ET_WOL	IRQ11	
97		PA0	A0/BC0#	MTIOC4A/TIOCA0/ PO16	SSLA1/ET_TX_EN/ RMII_TXD_EN		
98		P67	CS7#/DQM1		CRX2*2	IRQ15	
99		P66	CS6#/DQM0		CTX2*2		
100		P65	CS5#/CKE				
101		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
102		PE6	D14[A14/D14]	TIOCA11	MOSIB	IRQ6	AN4
103	VCC						
104	SDCLK	P70					
105	VSS						
106		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	RSPCKB/ET_RX_CLK/ REF50CK	IRQ5	AN3
107		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0/ET_ERXD2		AN2
108		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/ PO26/POE8#	CTS12#/RTS12#/ SS12#/MISOB/ ET_ERXD3		AN1
109		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/ PO23	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3/MOSIB	IRQ7-DS	AN0
110		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/ PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/ RSPCKB		ANEX1
111		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
112		P64	CS4#/WE#				
113		P63	CS3#/CAS#				
114		P62	CS2#/RAS#				
115		P61	CS1#/SDCS#				
116	VSS						
117		P60	CS0#				
118	VCC						
119		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
120		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
121		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
122		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
123		PD3	D3[A3/D3]	TIOCB8/TCLKH/ POE8#	RSPCKC	IRQ3	AN011
124		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (1/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
A1		P05				IRQ13	DA1
A2	VREFH						
A3		P07				IRQ15	ADTRG0#
A4	VREFL0						
A5		P43				IRQ11-DS	AN003
A6		PD0	D0[A0/D0]			IRQ0	AN008
A7		PD4	D4[A4/D4]	POE3#		IRQ4	AN012
A8		PE0	D8[A8/D8]		SCK12/SSLB1		ANEX0
A9		PE1	D9[A9/D9]	MTIOC4C/ PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/ RSPCKB		ANEX1
A10		PE2	D10[A10/D10]	MTIOC4A/ PO23	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3/MOSIB	IRQ7-DS	AN0
B1	EMLE						
B2	AVSS0						
B3	AVCC0						
B4		P40				IRQ8-DS	AN000
B5		P44				IRQ12-DS	AN004
B6		PD1	D1[A1/D1]	MTIOC4B	CTX0*1	IRQ1	AN009
B7		PD3	D3[A3/D3]	POE8#		IRQ3	AN011
B8		PD6	D6[A6/D6]	MTIC5V/ POE1#		IRQ6	AN6
B9		PD7	D7[A7/D7]	MTIC5U/ POE0#		IRQ7	AN7
B10		PE3	D11[A11/D11]	MTIOC4B/ PO26/POE8#	CTS12#/RTS12#/ SS12#/MISOB/ ET_ERXD3		AN1
C1	VCL						
C2	VREFL						
C3		PJ3		MTIOC3C	CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#		
C4	VREFH0						
C5		P42				IRQ10-DS	AN002
C6		P47				IRQ15-DS	AN007
C7		PD2	D2[A2/D2]	MTIOC4D	CRX0*1	IRQ2	AN010
C8		PD5	D5[A5/D5]	MTIC5W/ POE2#		IRQ5	AN013
C9		PE5	D13[A13/D13]	MTIOC4C/ MTIOC2B	RSPCKB/ ET_RX_CLK/ REF50CK	IRQ5	AN3
C10		PE4	D12[A12/D12]	MTIOC4D/ MTIOC1A/ PO28	SSLB0/ET_ERXD2		AN2
D1	XCIN						

Table 4.1 List of I/O Registers (Address Order) (2/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 201Ch	DMAC0	DMA transfer enable register	DMCNT	8	8	2 ICLK		DMACA
0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8	2 ICLK		DMACA
0008 201Eh	DMAC0	DMA status register	DMSTS	8	8	2 ICLK		
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32	2 ICLK		
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 205Ch	DMAC1	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8	2 ICLK		
0008 205Eh	DMAC1	DMA status register	DMSTS	8	8	2 ICLK		
0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 2080h	DMAC2	DMA source address register	DMSAR	32	32	2 ICLK		
0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8	2 ICLK		
0008 209Eh	DMAC2	DMA status register	DMSTS	8	8	2 ICLK		
0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32	2 ICLK		
0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8	2 ICLK		
0008 20DEh	DMAC3	DMA status register	DMSTS	8	8	2 ICLK		
0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 2200h	DMAC	DMACA module activation register	DMAST	8	8	2 ICLK		
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK		DTCa
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK		
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK		
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK		
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK		
0008 2800h	EXDMAC0	EXDMA source address register	EDMSAR	32	32	1, 2 BCLK		EXDMACa
0008 2804h	EXDMAC0	EXDMA destination address register	EDMDAR	32	32	1, 2 BCLK		
0008 2808h	EXDMAC0	EXDMA transfer count register	EDMCRA	32	32	1, 2 BCLK		
0008 280Ch	EXDMAC0	EXDMA block transfer count register	EDMCRB	16	16	1, 2 BCLK		
0008 2810h	EXDMAC0	EXDMA transfer mode register	EDMTMD	16	16	1, 2 BCLK		
0008 2812h	EXDMAC0	EXDMA output setting register	EDMOMD	8	8	1, 2 BCLK		
0008 2813h	EXDMAC0	EXDMA interrupt setting register	EDMINT	8	8	1, 2 BCLK		
0008 2814h	EXDMAC0	EXDMA address mode register	EDMAMD	32	32	1, 2 BCLK		

Table 4.1 List of I/O Registers (Address Order) (6/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK		ICUb
0008 7048h	ICU	Interrupt request register 072	IR072	8	8	2 ICLK		
0008 7049h	ICU	Interrupt request register 073	IR073	8	8	2 ICLK		
0008 704Ah	ICU	Interrupt request register 074	IR074	8	8	2 ICLK		
0008 704Bh	ICU	Interrupt request register 075	IR075	8	8	2 ICLK		
0008 704Ch	ICU	Interrupt request register 076	IR076	8	8	2 ICLK		
0008 704Dh	ICU	Interrupt request register 077	IR077	8	8	2 ICLK		
0008 704Eh	ICU	Interrupt request register 078	IR078	8	8	2 ICLK		
0008 704Fh	ICU	Interrupt request register 079	IR079	8	8	2 ICLK		
0008 705Ah	ICU	Interrupt request register 090	IR090	8	8	2 ICLK		
0008 705Bh	ICU	Interrupt request register 091	IR091	8	8	2 ICLK		
0008 705Ch	ICU	Interrupt request register 092	IR092	8	8	2 ICLK		
0008 705Dh	ICU	Interrupt request register 093	IR093	8	8	2 ICLK		
0008 7062h	ICU	Interrupt request register 098	IR098	8	8	2 ICLK		
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK		
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2 ICLK		
0008 706Bh	ICU	Interrupt request register 107	IR107	8	8	2 ICLK		
0008 706Ch	ICU	Interrupt request register 108	IR108	8	8	2 ICLK		
0008 706Dh	ICU	Interrupt request register 109	IR109	8	8	2 ICLK		
0008 706Eh	ICU	Interrupt request register 110	IR110	8	8	2 ICLK		
0008 706Fh	ICU	Interrupt request register 111	IR111	8	8	2 ICLK		
0008 7070h	ICU	Interrupt request register 112	IR112	8	8	2 ICLK		
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK		
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8	2 ICLK		
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8	2 ICLK		
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8	2 ICLK		
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8	2 ICLK		
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8	2 ICLK		
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8	2 ICLK		
0008 7080h	ICU	Interrupt request register 128	IR128	8	8	2 ICLK		
0008 7081h	ICU	Interrupt request register 129	IR129	8	8	2 ICLK		
0008 7082h	ICU	Interrupt request register 130	IR130	8	8	2 ICLK		
0008 7083h	ICU	Interrupt request register 131	IR131	8	8	2 ICLK		
0008 7084h	ICU	Interrupt request register 132	IR132	8	8	2 ICLK		
0008 7085h	ICU	Interrupt request register 133	IR133	8	8	2 ICLK		
0008 7086h	ICU	Interrupt request register 134	IR134	8	8	2 ICLK		
0008 7087h	ICU	Interrupt request register 135	IR135	8	8	2 ICLK		
0008 7088h	ICU	Interrupt request register 136	IR136	8	8	2 ICLK		
0008 7089h	ICU	Interrupt request register 137	IR137	8	8	2 ICLK		
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8	2 ICLK		
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8	2 ICLK		
0008 708Ch	ICU	Interrupt request register 140	IR140	8	8	2 ICLK		
0008 708Dh	ICU	Interrupt request register 141	IR141	8	8	2 ICLK		
0008 708Eh	ICU	Interrupt request register 142	IR142	8	8	2 ICLK		
0008 708Fh	ICU	Interrupt request register 143	IR143	8	8	2 ICLK		
0008 7090h	ICU	Interrupt request register 144	IR144	8	8	2 ICLK		
0008 7091h	ICU	Interrupt request register 145	IR145	8	8	2 ICLK		
0008 7092h	ICU	Interrupt request register 146	IR146	8	8	2 ICLK		
0008 7093h	ICU	Interrupt request register 147	IR147	8	8	2 ICLK		
0008 7094h	ICU	Interrupt request register 148	IR148	8	8	2 ICLK		
0008 7095h	ICU	Interrupt request register 149	IR149	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (12/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7322h	ICU	Interrupt source priority register 034	IPR034	8	8	2 ICLK		ICUb
0008 7323h	ICU	Interrupt source priority register 035	IPR035	8	8	2 ICLK		
0008 7324h	ICU	Interrupt source priority register 036	IPR036	8	8	2 ICLK		
0008 7325h	ICU	Interrupt source priority register 037	IPR037	8	8	2 ICLK		
0008 7326h	ICU	Interrupt source priority register 038	IPR038	8	8	2 ICLK		
0008 7327h	ICU	Interrupt source priority register 039	IPR039	8	8	2 ICLK		
0008 732Ah	ICU	Interrupt source priority register 042	IPR042	8	8	2 ICLK		
0008 732Dh	ICU	Interrupt source priority register 045	IPR045	8	8	2 ICLK		
0008 7330h	ICU	Interrupt source priority register 048	IPR048	8	8	2 ICLK		
0008 7334h	ICU	Interrupt source priority register 052	IPR052	8	8	2 ICLK		
0008 7338h	ICU	Interrupt source priority register 056	IPR056	8	8	2 ICLK		
0008 733Eh	ICU	Interrupt source priority register 062	IPR062	8	8	2 ICLK		
0008 7340h	ICU	Interrupt source priority register 064	IPR064	8	8	2 ICLK		
0008 7341h	ICU	Interrupt source priority register 065	IPR065	8	8	2 ICLK		
0008 7342h	ICU	Interrupt source priority register 066	IPR066	8	8	2 ICLK		
0008 7343h	ICU	Interrupt source priority register 067	IPR067	8	8	2 ICLK		
0008 7344h	ICU	Interrupt source priority register 068	IPR068	8	8	2 ICLK		
0008 7345h	ICU	Interrupt source priority register 069	IPR069	8	8	2 ICLK		
0008 7346h	ICU	Interrupt source priority register 070	IPR070	8	8	2 ICLK		
0008 7347h	ICU	Interrupt source priority register 071	IPR071	8	8	2 ICLK		
0008 7348h	ICU	Interrupt source priority register 072	IPR072	8	8	2 ICLK		
0008 7349h	ICU	Interrupt source priority register 073	IPR073	8	8	2 ICLK		
0008 734Ah	ICU	Interrupt source priority register 074	IPR074	8	8	2 ICLK		
0008 734Bh	ICU	Interrupt source priority register 075	IPR075	8	8	2 ICLK		
0008 734Ch	ICU	Interrupt source priority register 076	IPR076	8	8	2 ICLK		
0008 734Dh	ICU	Interrupt source priority register 077	IPR077	8	8	2 ICLK		
0008 734Eh	ICU	Interrupt source priority register 078	IPR078	8	8	2 ICLK		
0008 734Fh	ICU	Interrupt source priority register 079	IPR079	8	8	2 ICLK		
0008 735Ah	ICU	Interrupt source priority register 090	IPR090	8	8	2 ICLK		
0008 735Bh	ICU	Interrupt source priority register 091	IPR091	8	8	2 ICLK		
0008 735Ch	ICU	Interrupt source priority register 092	IPR092	8	8	2 ICLK		
0008 735Dh	ICU	Interrupt source priority register 093	IPR093	8	8	2 ICLK		
0008 7362h	ICU	Interrupt source priority register 098	IPR098	8	8	2 ICLK		
0008 7366h	ICU	Interrupt source priority register 102	IPR102	8	8	2 ICLK		
0008 736Ah	ICU	Interrupt source priority register 106	IPR106	8	8	2 ICLK		
0008 736Bh	ICU	Interrupt source priority register 107	IPR107	8	8	2 ICLK		
0008 736Ch	ICU	Interrupt source priority register 108	IPR108	8	8	2 ICLK		
0008 736Dh	ICU	Interrupt source priority register 109	IPR109	8	8	2 ICLK		
0008 736Eh	ICU	Interrupt source priority register 110	IPR110	8	8	2 ICLK		
0008 736Fh	ICU	Interrupt source priority register 111	IPR111	8	8	2 ICLK		
0008 7370h	ICU	Interrupt source priority register 112	IPR112	8	8	2 ICLK		
0008 7372h	ICU	Interrupt source priority register 114	IPR114	8	8	2 ICLK		
0008 737Ah	ICU	Interrupt source priority register 122	IPR122	8	8	2 ICLK		
0008 737Eh	ICU	Interrupt source priority register 126	IPR126	8	8	2 ICLK		
0008 7382h	ICU	Interrupt source priority register 130	IPR130	8	8	2 ICLK		
0008 7384h	ICU	Interrupt source priority register 132	IPR132	8	8	2 ICLK		
0008 7386h	ICU	Interrupt source priority register 134	IPR134	8	8	2 ICLK		
0008 738Ah	ICU	Interrupt source priority register 138	IPR138	8	8	2 ICLK		
0008 738Ch	ICU	Interrupt source priority register 140	IPR140	8	8	2 ICLK		
0008 738Eh	ICU	Interrupt source priority register 142	IPR142	8	8	2 ICLK		
0008 7392h	ICU	Interrupt source priority register 146	IPR146	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (19/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 8313h	RIIC0	I²C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIIC
0008 8320h	RIIC1	I²C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8321h	RIIC1	I²C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8322h	RIIC1	I²C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8323h	RIIC1	I²C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8324h	RIIC1	I²C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8325h	RIIC1	I²C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8326h	RIIC1	I²C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8327h	RIIC1	I²C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8328h	RIIC1	I²C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8329h	RIIC1	I²C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 832Ah	RIIC1	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 832Ah	RIIC1	Timeout Internal Counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK	
0008 832Bh	RIIC1	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 832Bh	RIIC1	Timeout Internal Counter U	TMOCNTU	8	8	2, 3 PCLKB	2 ICLK	
0008 832Ch	RIIC1	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 832Dh	RIIC1	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 832Eh	RIIC1	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 832Fh	RIIC1	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8330h	RIIC1	I²C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8331h	RIIC1	I²C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8332h	RIIC1	I²C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8333h	RIIC1	I²C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8340h	RIIC2	I²C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8341h	RIIC2	I²C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8342h	RIIC2	I²C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8343h	RIIC2	I²C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8344h	RIIC2	I²C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8345h	RIIC2	I²C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8346h	RIIC2	I²C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8347h	RIIC2	I²C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8348h	RIIC2	I²C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8349h	RIIC2	I²C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 834Ah	RIIC2	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 834Bh	RIIC2	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 834Ch	RIIC2	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 834Dh	RIIC2	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 834Eh	RIIC2	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 834Fh	RIIC2	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8350h	RIIC2	I²C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8351h	RIIC2	I²C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8352h	RIIC2	I²C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8353h	RIIC2	I²C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8360h	RIIC3	I²C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8361h	RIIC3	I²C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8362h	RIIC3	I²C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8363h	RIIC3	I²C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8364h	RIIC3	I²C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8365h	RIIC3	I²C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8366h	RIIC3	I²C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8367h	RIIC3	I²C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (20/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 8368h	RIIC3	I²C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RSPI
0008 8369h	RIIC3	I²C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 836Ah	RIIC3	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 836Bh	RIIC3	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 836Ch	RIIC3	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 836Dh	RIIC3	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 836Eh	RIIC3	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 836Fh	RIIC3	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8370h	RIIC3	I²C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8371h	RIIC3	I²C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8372h	RIIC3	I²C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8373h	RIIC3	I²C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	
0008 839Ah	RSPI0	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	
0008 839Ch	RSPI0	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	RSPI
0008 839Eh	RSPI0	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 83A0h	RSPI1	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A1h	RSPI1	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 83A2h	RSPI1	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A3h	RSPI1	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A4h	RSPI1	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 83A8h	RSPI1	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A9h	RSPI1	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83AAh	RSPI1	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 83ABh	RSPI1	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83ACh	RSPI1	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 83ADh	RSPI1	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 83AEh	RSPI1	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 83AFh	RSPI1	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 83B0h	RSPI1	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 83B2h	RSPI1	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 83B4h	RSPI1	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 83B6h	RSPI1	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 83B8h	RSPI1	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (28/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 A806h	IEB	IEBus slave address setting register 2	IESA2	8	8	3 to 4 PCLKB	2, 3 ICLK	IEB
0008 A807h	IEB	IEBus transmit message length register	IETBFL	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A809h	IEB	IEBus reception master address register 1	IEMA1	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A80Ah	IEB	IEBus reception master address register 2	IEMA2	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A80Bh	IEB	IEBus receive control field register	IERCTL	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A80Ch	IEB	IEBus receive message length register	IERBFL	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A80Eh	IEB	IEBus lock address register 1	IELA1	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A80Fh	IEB	IEBus lock address register 2	IELA2	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A810h	IEB	IEBus general flag register	IEFLG	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A811h	IEB	IEBus transmit status register	IETSR	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A812h	IEB	IEBus transmit interrupt enable register	IEIET	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A814h	IEB	IEBus receive status register	IERSR	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A815h	IEB	IEBus receive interrupt enable register	IEIER	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A818h	IEB	IEBus clock select register	IECKSR	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A900h to 0008 A91Fh	IEB	IEBus transmit data buffer register 001 to 032	IETB001 to 032	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 AA00h to 0008 AA1Fh	IEB	IEBus receive data buffer register 001 to 032	IERB001 to 032	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 B300h	SCI12	Serial mode register	SMR12	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId
0008 B301h	SCI12	Bit rate register	BRR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B302h	SCI12	Serial control register	SCR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B303h	SCI12	Transmit data register	TDR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B304h	SCI12	Serial status register	SSR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B305h	SCI12	Receive data register	RDR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B306h	SCI12	Smart card mode register	SCMR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B307h	SCI12	Serial extended mode register	SEMR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B308h	SCI12	Noise filter setting register	SNFR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B309h	SCI12	I^2C mode register 1	SIMR112	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Ah	SCI12	I^2C mode register 2	SIMR212	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Bh	SCI12	I^2C mode register 3	SIMR312	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Ch	SCI12	I^2C status register	SISR12	8	8	2, 3 PCLKB	2 ICLK	
0008 B30Dh	SCI12	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 B320h	SCI12	Extended serial module enable register	ESMER	8	8	2, 3 PCLKB	2 ICLK	
0008 B321h	SCI12	Control register 0	CR0	8	8	2, 3 PCLKB	2 ICLK	
0008 B322h	SCI12	Control register 1	CR1	8	8	2, 3 PCLKB	2 ICLK	
0008 B323h	SCI12	Control register 2	CR2	8	8	2, 3 PCLKB	2 ICLK	
0008 B324h	SCI12	Control register 3	CR3	8	8	2, 3 PCLKB	2 ICLK	
0008 B325h	SCI12	Port control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 B326h	SCI12	Interrupt control register	ICR	8	8	2, 3 PCLKB	2 ICLK	
0008 B327h	SCI12	Status register	STR	8	8	2, 3 PCLKB	2 ICLK	
0008 B328h	SCI12	Status clear register	STCR	8	8	2, 3 PCLKB	2 ICLK	
0008 B329h	SCI12	Control field 0 data register	CF0DR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Ah	SCI12	Control field 0 compare enable register	CF0CR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Bh	SCI12	Control field 0 receive data register	CF0RR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId
0008 B32Ch	SCI12	Primary control field 1 data register	PCF1DR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Dh	SCI12	Secondary control field 1 data register	SCF1DR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Eh	SCI12	Control field 1 compare enable register	CF1CR	8	8	2, 3 PCLKB	2 ICLK	
0008 B32Fh	SCI12	Control field 1 receive data register	CF1RR	8	8	2, 3 PCLKB	2 ICLK	
0008 B330h	SCI12	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 B331h	SCI12	Timer mode register	TMR	8	8	2, 3 PCLKB	2 ICLK	
0008 B332h	SCI12	Timer prescaler register	TPRE	8	8	2, 3 PCLKB	2 ICLK	
0008 B333h	SCI12	Timer count register	TCNT	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (31/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C095h	PORTA	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C096h	PORTB	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C097h	PORTB	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C098h	PORTC	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C099h	PORTC	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Ah	PORTD	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Bh	PORTD	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Ch	PORTE	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Dh	PORTE	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Eh	PORTF	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Fh	PORTF	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A0h	PORTG	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A1h	PORTG	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A4h	PORTJ	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A5h	PORTJ	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0C0h	PORT0	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C1h	PORT1	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C2h	PORT2	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C3h	PORT3	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C4h	PORT4	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C5h	PORT5	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C6h	PORT6	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C7h	PORT7	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C8h	PORT8	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C9h	PORT9	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CAh	PORTA	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CBh	PORTB	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CCh	PORTC	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CDh	PORTD	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CEh	PORTE	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CFh	PORTF	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0D0h	PORTG	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0D2h	PORTJ	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E0h	PORT0	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E2h	PORT2	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E5h	PORT5	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E9h	PORT9	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EAh	PORTA	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EBh	PORTB	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0ECh	PORTC	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EDh	PORTD	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EEh	PORTE	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0F0h	PORTG	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C100h	MPC	CS output enable register	PFCSE	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C102h	MPC	CS output pin select register 0	PFCSS0	8	8	2, 3 PCLKB	2 ICLK	
0008 C103h	MPC	CS output pin select register 1	PFCSS1	8	8	2, 3 PCLKB	2 ICLK	
0008 C104h	MPC	Address output enable register 0	PFAOE0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C105h	MPC	Address output enable register 1	PFAOE1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C106h	MPC	External bus control register 0	PFBCR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C107h	MPC	External bus control register 1	PFBCR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C10Eh	MPC	Ethernet control resister 1	PFENET	8	8	2, 3 PCLKB	2 ICLK	

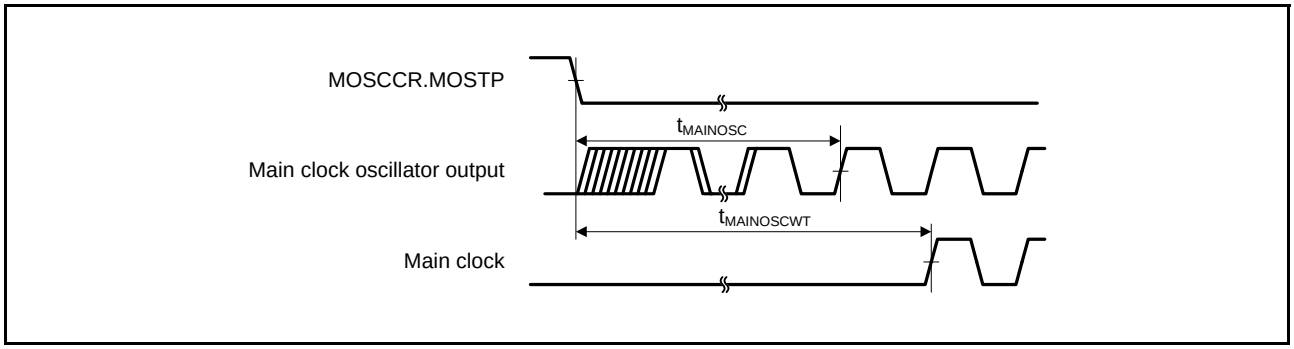


Figure 5.5 Main Clock Oscillation Start Timing

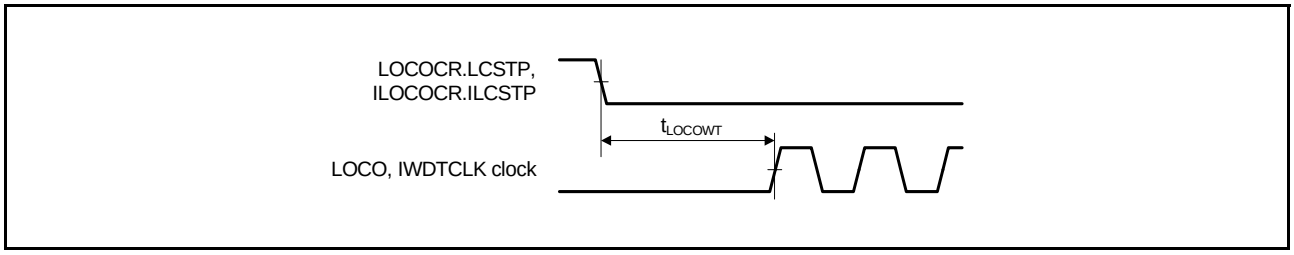


Figure 5.6 LOCO, IWDTCLK Oscillation Start Timing

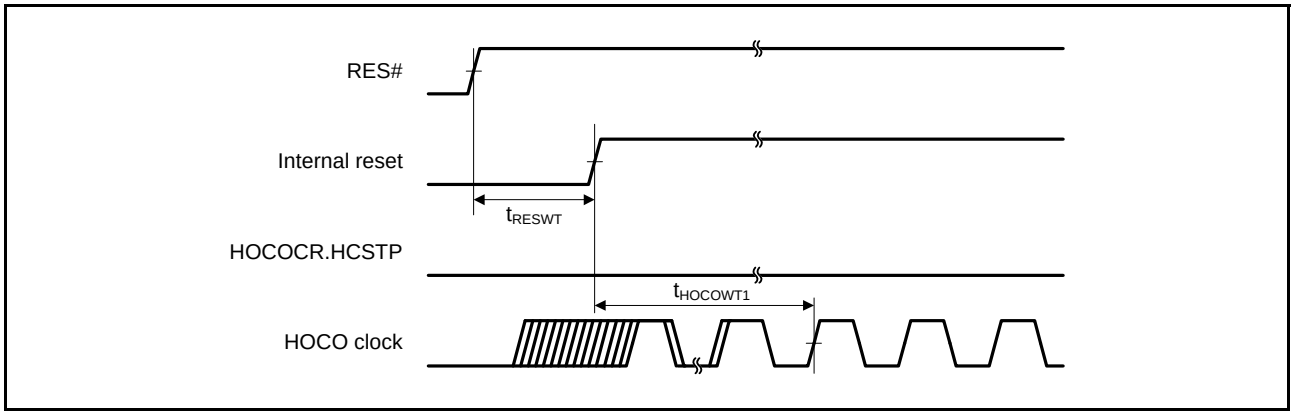


Figure 5.7 HOCO Oscillation Start Timing (After Reset is Canceled by Setting the OFS1.HOCOEN Bit to 0)

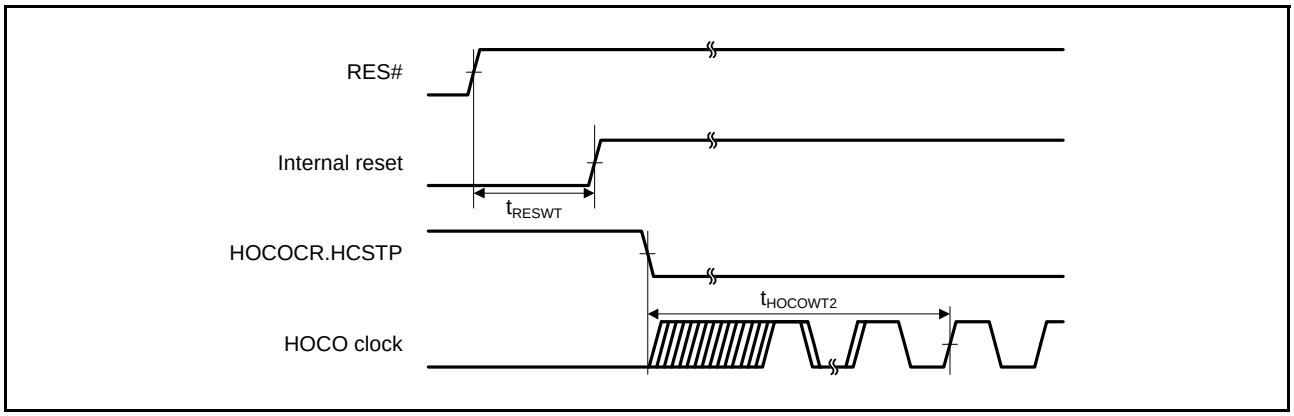


Figure 5.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

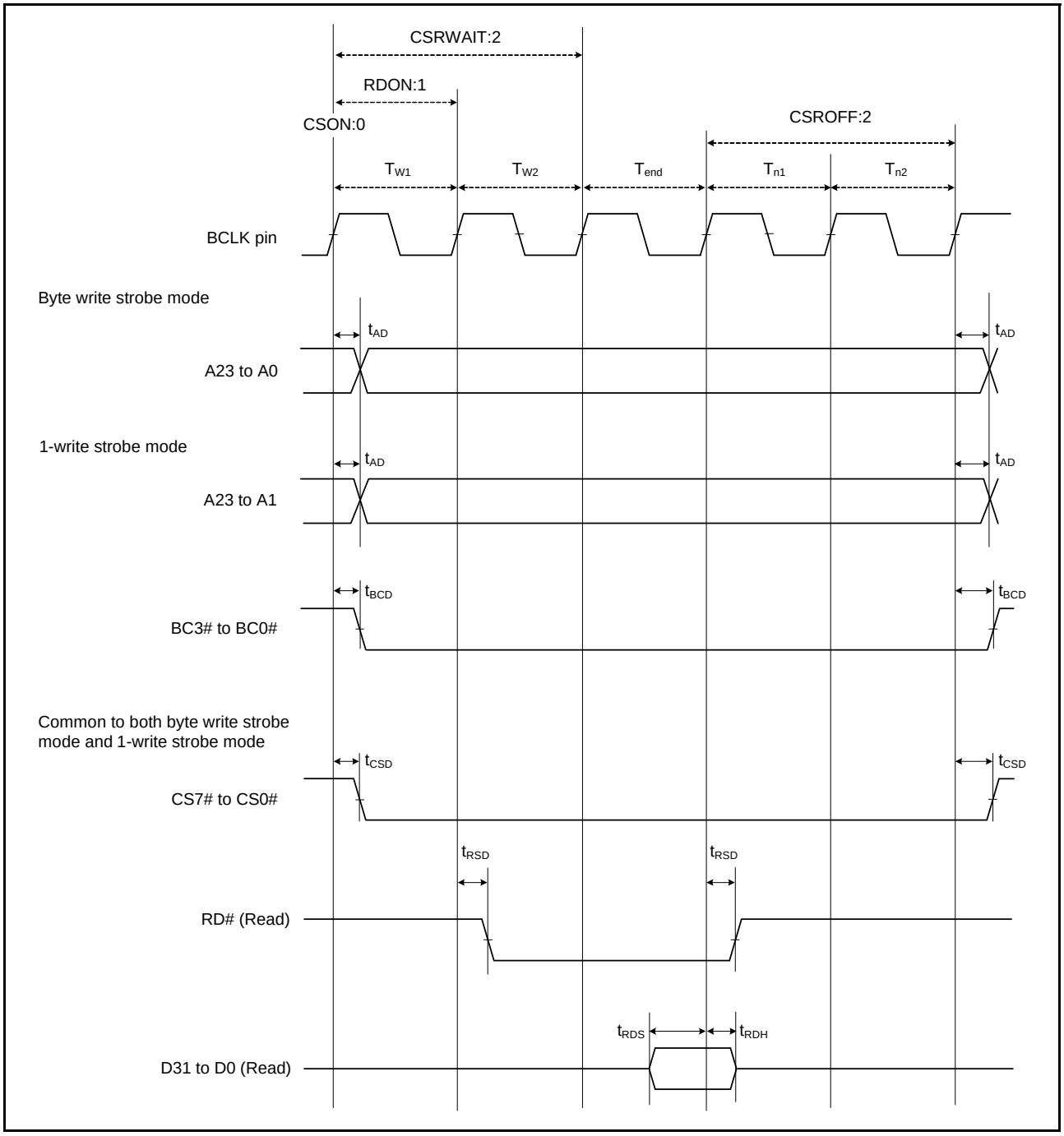
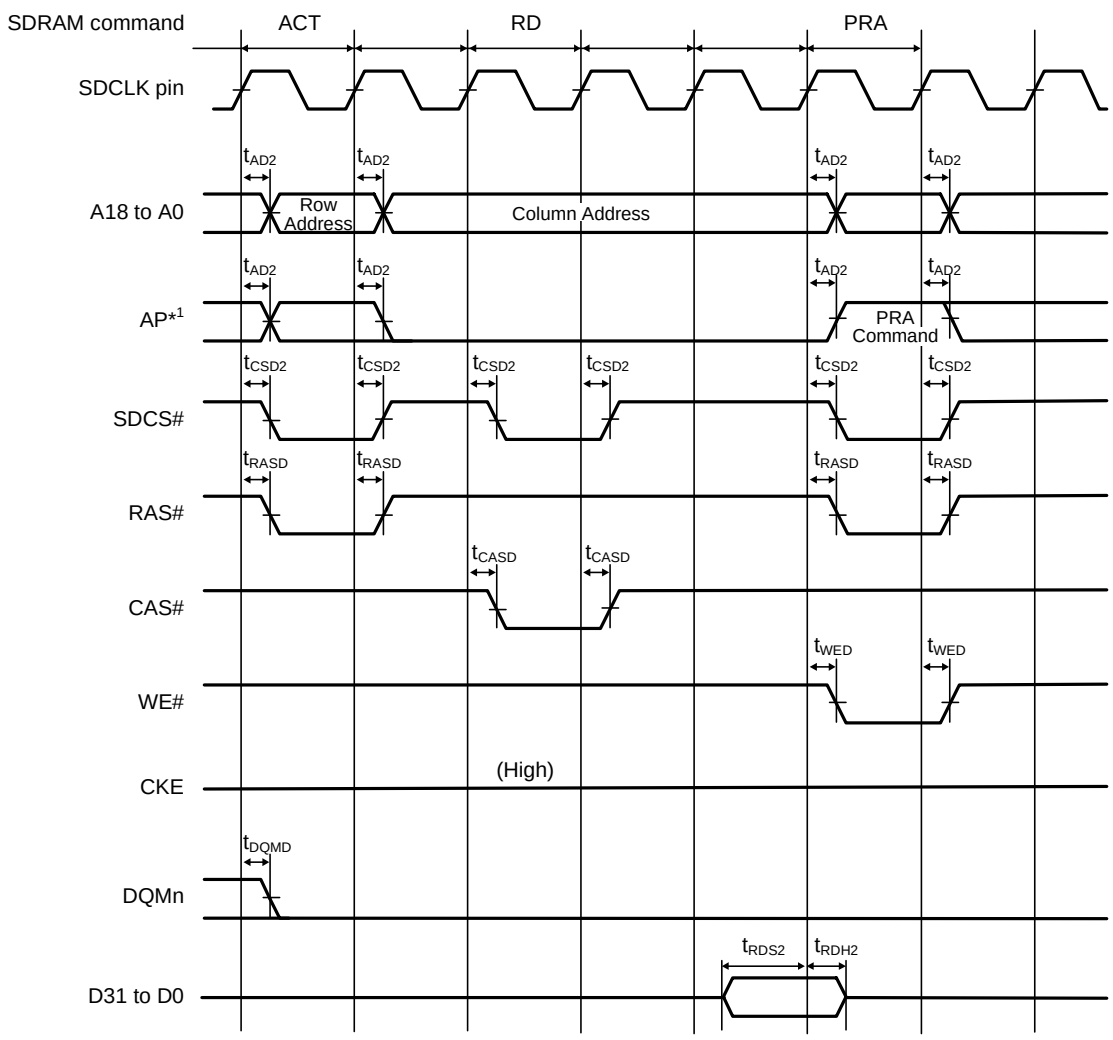


Figure 5.19 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.24 SDRAM Space Single Read Bus Timing

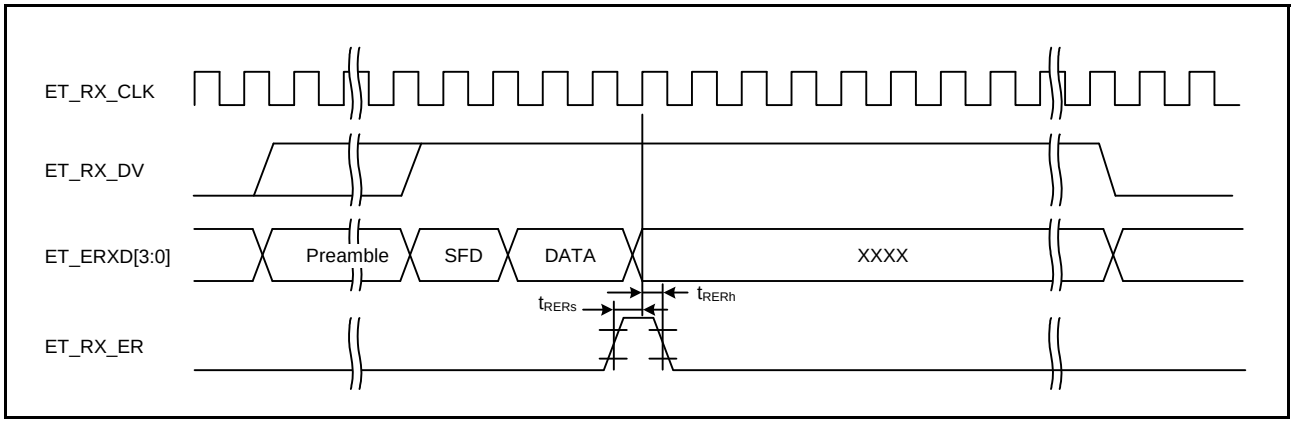


Figure 5.56 MII Reception Timing (Error Occurrence)

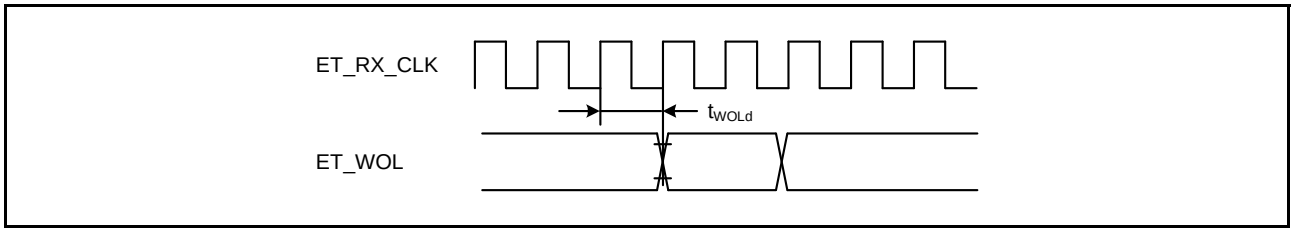


Figure 5.57 WOL Output Timing (MII)

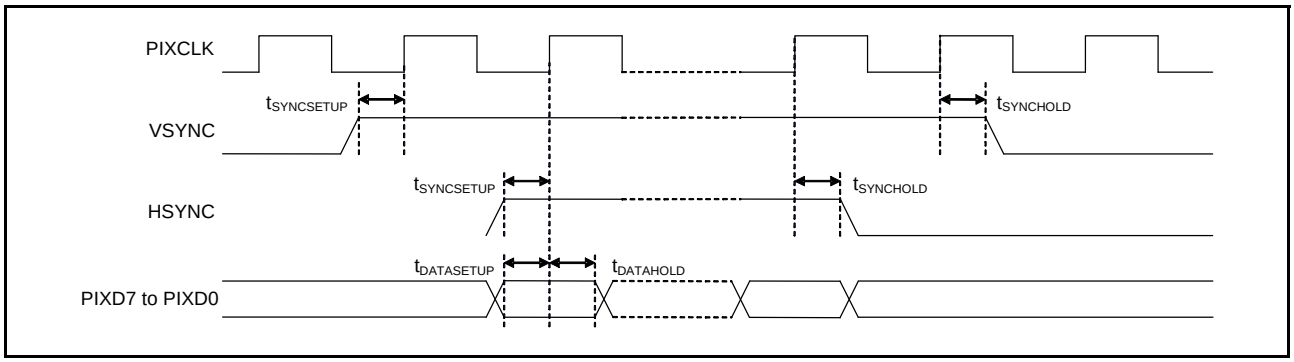


Figure 5.58 PDC Timing

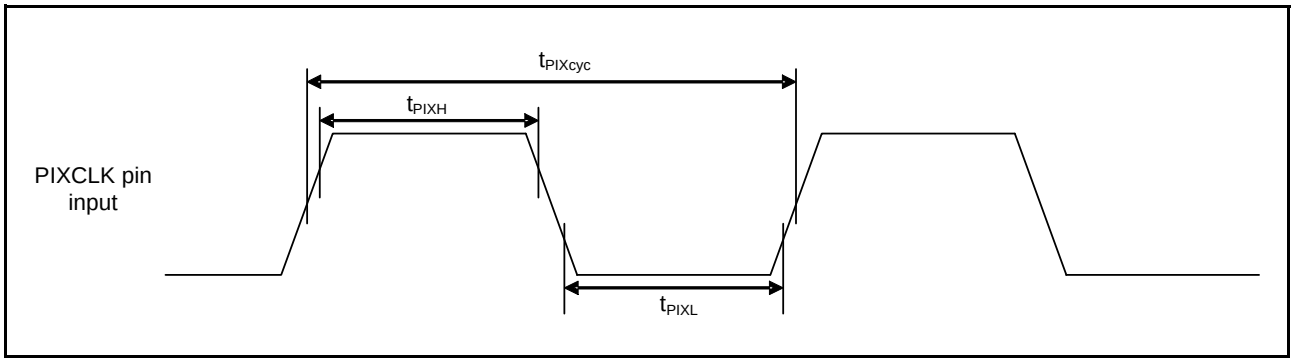


Figure 5.59 PDC Input Clock Characteristic

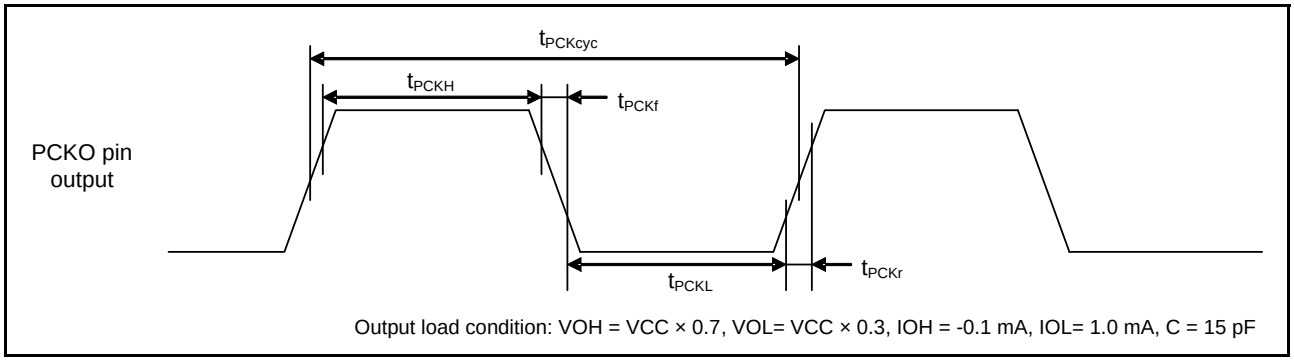


Figure 5.60 PDC Output Clock Characteristic

5.12 E^2 Flash Characteristics

Table 5.38 E2 Flash Characteristics (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V
Temperature range for the programming/erasure operation: $T_a = T_{opr}$

Item	Symbol	min	typ	max	Unit	Condition
Reprogram/erasure cycle*1	N_{DPEC}	100000	—	—	Times	
Data hold time	t_{DDRP}	30*2	—	—	Year	Ta = +85°C

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The result obtained from the reliability test.

Table 5.39 E^2 Flash Characteristics (2)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
Temperature range for the programming/erasure operation: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time $N_{PEC} \leq 100$ times	2 bytes	t_{DP2}	—	0.7	6	—	0.25	2	ms
Programming time $N_{PEC} > 100$ times	2 bytes	t_{DP2}	—	0.7	6	—	0.25	2	ms
Erasure time $N_{PEC} \leq 100$ times	32 bytes	t_{DE32}	—	4	40	—	2	20	ms
Erasure time $N_{PEC} > 100$ times	32 bytes	t_{DE32}	—	7	40	—	4	20	ms
Blank check time	2 bytes	t_{DBC2}	—	—	100	—	—	30	µs
Suspend delay time during programming		t_{DSPD}	—	—	250	—	—	120	µs
First suspend delay time during erasure (in suspend priority mode)		t_{DSESD1}	—	—	250	—	—	120	µs
Second suspend delay time during erasure (in suspend priority mode)		t_{DSESD2}	—	—	500	—	—	300	µs
Suspend delay time during erasure (in erasure priority mode)		t_{DSEED}	—	—	500	—	—	300	µs