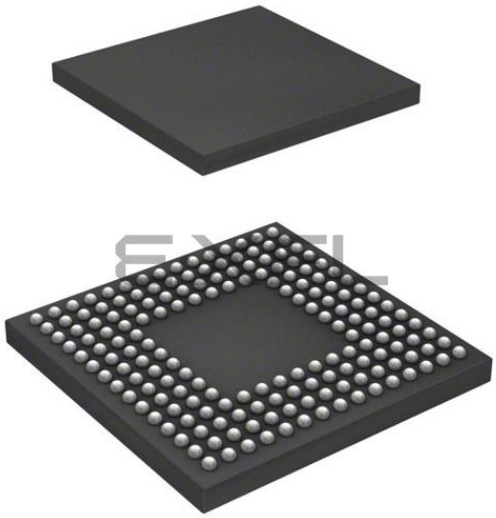
Renesas Electronics America Inc - R5F5631BDDBG#U0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631bddbg-u0

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and table 1.2 gives a comparison of the functions of products in different packages.
Table 1.1 is for products with the greatest number of functions, so numbers of peripheral modules and channels will differ in accord with the package. For details, see Table 1.2, Comparison of Functions for Different Packages in the RX63N/RX631 Group.

Table 1.1 Outline of Specifications (1/6)

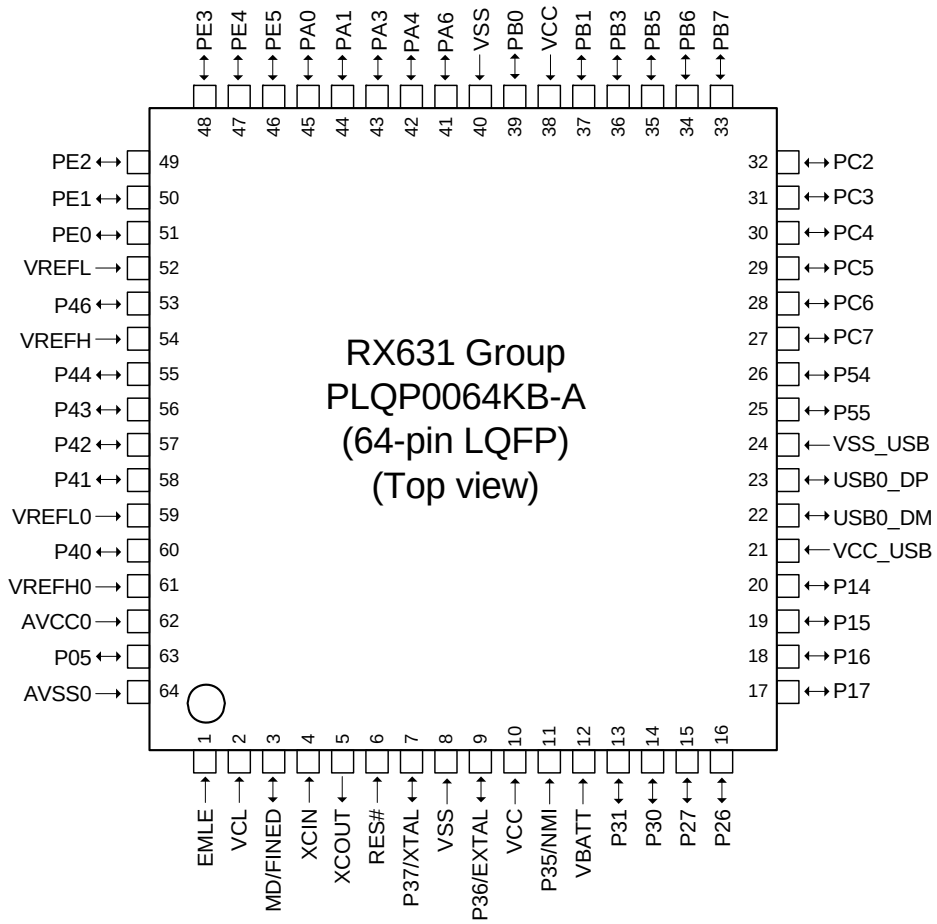
Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 x 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: ROMless, 256 Kbytes, 384 Kbytes, 512 Kbytes, 768 Kbytes, 1 Mbyte, 1.5 Mbytes, 2 Mbytes • 100 MHz, no-wait access • On-board programming: Four types • Off-board programming (parallel programmer mode) (for products with 100 pins or more)
	RAM	• Capacity: 64 Kbytes, 128 Kbytes, 192 Kbytes, 256 Kbytes • 100 MHz, no-wait access
	E2 data flash	Capacity: 32 Kbytes Programming/erasing: 100,000 times
MCU operating modes		Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	• Main clock oscillator, subclock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Main-clock oscillation stoppage detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLK), FlashIF clock (FCLK) and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLK): Up to 50 MHz Flash IF run in synchronization with the flashIF clock (FCLK): Up to 50 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 50 MHz
Reset		RES# pin reset, power-on reset, voltage-monitoring reset, independent watchdog timer reset, watchdog timer reset, deep software standby reset, and software reset
Voltage detection circuit		When the voltage on VCC passes the voltage detection level (Vdet), an internal reset or internal interrupt is generated.

Table 1.1 Outline of Specifications (5/6)

Classification	Module/Function	Description
Communication function	Ethernet controller (ETHERC)	• Input and output of Ethernet/IEEE 802.3 frames • Transfer at 10 or 100 Mbps • Full- and half-duplex modes • MII (Media Independent Interface) or RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u • Detection of Magic Packets™*1 or output of a "wake-on-LAN" signal (WOL) • Compliance with flow control as defined in IEEE 802.3x standards Note 1. Magic PacketTM is a registered trademark of Advanced Micro Devices, Inc.
	DMA controller for Ethernet controller (EDMAC)	• Alleviation of CPU loads by the descriptor control method • Transmission FIFO: 2 Kbytes; Reception FIFO: 2 Kbytes
	USB 2.0 host/function module (USBa)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 • Host/function module: one port, function module: one port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps) • Self-power mode and bus-power mode are selectable • OTG (On the Go) operation is possible • Incorporates 2 Kbytes of RAM as a transfer buffer
	Serial communications interfaces (SCIc, SCId)	• 13 channels (SCIc: 12 channels + SCId: 1 channel) • SCIc Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Simple I^2C Simple SPI • SCId (The following functions are added to SCIc) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	I^2C bus interfaces (RIIC)	• 4 channels (one of them is FM+) • Communication formats I^2C bus format/SMBus format Supports the multi-master Max. transfer rate: 1 Mbps (channel 0)
	IEBus (IEB)	• 1 channel • Supports protocol control for the IEBus Half-duplex asynchronous transfer Multi-master operation Broadcast communications function Two selectable modes, differentiated by transfer rate
	CAN module (CAN)	• 3 channels • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes each
	Serial peripheral interfaces (SPI)	• 3 channels • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure Double buffers for both transmission and reception

Table 1.2 Comparison of Functions for Different Packages in the RX63N/RX631 Group

Functions		RX63N Group			RX631 Group					
Package		177-pin 176-pin	145-pin 144-pin	100-pin	177-pin 176-pin	145-pin 144-pin	100-pin	64-pin LQFP	64-pin TFLGA	48-pin
External bus width	External bus width	32 bits	16 bits		32 bits	16 bits		Not available		
	SDRAM area controller	Available		Not available	Available			Not available		
DMA	DMA controller	Ch. 0 to 3			Ch. 0 to 3					
	EXDMA controller	Ch. 0 and 1			Ch. 0 and 1			Not available		
	Data transfer controller	Available			Available					
Timers	16-bit timer pulse unit	Ch. 0 to 11		Ch. 0 to 5	Ch. 0 to 11			Ch. 0 to 5		
	Multi-function timer pulse unit 2	Ch. 0 to 5			Ch. 0 to 5					
	Port output enable 2	Available			Available					
	Programmable pulse generator	Ch. 0 and 1			Ch. 0 and 1					
	8-bit timers	Ch. 0 to 3			Ch. 0 to 3					
	Compare match timer	Ch. 0 to 3			Ch. 0 to 3					
	Realtime clock	Available			Available					Not available
	Watchdog timer	Available			Available					
	Independent watchdog timer	Available			Available					
Communication function	Ethernet controller	Available			Not available					
	DMA controller for Ethernet controller	Available			Not available					
	USB 2.0 host/function module	Ch. 0 and 1		Ch.0	Ch. 0 and 1		Ch.0		Ch. 0 and 1	Ch.0
	Serial communications interfaces (SCIc)	Ch. 0 to 11		Ch. 0 to 3, 5, 6, 8 and 9	Ch. 0 to 11		Ch. 0 to 3, 5, 6, 8 and 9	Ch. 1, 5, 6, 8 and 9		Ch. 1, 5, 6, and 8
	Serial communications interfaces (SCId)	Ch. 12			Ch. 12					
	I^2C bus interfaces	Ch. 0 to 3		Ch.0 and 2	Ch. 0 to 3		Ch.0 and 2	Ch.2		
	IEBus	Available			Available					
	Serial peripheral interfaces	Ch.0 to 2		Ch. 0 and 1	Ch.0 to 2			Ch. 0 and 1		
	CAN module	For 1.5 M or more: Ch. 0 to 2, For 1 M or less: Ch. 0 and 1		Ch. 0 and 1	For 1.5 M or more: Ch. 0 to 2, For 1 M or less: Ch. 0 and 1		Ch. 0 and 1	Ch.1		
	Parallel data capture unit (PDC)	Not available			Available			Not available		
12-bit A/D converter (channel)		AN000 to 020		AN000 to 013	AN000 to 020		AN000 to 013	AN000 to 004, 006, 008 to 013		AN000 to 002, 006, 009 to 012
10-bit A/D converter (channel)		AN0 to 7			AN0 to 7			Not available		
D/A converter		Ch. 0 and 1		Ch.1	Ch. 0 and 1		Ch.1	Ch.1		Not available
Temperature sensor		Available			Available					
CRC calculator		Available			Available					
Unique ID		Available (only for the G version)								
Off-board programming (parallel programmer mode)		Available						Not available		
Sub-clock oscillator (for low clock loads)		Available						Not available		
Sub-clock oscillator (for standard clock loads)		Available								Not available
Battery backup function		Available								Not available
I/O port switching function		Not available			Not available			Available		



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.12, List of Pins and Pin Functions (64-Pin LQFP).

Figure 1.11 Pin Assignment (64-Pin LQFP)

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (5/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
K2		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/TMO0/ PO2	SCK0/USB0_DRPD		
K3		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID	IRQ8	
K4		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_DPUPE/ USB0_OVRCURA	IRQ4	
K5					USB0_DM		
K6					USB0_DP		
K7		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
K8		PC5	A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	SCK8/RSPCKA/ ET_ETXD2		
K9		PC3	A19	MTIOC4D/ TCLKB/PO24	TXD5/SMOSI5/ SSDA5/IETXD/ ET_TX_ER		
K10		PC2	A18	MTIOC4B/ TCLKA/PO21	RXD5/SMISO5/ SSCL5/SSLA3/ IERXD/ET_RX_DV		

Note 1. Enabled only for the ROM capacity of 768 Kbytes or more.
Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 4.1 List of I/O Registers (Address Order) (11/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 71EEh	ICU	DTC activation enable register 238	DTCER238	8	8	2 ICLK		ICUb
0008 71EFh	ICU	DTC activation enable register 239	DTCER239	8	8	2 ICLK		
0008 71F1h	ICU	DTC activation enable register 241	DTCER241	8	8	2 ICLK		
0008 71F2h	ICU	DTC activation enable register 242	DTCER242	8	8	2 ICLK		
0008 71F4h	ICU	DTC activation enable register 244	DTCER244	8	8	2 ICLK		
0008 71F5h	ICU	DTC activation enable register 245	DTCER245	8	8	2 ICLK		
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2 ICLK		
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2 ICLK		
0008 71FAh	ICU	DTC activation enable register 250	DTCER250	8	8	2 ICLK		
0008 71FBh	ICU	DTC activation enable register 251	DTCER251	8	8	2 ICLK		
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK		
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8	2 ICLK		
0008 7204h	ICU	Interrupt request enable register 04	IER04	8	8	2 ICLK		
0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8	2 ICLK		
0008 7206h	ICU	Interrupt request enable register 06	IER06	8	8	2 ICLK		
0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8	2 ICLK		
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8	2 ICLK		
0008 7209h	ICU	Interrupt request enable register 09	IER09	8	8	2 ICLK		
0008 720Bh	ICU	Interrupt request enable register 0B	IER0B	8	8	2 ICLK		
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8	2 ICLK		
0008 720Dh	ICU	Interrupt request enable register 0D	IER0D	8	8	2 ICLK		
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8	2 ICLK		
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8	2 ICLK		
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8	2 ICLK		
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8	2 ICLK		
0008 7212h	ICU	Interrupt request enable register 12	IER12	8	8	2 ICLK		
0008 7213h	ICU	Interrupt request enable register 13	IER13	8	8	2 ICLK		
0008 7214h	ICU	Interrupt request enable register 14	IER14	8	8	2 ICLK		
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8	2 ICLK		
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8	2 ICLK		
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8	2 ICLK		
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8	2 ICLK		
0008 7219h	ICU	Interrupt request enable register 19	IER19	8	8	2 ICLK		
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8	2 ICLK		
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8	2 ICLK		
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8	2 ICLK		
0008 721Dh	ICU	Interrupt request enable register 1D	IER1D	8	8	2 ICLK		
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8	2 ICLK		
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8	2 ICLK		
0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8	2 ICLK		
0008 72F0h	ICU	Fast interrupt set register	FIR	16	16	2 ICLK		
0008 7300h	ICU	Interrupt source priority register 000	IPR000	8	8	2 ICLK		
0008 7301h	ICU	Interrupt source priority register 001	IPR001	8	8	2 ICLK		
0008 7302h	ICU	Interrupt source priority register 002	IPR002	8	8	2 ICLK		
0008 7303h	ICU	Interrupt source priority register 003	IPR003	8	8	2 ICLK		
0008 7304h	ICU	Interrupt source priority register 004	IPR004	8	8	2 ICLK		
0008 7305h	ICU	Interrupt source priority register 005	IPR005	8	8	2 ICLK		
0008 7306h	ICU	Interrupt source priority register 006	IPR006	8	8	2 ICLK		
0008 7307h	ICU	Interrupt source priority register 007	IPR007	8	8	2 ICLK		
0008 7320h	ICU	Interrupt source priority register 032	IPR032	8	8	2 ICLK		
0008 7321h	ICU	Interrupt source priority register 033	IPR033	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (12/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7322h	ICU	Interrupt source priority register 034	IPR034	8	8	2 ICLK		ICUb
0008 7323h	ICU	Interrupt source priority register 035	IPR035	8	8	2 ICLK		
0008 7324h	ICU	Interrupt source priority register 036	IPR036	8	8	2 ICLK		
0008 7325h	ICU	Interrupt source priority register 037	IPR037	8	8	2 ICLK		
0008 7326h	ICU	Interrupt source priority register 038	IPR038	8	8	2 ICLK		
0008 7327h	ICU	Interrupt source priority register 039	IPR039	8	8	2 ICLK		
0008 732Ah	ICU	Interrupt source priority register 042	IPR042	8	8	2 ICLK		
0008 732Dh	ICU	Interrupt source priority register 045	IPR045	8	8	2 ICLK		
0008 7330h	ICU	Interrupt source priority register 048	IPR048	8	8	2 ICLK		
0008 7334h	ICU	Interrupt source priority register 052	IPR052	8	8	2 ICLK		
0008 7338h	ICU	Interrupt source priority register 056	IPR056	8	8	2 ICLK		
0008 733Eh	ICU	Interrupt source priority register 062	IPR062	8	8	2 ICLK		
0008 7340h	ICU	Interrupt source priority register 064	IPR064	8	8	2 ICLK		
0008 7341h	ICU	Interrupt source priority register 065	IPR065	8	8	2 ICLK		
0008 7342h	ICU	Interrupt source priority register 066	IPR066	8	8	2 ICLK		
0008 7343h	ICU	Interrupt source priority register 067	IPR067	8	8	2 ICLK		
0008 7344h	ICU	Interrupt source priority register 068	IPR068	8	8	2 ICLK		
0008 7345h	ICU	Interrupt source priority register 069	IPR069	8	8	2 ICLK		
0008 7346h	ICU	Interrupt source priority register 070	IPR070	8	8	2 ICLK		
0008 7347h	ICU	Interrupt source priority register 071	IPR071	8	8	2 ICLK		
0008 7348h	ICU	Interrupt source priority register 072	IPR072	8	8	2 ICLK		
0008 7349h	ICU	Interrupt source priority register 073	IPR073	8	8	2 ICLK		
0008 734Ah	ICU	Interrupt source priority register 074	IPR074	8	8	2 ICLK		
0008 734Bh	ICU	Interrupt source priority register 075	IPR075	8	8	2 ICLK		
0008 734Ch	ICU	Interrupt source priority register 076	IPR076	8	8	2 ICLK		
0008 734Dh	ICU	Interrupt source priority register 077	IPR077	8	8	2 ICLK		
0008 734Eh	ICU	Interrupt source priority register 078	IPR078	8	8	2 ICLK		
0008 734Fh	ICU	Interrupt source priority register 079	IPR079	8	8	2 ICLK		
0008 735Ah	ICU	Interrupt source priority register 090	IPR090	8	8	2 ICLK		
0008 735Bh	ICU	Interrupt source priority register 091	IPR091	8	8	2 ICLK		
0008 735Ch	ICU	Interrupt source priority register 092	IPR092	8	8	2 ICLK		
0008 735Dh	ICU	Interrupt source priority register 093	IPR093	8	8	2 ICLK		
0008 7362h	ICU	Interrupt source priority register 098	IPR098	8	8	2 ICLK		
0008 7366h	ICU	Interrupt source priority register 102	IPR102	8	8	2 ICLK		
0008 736Ah	ICU	Interrupt source priority register 106	IPR106	8	8	2 ICLK		
0008 736Bh	ICU	Interrupt source priority register 107	IPR107	8	8	2 ICLK		
0008 736Ch	ICU	Interrupt source priority register 108	IPR108	8	8	2 ICLK		
0008 736Dh	ICU	Interrupt source priority register 109	IPR109	8	8	2 ICLK		
0008 736Eh	ICU	Interrupt source priority register 110	IPR110	8	8	2 ICLK		
0008 736Fh	ICU	Interrupt source priority register 111	IPR111	8	8	2 ICLK		
0008 7370h	ICU	Interrupt source priority register 112	IPR112	8	8	2 ICLK		
0008 7372h	ICU	Interrupt source priority register 114	IPR114	8	8	2 ICLK		
0008 737Ah	ICU	Interrupt source priority register 122	IPR122	8	8	2 ICLK		
0008 737Eh	ICU	Interrupt source priority register 126	IPR126	8	8	2 ICLK		
0008 7382h	ICU	Interrupt source priority register 130	IPR130	8	8	2 ICLK		
0008 7384h	ICU	Interrupt source priority register 132	IPR132	8	8	2 ICLK		
0008 7386h	ICU	Interrupt source priority register 134	IPR134	8	8	2 ICLK		
0008 738Ah	ICU	Interrupt source priority register 138	IPR138	8	8	2 ICLK		
0008 738Ch	ICU	Interrupt source priority register 140	IPR140	8	8	2 ICLK		
0008 738Eh	ICU	Interrupt source priority register 142	IPR142	8	8	2 ICLK		
0008 7392h	ICU	Interrupt source priority register 146	IPR146	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (21/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 83BAh	RSPI1	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	RSPI
0008 83BCh	RSPI1	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 83BEh	RSPI1	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 83C0h	RSPI2	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C1h	RSPI2	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 83C2h	RSPI2	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C3h	RSPI2	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C4h	RSPI2	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 83C8h	RSPI2	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C9h	RSPI2	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83CAh	RSPI2	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 83CBh	RSPI2	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83CCh	RSPI2	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 83CDh	RSPI2	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 83CEh	RSPI2	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 83CFh	RSPI2	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 83D0h	RSPI2	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 83D2h	RSPI2	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 83D4h	RSPI2	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 83D6h	RSPI2	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 83D8h	RSPI2	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	
0008 83DAh	RSPI2	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	
0008 83DCh	RSPI2	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 83DEh	RSPI2	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 8600h	MTU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	MTU2a
0008 8601h	MTU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8602h	MTU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8603h	MTU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8604h	MTU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8605h	MTU3	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8606h	MTU4	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8607h	MTU4	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8608h	MTU3	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8609h	MTU4	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 860Ah	MTU	Timer output master enable register	TOER	8	8	2, 3 PCLKB	2 ICLK	
0008 860Dh	MTU	Timer gate control register	TGCR	8	8	2, 3 PCLKB	2 ICLK	
0008 860Eh	MTU	Timer output control register 1	TOCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 860Fh	MTU	Timer output control register 2	TOCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8610h	MTU3	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8612h	MTU4	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8614h	MTU	Timer cycle data register	TCDR	16	16	2, 3 PCLKB	2 ICLK	
0008 8616h	MTU	Timer dead time data register	TDDR	16	16	2, 3 PCLKB	2 ICLK	
0008 8618h	MTU3	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 861Ah	MTU3	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 861Ch	MTU4	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 861Eh	MTU4	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8620h	MTU	Timer subcounter	TCNTS	16	16	2, 3 PCLKB	2 ICLK	
0008 8622h	MTU	Timer cycle buffer register	TCBR	16	16	2, 3 PCLKB	2 ICLK	
0008 8624h	MTU3	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 8626h	MTU3	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 8628h	MTU4	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (38/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 0000h	USB0	System configuration control register	SYSCFG	16	16	3 to 4 PCLKB	2, 3 ICLK	USBa
000A 0004h	USB0	System configuration status register 0	SYSSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0008h	USB0	Device state control register 0	DVSTCTR0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0014h	USB0	CFIFO port register	CFIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 0018h	USB0	D0FIFO port register	D0FIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 001Ch	USB0	D1FIFO port register	D1FIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 0020h	USB0	CFIFO port select register	CFIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0022h	USB0	CFIFO port control register	CFIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0028h	USB0	D0FIFO port select register	D0FIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 002Ah	USB0	D0FIFO port control register	D0FIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 002Ch	USB0	D1FIFO port select register	D1FIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 002Eh	USB0	D1FIFO port control register	D1FIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0030h	USB0	Interrupt enable register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0032h	USB0	Interrupt enable register 1	INTENB1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0036h	USB0	BRDY interrupt enable register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0038h	USB0	NRDY interrupt enable register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	

Table 4.1 List of I/O Registers (Address Order) (44/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 0230h	USB1	Interrupt enable register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0236h	USB1	BRDY interrupt enable register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0238h	USB1	NRDY interrupt enable register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 023Ah	USB1	BEMP interrupt enable register	BEMPENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 023Ch	USB1	SOF output configuration register	SOFCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0240h	USB1	Interrupt status register 0	INTSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0246h	USB1	BRDY interrupt status register	BRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0248h	USB1	NRDY interrupt status register	NRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	USBa
000A 024Ah	USB1	BEMP interrupt status register	BEMPSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 024Ch	USB1	Frame number register	FRMNUM	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	

Table 4.1 List of I/O Registers (Address Order) (50/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
007F C402h	FLASH	Flash mode register	FMODR	8	8	2 to 4 FCLK	2, 3 ICLK	Flash Memory
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2 to 4 FCLK	2, 3 ICLK	
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2 to 4 FCLK	2, 3 ICLK	
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2 to 4 FCLK	2, 3 ICLK	
007F C440h	FLASH	E2 DataFlash read enable register 0	DFLRE0	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C442h	FLASH	E2 DataFlash read enable register 1	DFLRE1	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C450h	FLASH	E2 DataFlash P/E enable register 0	DFLWE0	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C452h	FLASH	E2 DataFlash P/E enable register 1	DFLWE1	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2 to 4 FCLK	2, 3 ICLK	
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2 to 4 FCLK	2, 3 ICLK	
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFCAh	FLASH	E2 data flash blank check control register	DFLBCCNT	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFCEh	FLASH	E2 DataFlash blank check status register	DFLBCSTAT	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2 to 4 FCLK	2, 3 ICLK	
FEFF FAC0h	FLASH	Unique ID register 0*8	UIDR0	8	8	1 ICLK	1 ICLK	
FEFF FAC1h	FLASH	Unique ID register 1*8	UIDR1	8	8	1 ICLK	1 ICLK	
FEFF FAC2h	FLASH	Unique ID register 2*8	UIDR2	8	8	1 ICLK	1 ICLK	
FEFF FAC3h	FLASH	Unique ID register 3*8	UIDR3	8	8	1 ICLK	1 ICLK	
FEFF FAC4h	FLASH	Unique ID register 4*8	UIDR4	8	8	1 ICLK	1 ICLK	
FEFF FAC5h	FLASH	Unique ID register 5*8	UIDR5	8	8	1 ICLK	1 ICLK	
FEFF FAC6h	FLASH	Unique ID register 6*8	UIDR6	8	8	1 ICLK	1 ICLK	
FEFF FAC7h	FLASH	Unique ID register 7*8	UIDR7	8	8	1 ICLK	1 ICLK	
FEFF FAC8h	FLASH	Unique ID register 8*8	UIDR8	8	8	1 ICLK	1 ICLK	
FEFF FAC9h	FLASH	Unique ID register 9*8	UIDR9	8	8	1 ICLK	1 ICLK	
FEFF FACAh	FLASH	Unique ID register 10*8	UIDR10	8	8	1 ICLK	1 ICLK	
FEFF FACBh	FLASH	Unique ID register 11*8	UIDR11	8	8	1 ICLK	1 ICLK	
FEFF FACCh	FLASH	Unique ID register 12*8	UIDR12	8	8	1 ICLK	1 ICLK	
FEFF FACDh	FLASH	Unique ID register 13*8	UIDR13	8	8	1 ICLK	1 ICLK	
FEFF FACEh	FLASH	Unique ID register 14*8	UIDR14	8	8	1 ICLK	1 ICLK	
FEFF FACFh	FLASH	Unique ID register 15*8	UIDR15	8	8	1 ICLK	1 ICLK	
FEFF FAD2h	TEMPS	Temperature sensor calibration data register*8	TSCDRL	8	8	1 ICLK	1 ICLK	Temperature sensor
FEFF FAD3h	TEMPS	Temperature sensor calibration data register*8	TSCDRH	8	8	1 ICLK	1 ICLK	

Note 1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 000881ECh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 000881EEh and 000881ECh, respectively.

Note 2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRL address is 000881EDh. When different output triggers are specified, the PPG0.NDRL addresses for pulse output groups 0 and 1 are 000881EFh and 000881EDh, respectively.

Note 3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 000881FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 000881FEh and 000881FCh, respectively.

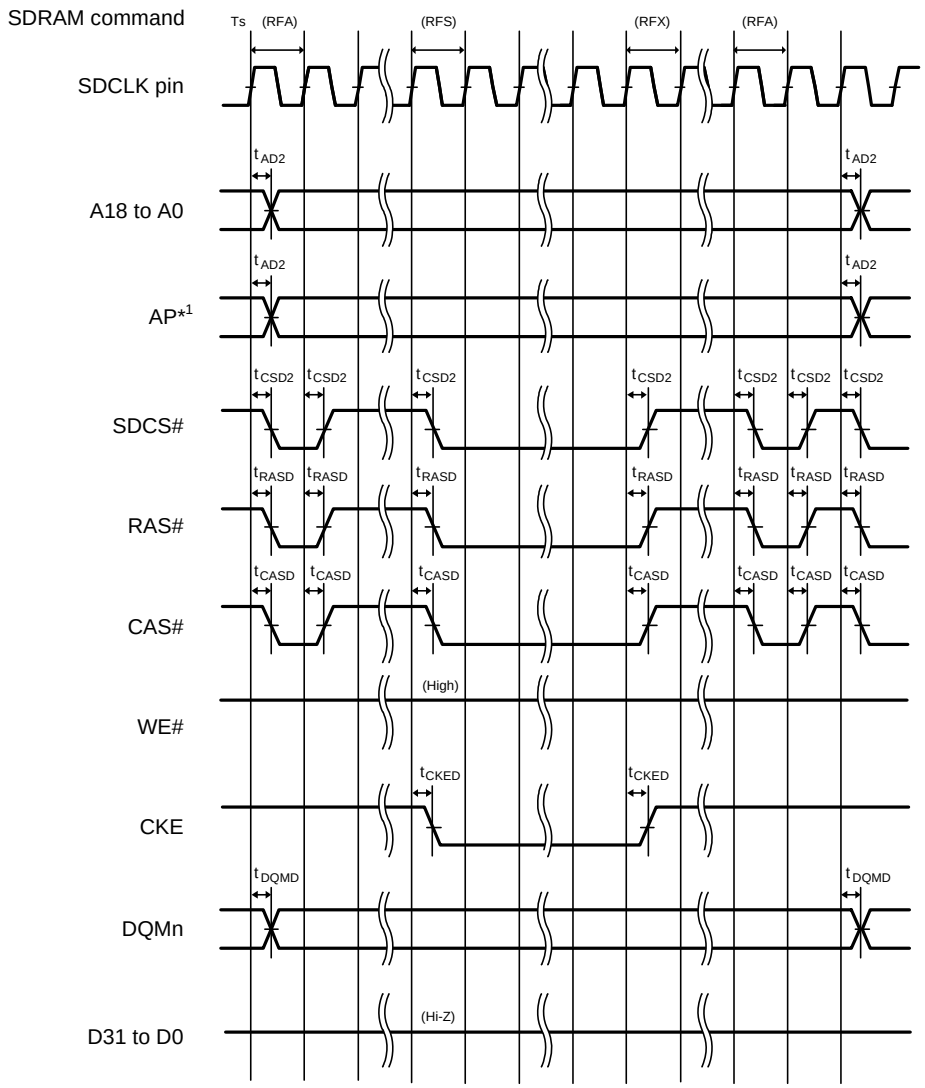
Note 4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRL address is 000881FDh. When different output triggers are specified, the PPG1.NDRL addresses for pulse output groups 4 and 5 are 000881FFh and 000881FDh, respectively.

Note 5. Odd addresses should not be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register. Table 27.4 lists register allocation for 16-bit access in the User's manual: Hardware.

Note 6. When the register is accessed while the USB is operating, a delay may be generated in accessing.

Note 7. The addresses with odd number cannot be accessed in 16-bit units. 16-bit access to a register should be made to the addresses of the TMOCNTL register. Allocation of registers to be accessed in 16-bit units is described in the Table 36.6, Allocation of Registers to be Accessed in 16-bit Units in the User's manual: Hardware.

Note 8. These registers are only present in the G version.



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.30 SDRAM Space Self-Refresh Bus Timing

Table 5.21 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V*1, VREFH0 = 2.7 V to AVCC0*1,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V,
PCLK = 8 to 50 MHz,
$T_a = T_{opr}$
High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit*2	Test Conditions
RSPI	Data output delay time	Master	Packages with 177 to 144 pins	t_{OD}	—	18	ns	Figure 5.43 to Figure 5.46 C = 30pF
			Packages with 100 pins or less		—	30		
		Slave	Packages with 177 to 144 pins		—	3 × t_{Pcyc} + 40		
			Packages with 100 pins or less		—	3 × t_{Pcyc} + 50		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave			4 × t_{Pcyc}	—		
	MOSI and MISO rise/fall time	Output	Packages with 177 to 144 pins	t_{Dr}, t_{Df}	—	5	ns	
			Packages with 100 pins or less		—	10		
		Input			—	1	µs	
	SSL rise/fall time	Output	Packages with 177 to 144 pins	t_{SSLr}, t_{SSLf}	—	5	ns	
			Packages with 100 pins or less		—	10		
		Input			—	1	µs	
	Slave access time			t_{SA}	—	4	t_{Pcyc}	Figure 5.45 and Figure 5.46 C = 30pF
	Slave output release time			t_{REL}	—	3	t_{Pcyc}	

Note 1. When operation at 3.0 V or a lower voltage is needed, please contact a Renesas sales office.
Note 2. t_{Pcyc}: PCLK cycle

Table 5.23 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a = T_{opr}$
High drive output is selected by the drive capacity control register.

Item		Symbol	Min.*1,*2	Max.*	Unit	Test Conditions
RIIC (Standard-mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 1300$	—	ns	Figure 5.47
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 600$	—	ns	
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICϕ) Cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. Cb is the total capacitance of the bus lines.

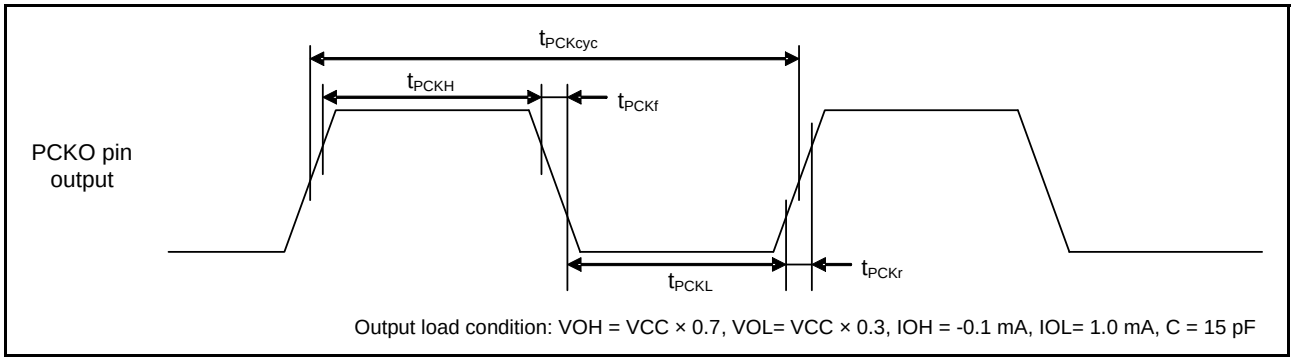


Figure 5.60 PDC Output Clock Characteristic

5.9 Oscillation Stop Detection Timing

Table 5.34 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.67

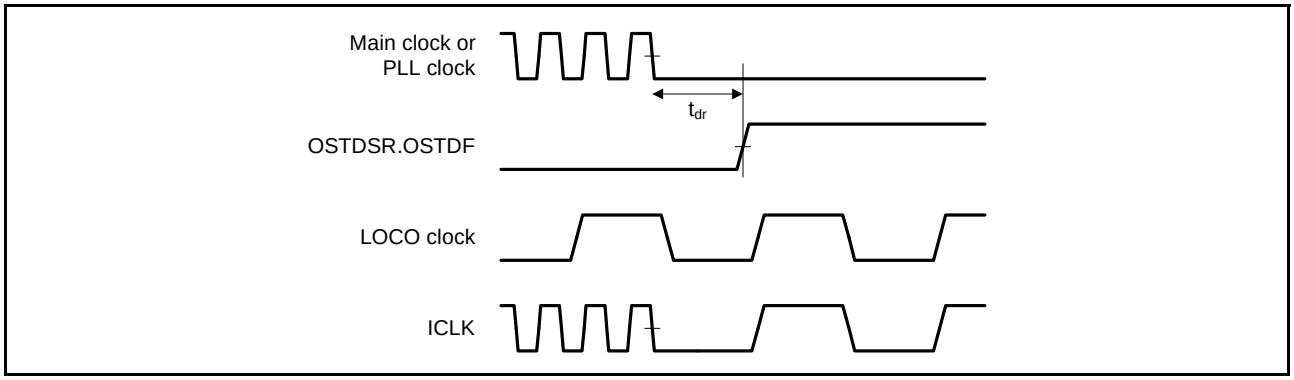


Figure 5.67 Oscillation Stop Detection Timing

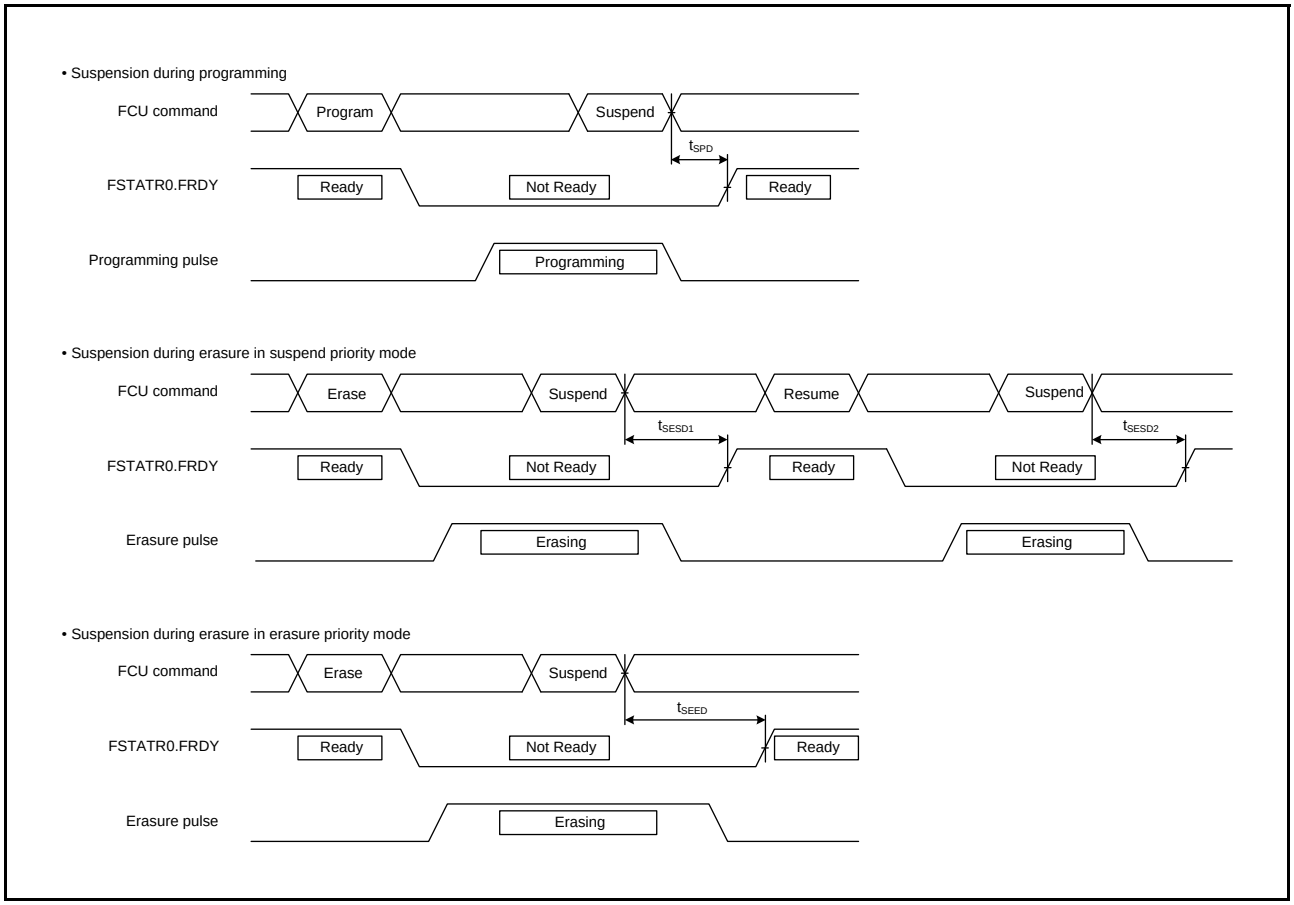


Figure 5.69 Flash Memory Program/Erase Suspend Timing

5.13 Boundary Scan

Table 5.40 Boundary Scan

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 5.70
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TRST# pulse width	t_{TRSTW}	20	—	—	t_{TCKcyc}	Figure 5.71
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 5.72
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	40	ns	

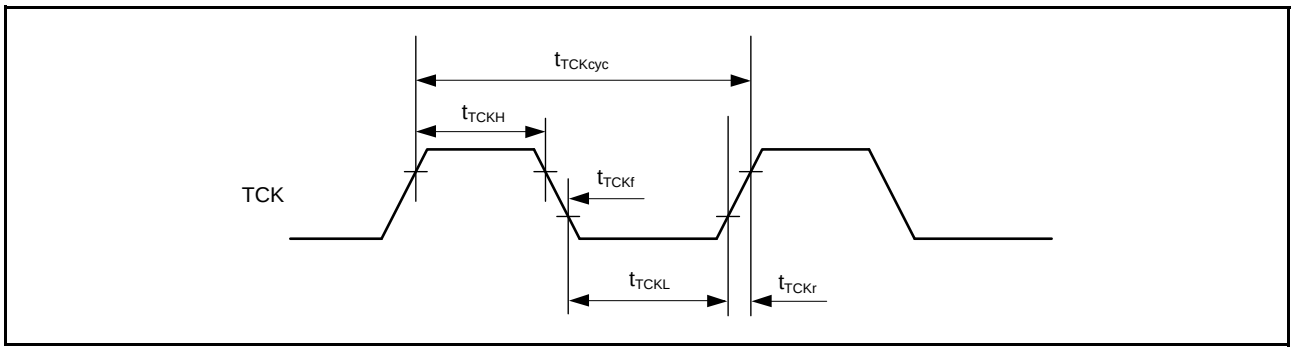


Figure 5.70 Boundary Scan TCK Timing

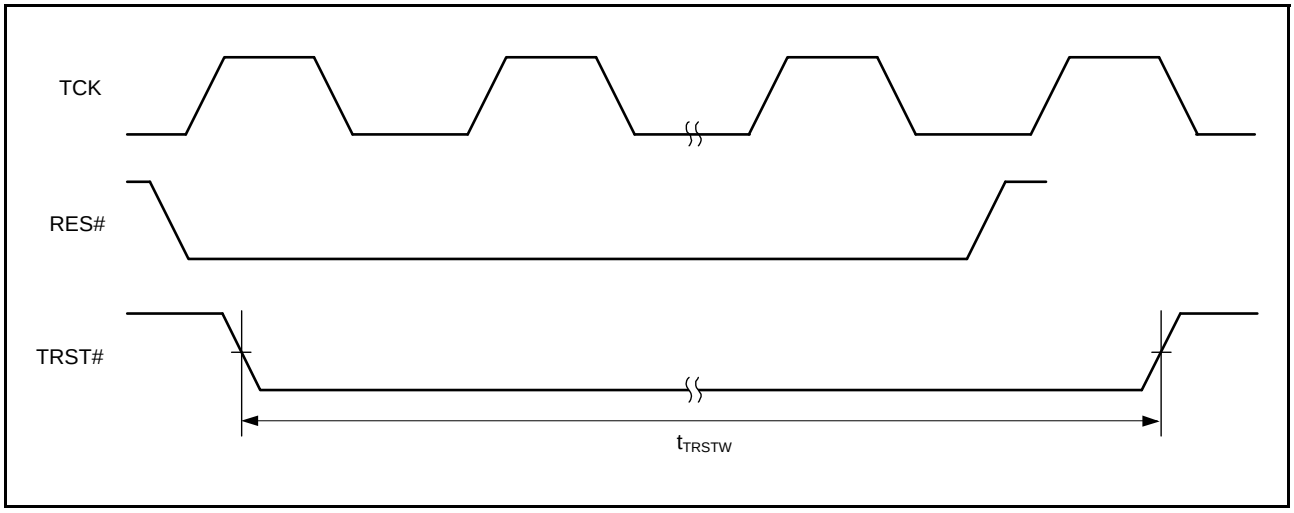
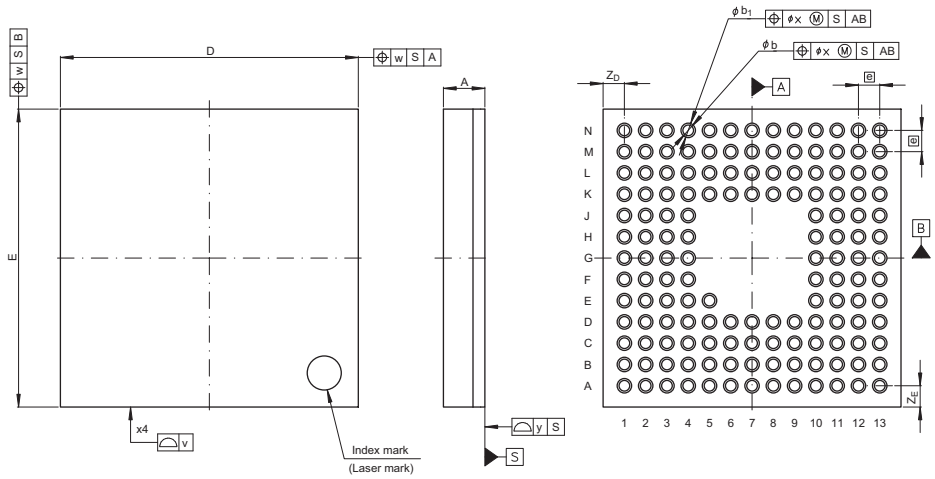


Figure 5.71 Boundary Scan TRST# Timing

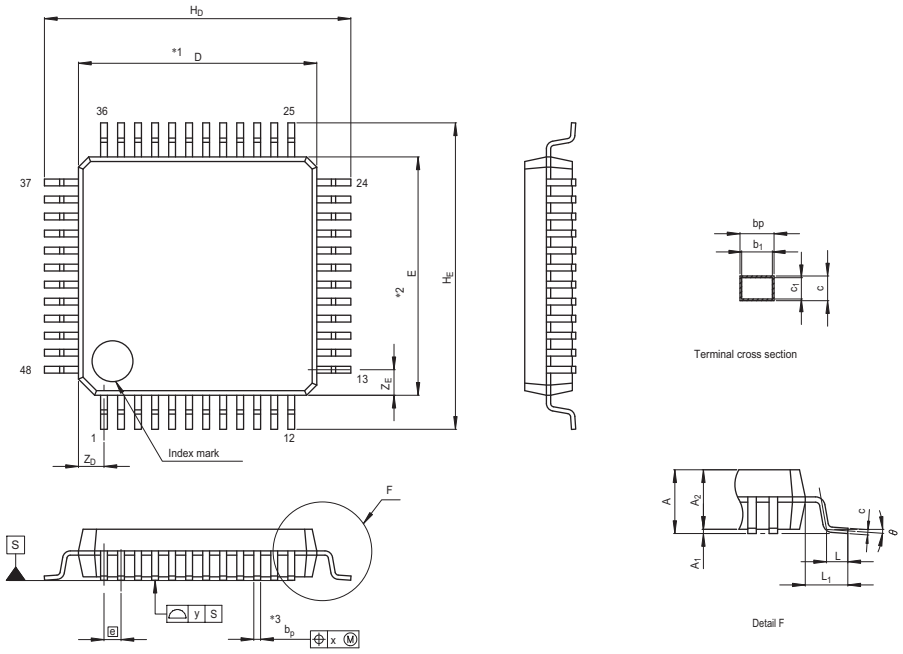
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA145-7x7-0.50	PTLG0145KA-A	145F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure D 145-pin TFLGA (PTLG0145KA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure J 48-pin LQFP (PLQP0048KB-A)