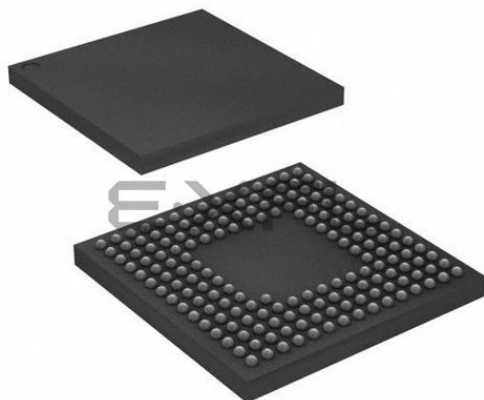




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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	177-TFLGA
Supplier Device Package	177-TFLGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631bddlc-u0

Table 1.1 Outline of Specifications (6/6)

Classification	Module/Function	Description
Communication function	Parallel data capture unit (PDC)	1 channel - Communicates with an image sensor or other external I/Os and transfer parallel data such as an image output from those devices to internal RAM or external address spaces (CS space and SDRAM space) through DTC or DMAC.
12-bit A/D converter (S12ADa)		1 unit (1 unit x 21 channels) 12-bit resolution - Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz) - Operating mode - Scan mode (single scan mode or continuous scan mode) - Sample-and-hold function - Reference voltage generation - Three ways to start A/D conversion - Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal. - A/D conversion of the temperature sensor output
10-bit A/D converter (ADb)		1 unit (1 unit x 8 channels) 10-bit resolution - Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz) - Operating mode - Scan mode (single scan mode or continuous scan mode) - External amplifier connection mode - Sample-and-hold function - Three ways to start A/D conversion - Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal.
D/A converter (DAa)		2 channels 10-bit resolution - Output voltage: 0 V to VREFH
Temperature sensor		1 channel - Precision: $\pm 1^{\circ}\text{C}$ - The voltage of the temperature is converted into a digital value by the 12-bit A/D converter.
CRC calculator (CRC)		- CRC code generation for arbitrary amounts of data in 8-bit units - Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. - Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
Unique ID		A 16-byte device-specific ID (only for the G version)
Data encryption unit (DEU)*1		- AES encryption and decryption functions 128/192/256-bit key length - ECB/CBC mode
Operating frequency		Up to 100 MHz
Power supply voltage		VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0, V _{BATT} = 2.0 V to 3.6 V (for products with 100 or more pins), V _{BATT} = 2.3 V to 3.6 V (for the 64-pin product)
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C*2
Package		177-pin TFLGA (PTLG0177KA-A) 176-pin LFBGA (PLBG0176GA-A) 176-pin LQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) 144-pin LQFP (PLQP0144KA-A) 100-pin TFLGA (PTLG0100JA-A) (in the planning stage) 100-pin LQFP (PLQP0100KB-A) 64-pin TFLGA (PTLG0064JA-A) 64-pin LQFP (PLQP0064KB-A) 48-pin LQFP (PLQP0048KB-A)
On-chip debugging system		- E1 emulator (JTAG and FINE interfaces) - E20 emulator (JTAG interface)

Note 1. Please contact our sales office for more information.

Note 2. Please contact us if you are using a G version.

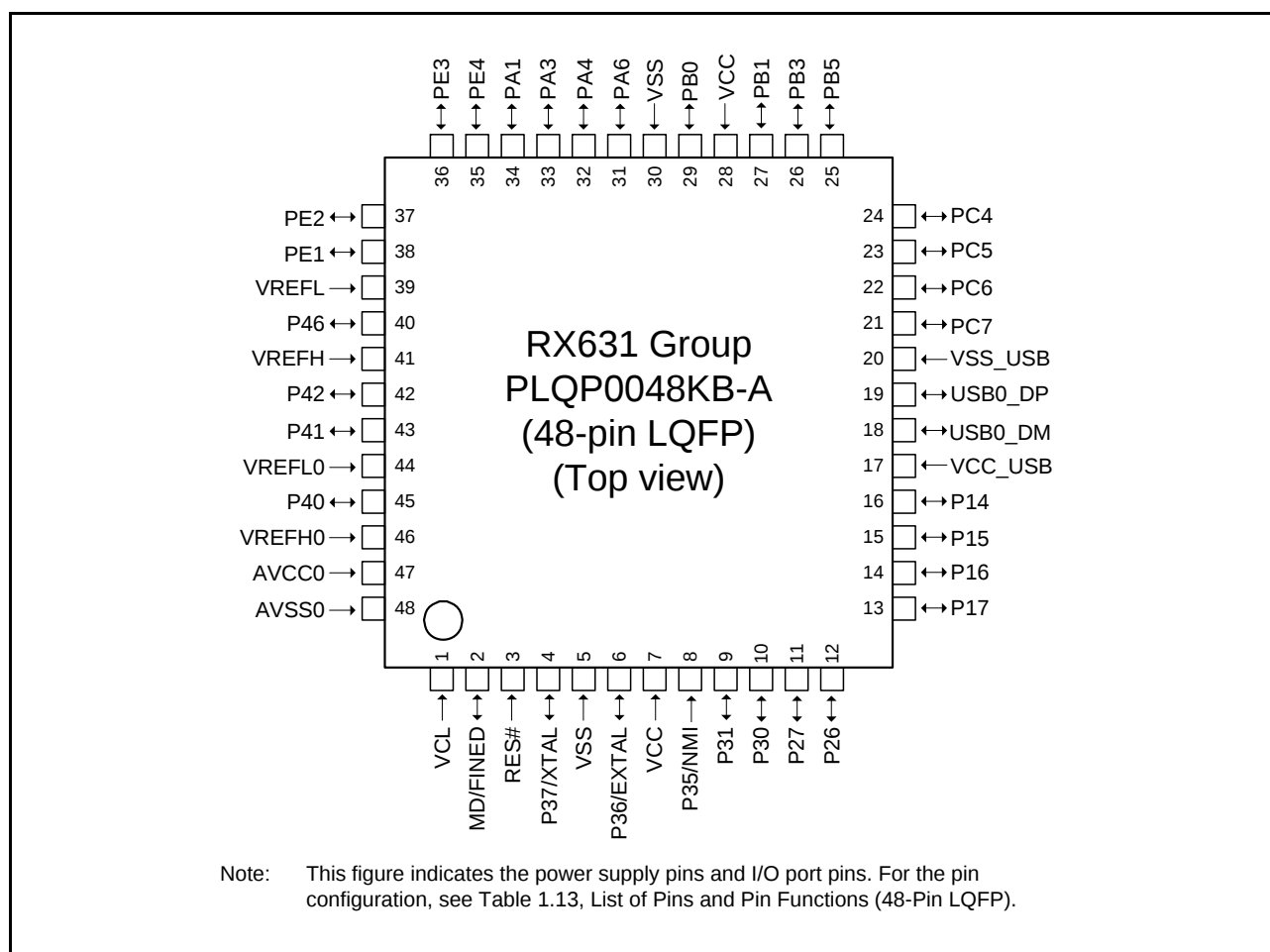


Figure 1.12 Pin Assignment (48-Pin LQFP)

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (5/5)

Pin No. 144-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
125		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
126		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
127		P93	A19		CTS7#/RTS7#/SS7#		AN017
128		P92	A18		RXD7/SMISO7/SSCL7		AN016
129		P91	A17		SCK7		AN015
130	VSS						
131		P90	A16		TXD7/SMOSI7/SSDA7		AN014
132	VCC						
133		P47				IRQ15-DS	AN007
134		P46				IRQ14-DS	AN006
135		P45				IRQ13-DS	AN005
136		P44				IRQ12-DS	AN004
137		P43				IRQ11-DS	AN003
138		P42				IRQ10-DS	AN002
139		P41				IRQ9-DS	AN001
140	VREFL0						
141		P40				IRQ8-DS	AN000
142	VREFH0						
143	AVCC0						
144		P07				IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 4.1 List of I/O Registers (Address Order) (13/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7394h	ICU	Interrupt source priority register 148	IPR148	8	8	2 ICLK		ICUb
0008 7396h	ICU	Interrupt source priority register 150	IPR150	8	8	2 ICLK		
0008 7398h	ICU	Interrupt source priority register 152	IPR152	8	8	2 ICLK		
0008 739Ch	ICU	Interrupt source priority register 156	IPR156	8	8	2 ICLK		
0008 73A0h	ICU	Interrupt source priority register 160	IPR160	8	8	2 ICLK		
0008 73A1h	ICU	Interrupt source priority register 161	IPR161	8	8	2 ICLK		
0008 73A4h	ICU	Interrupt source priority register 164	IPR164	8	8	2 ICLK		
0008 73A6h	ICU	Interrupt source priority register 166	IPR166	8	8	2 ICLK		
0008 73AAh	ICU	Interrupt source priority register 170	IPR170	8	8	2 ICLK		
0008 73ADh	ICU	Interrupt source priority register 173	IPR173	8	8	2 ICLK		
0008 73B0h	ICU	Interrupt source priority register 176	IPR176	8	8	2 ICLK		
0008 73B3h	ICU	Interrupt source priority register 179	IPR179	8	8	2 ICLK		
0008 73B6h	ICU	Interrupt source priority register 182	IPR182	8	8	2 ICLK		
0008 73B7h	ICU	Interrupt source priority register 183	IPR183	8	8	2 ICLK		
0008 73B8h	ICU	Interrupt source priority register 184	IPR184	8	8	2 ICLK		
0008 73B9h	ICU	Interrupt source priority register 185	IPR185	8	8	2 ICLK		
0008 73BAh	ICU	Interrupt source priority register 186	IPR186	8	8	2 ICLK		
0008 73BBh	ICU	Interrupt source priority register 187	IPR187	8	8	2 ICLK		
0008 73BCh	ICU	Interrupt source priority register 188	IPR188	8	8	2 ICLK		
0008 73BDh	ICU	Interrupt source priority register 189	IPR189	8	8	2 ICLK		
0008 73BEh	ICU	Interrupt source priority register 190	IPR190	8	8	2 ICLK		
0008 73BFh	ICU	Interrupt source priority register 191	IPR191	8	8	2 ICLK		
0008 73C0h	ICU	Interrupt source priority register 192	IPR192	8	8	2 ICLK		
0008 73C1h	ICU	Interrupt source priority register 193	IPR193	8	8	2 ICLK		
0008 73C2h	ICU	Interrupt source priority register 194	IPR194	8	8	2 ICLK		
0008 73C3h	ICU	Interrupt source priority register 195	IPR195	8	8	2 ICLK		
0008 73C4h	ICU	Interrupt source priority register 196	IPR196	8	8	2 ICLK		
0008 73C5h	ICU	Interrupt source priority register 197	IPR197	8	8	2 ICLK		
0008 73C6h	ICU	Interrupt source priority register 198	IPR198	8	8	2 ICLK		
0008 73C7h	ICU	Interrupt source priority register 199	IPR199	8	8	2 ICLK		
0008 73C8h	ICU	Interrupt source priority register 200	IPR200	8	8	2 ICLK		
0008 73C9h	ICU	Interrupt source priority register 201	IPR201	8	8	2 ICLK		
0008 73CAh	ICU	Interrupt source priority register 202	IPR202	8	8	2 ICLK		
0008 73CBh	ICU	Interrupt source priority register 203	IPR203	8	8	2 ICLK		
0008 73CEh	ICU	Interrupt source priority register 206	IPR206	8	8	2 ICLK		
0008 73CFh	ICU	Interrupt source priority register 207	IPR207	8	8	2 ICLK		
0008 73D0h	ICU	Interrupt source priority register 208	IPR208	8	8	2 ICLK		
0008 73D6h	ICU	Interrupt source priority register 214	IPR214	8	8	2 ICLK		
0008 73D9h	ICU	Interrupt source priority register 217	IPR217	8	8	2 ICLK		
0008 73DCh	ICU	Interrupt source priority register 220	IPR220	8	8	2 ICLK		
0008 73DFh	ICU	Interrupt source priority register 223	IPR223	8	8	2 ICLK		
0008 73E2h	ICU	Interrupt source priority register 226	IPR226	8	8	2 ICLK		
0008 73E5h	ICU	Interrupt source priority register 229	IPR229	8	8	2 ICLK		
0008 73E8h	ICU	Interrupt source priority register 232	IPR232	8	8	2 ICLK		
0008 73EBh	ICU	Interrupt source priority register 235	IPR235	8	8	2 ICLK		
0008 73EEh	ICU	Interrupt source priority register 238	IPR238	8	8	2 ICLK		
0008 73F1h	ICU	Interrupt source priority register 241	IPR241	8	8	2 ICLK		
0008 73F4h	ICU	Interrupt source priority register 244	IPR244	8	8	2 ICLK		
0008 73F7h	ICU	Interrupt source priority register 247	IPR247	8	8	2 ICLK		
0008 73FAh	ICU	Interrupt source priority register 250	IPR250	8	8	2 ICLK		
0008 73FDh	ICU	Interrupt source priority register 253	IPR253	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (14/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function	
						ICLK≥PCLK	ICLK<PCLK		
0008 7400h	ICU	DMAC activation request select register 0	DMRSR0	8	8	2 ICLK		ICUb	
0008 7404h	ICU	DMAC activation request select register 1	DMRSR1	8	8	2 ICLK			
0008 7408h	ICU	DMAC activation request select register 2	DMRSR2	8	8	2 ICLK			
0008 740Ch	ICU	DMAC activation request select register 3	DMRSR3	8	8	2 ICLK			
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8	2 ICLK			
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8	2 ICLK			
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8	2 ICLK			
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8	2 ICLK			
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8	2 ICLK			
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK			
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8	2 ICLK			
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8	2 ICLK			
0008 7508h	ICU	IRQ control register 8	IRQCR8	8	8	2 ICLK			
0008 7509h	ICU	IRQ control register 9	IRQCR9	8	8	2 ICLK			
0008 750Ah	ICU	IRQ control register 10	IRQCR10	8	8	2 ICLK			
0008 750Bh	ICU	IRQ control register 11	IRQCR11	8	8	2 ICLK			
0008 750Ch	ICU	IRQ control register 12	IRQCR12	8	8	2 ICLK			
0008 750Dh	ICU	IRQ control register 13	IRQCR13	8	8	2 ICLK			
0008 750Eh	ICU	IRQ control register 14	IRQCR14	8	8	2 ICLK			
0008 750Fh	ICU	IRQ control register 15	IRQCR15	8	8	2 ICLK			
0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8	2 ICLK			
0008 7511h	ICU	IRQ pin digital filter enable register 1	IRQFLTE1	8	8	2 ICLK			
0008 7514h	ICU	IRQ pin digital filter setting register 0	IRQFLTC0	16	16	2 ICLK			
0008 7516h	ICU	IRQ pin digital filter setting register 1	IRQFLTC1	16	16	2 ICLK			
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK			
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK			
0008 7582h	ICU	Non-maskable interrupt status clear register	NMICLR	8	8	2 ICLK			
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK			
0008 7590h	ICU	NMI pin digital filter enable register	NMIFLTE	8	8	2 ICLK			
0008 7594h	ICU	NMI pin digital filter setting register	NMIFLTC	16	16	2 ICLK			
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT	
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK		
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8020h	WDT	WDT refresh register	WDTRR	8	8	2, 3 PCLKB	2 ICLK		WDTA
0008 8022h	WDT	WDT control register	WDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8024h	WDT	WDT status register	WDTSR	16	16	2, 3 PCLKB	2 ICLK		
0008 8026h	WDT	WDT reset control register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK		
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (17/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 81A8h	TPU8	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 81AAh	TPU8	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81B0h	TPU9	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B1h	TPU9	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B2h	TPU9	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 81B3h	TPU9	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 81B4h	TPU9	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81B5h	TPU9	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B6h	TPU9	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81B8h	TPU9	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81BAh	TPU9	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81BCh	TPU9	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 81BEh	TPU9	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 81C0h	TPU10	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C1h	TPU10	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C2h	TPU10	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C4h	TPU10	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81C5h	TPU10	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C6h	TPU10	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81C8h	TPU10	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81CAh	TPU10	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81D0h	TPU11	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D1h	TPU11	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D2h	TPU11	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D4h	TPU11	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81D5h	TPU11	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D6h	TPU11	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81D8h	TPU11	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81DAh	TPU11	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81E6h	PPG0	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E7h	PPG0	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81E8h	PPG0	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81E9h	PPG0	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EAh	PPG0	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EBh	PPG0	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81ECh ^{*1}	PPG0	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EDh ^{*2}	PPG0	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EEh ^{*1}	PPG0	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	
0008 81EFh ^{*2}	PPG0	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	
0008 81F0h	PPG1	PPG trigger select register	PTRSLR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F6h	PPG1	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F7h	PPG1	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F8h	PPG1	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81F9h	PPG1	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FAh	PPG1	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81FBh	PPG1	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FCh ^{*3}	PPG1	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FDh ^{*4}	PPG1	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FEh ^{*3}	PPG1	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	
0008 81FFh ^{*4}	PPG1	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (18/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 8200h	TMR0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8201h	TMR1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8202h	TMR0	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8203h	TMR1	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8204h	TMR0	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	
0008 8205h	TMR1	Time constant register A	TCORA	8	8 ⁵	2, 3 PCLKB	2 ICLK	
0008 8206h	TMR0	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	
0008 8207h	TMR1	Time constant register B	TCORB	8	8 ⁵	2, 3 PCLKB	2 ICLK	
0008 8208h	TMR0	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 8209h	TMR1	Timer counter	TCNT	8	8 ⁵	2, 3 PCLKB	2 ICLK	
0008 820Ah	TMR0	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK	
0008 820Bh	TMR1	Timer counter control register	TCCR	8	8 ⁵	2, 3 PCLKB	2 ICLK	
0008 8210h	TMR2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8211h	TMR3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8212h	TMR2	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8213h	TMR3	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8214h	TMR2	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	
0008 8215h	TMR3	Time constant register A	TCORA	8	8 ⁵	2, 3 PCLKB	2 ICLK	
0008 8216h	TMR2	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	
0008 8217h	TMR3	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	
0008 8218h	TMR2	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 8219h	TMR3	Timer counter	TCNT	8	8 ⁵	2, 3 PCLKB	2 ICLK	
0008 821Ah	TMR2	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK	
0008 821Bh	TMR3	Timer counter control register	TCCR	8	8 ⁵	2, 3 PCLKB	2 ICLK	
0008 8280h	CRC	CRC control register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK	
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8300h	RIIC0	I ² C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIIC
0008 8301h	RIIC0	I ² C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8302h	RIIC0	I ² C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8303h	RIIC0	I ² C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8304h	RIIC0	I ² C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8305h	RIIC0	I ² C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8306h	RIIC0	I ² C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8307h	RIIC0	I ² C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8308h	RIIC0	I ² C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8309h	RIIC0	I ² C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ah	RIIC0	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ah	RIIC0	Timeout Internal Counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK	
0008 830Bh	RIIC0	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 830Bh	RIIC0	Timeout Internal Counter U	TMOCNTU	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ch	RIIC0	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8310h	RIIC0	I ² C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8311h	RIIC0	I ² C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8312h	RIIC0	I ² C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (22/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 862Ah	MTU4	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	MTU2a
0008 862Ch	MTU3	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 862Dh	MTU4	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8630h	MTU	Timer interrupt skipping set register	TITCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8631h	MTU	Timer interrupt skipping counter	TITCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 8632h	MTU	Timer buffer transfer set register	TBTER	8	8	2, 3 PCLKB	2 ICLK	
0008 8634h	MTU	Timer dead time enable register	TDER	8	8	2, 3 PCLKB	2 ICLK	
0008 8636h	MTU	Timer output level buffer register	TOLBR	8	8	2, 3 PCLKB	2 ICLK	
0008 8638h	MTU3	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK	
0008 8639h	MTU4	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK	
0008 8640h	MTU4	Timer A/D converter start request control register	TADCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8644h	MTU4	Timer A/D converter start request cycle set register A	TADCORA	16	16	2, 3 PCLKB	2 ICLK	
0008 8646h	MTU4	Timer A/D converter start request cycle set register B	TADCORB	16	16	2, 3 PCLKB	2 ICLK	
0008 8648h	MTU4	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16	2, 3 PCLKB	2 ICLK	
0008 864Ah	MTU4	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8660h	MTU	Timer waveform control register	TWCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8680h	MTU	Timer start register	TSTR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8681h	MTU	Timer synchronous register	TSYR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8684h	MTU	Timer read/write enable register	TRWER	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8690h	MTU0	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8691h	MTU1	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8692h	MTU2	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8693h	MTU3	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8694h	MTU4	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8695h	MTU5	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8700h	MTU0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8701h	MTU0	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8702h	MTU0	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8703h	MTU0	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8704h	MTU0	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8705h	MTU0	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8706h	MTU0	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8708h	MTU0	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 870Ah	MTU0	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 870Ch	MTU0	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 870Eh	MTU0	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 8720h	MTU0	Timer general register E	TGRE	16	16	2, 3 PCLKB	2 ICLK	
0008 8722h	MTU0	Timer general register F	TGRF	16	16	2, 3 PCLKB	2 ICLK	
0008 8724h	MTU0	Timer interrupt enable register2	TIER2	8	8	2, 3 PCLKB	2 ICLK	
0008 8726h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK	
0008 8780h	MTU1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8781h	MTU1	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8782h	MTU1	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8784h	MTU1	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8785h	MTU1	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8786h	MTU1	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8788h	MTU1	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 878Ah	MTU1	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8790h	MTU1	Timer input capture control register	TICCR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (27/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 A121h	SCI9	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId
0008 A122h	SCI9	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A123h	SCI9	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A124h	SCI9	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A125h	SCI9	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A126h	SCI9	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A127h	SCI9	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A128h	SCI9	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A129h	SCI9	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A12Ah	SCI9	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A12Bh	SCI9	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A12Ch	SCI9	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A12Dh	SCI9	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A140h	SCI10	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A141h	SCI10	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A142h	SCI10	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A143h	SCI10	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A144h	SCI10	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A145h	SCI10	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A146h	SCI10	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A147h	SCI10	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A148h	SCI10	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A149h	SCI10	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A14Ah	SCI10	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A14Bh	SCI10	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A14Ch	SCI10	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A14Dh	SCI10	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A160h	SCI11	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A161h	SCI11	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A162h	SCI11	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A163h	SCI11	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A164h	SCI11	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A165h	SCI11	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A166h	SCI11	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A167h	SCI11	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A168h	SCI11	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A169h	SCI11	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A16Ah	SCI11	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A16Bh	SCI11	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A16Ch	SCI11	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A16Dh	SCI11	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A800h	IEB	IEBus control register	IECTR	8	8	3 to 4 PCLKB	2, 3 ICLK	IEB
0008 A801h	IEB	IEBus command register	IECMR	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A802h	IEB	IEBus master control register	IEMCR	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A803h	IEB	IEBus master unit address register 1	IEAR1	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A804h	IEB	IEBus master unit address register 2	IEAR2	8	8	3 to 4 PCLKB	2, 3 ICLK	
0008 A805h	IEB	IEBus slave address setting register 1	IESA1	8	8	3 to 4 PCLKB	2, 3 ICLK	

Table 4.1 List of I/O Registers (Address Order) (29/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C000h	PORT0	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C001h	PORT1	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C002h	PORT2	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C003h	PORT3	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C004h	PORT4	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C005h	PORT5	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C006h	PORT6	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C007h	PORT7	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C008h	PORT8	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C009h	PORT9	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Ah	PORTA	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Bh	PORTB	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Ch	PORTC	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Dh	PORTD	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Eh	PORTE	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Fh	PORTF	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C010h	PORTG	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C012h	PORTJ	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C020h	PORT0	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C021h	PORT1	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C022h	PORT2	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C023h	PORT3	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C024h	PORT4	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C025h	PORT5	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C026h	PORT6	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C027h	PORT7	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C028h	PORT8	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C029h	PORT9	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Ah	PORTA	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Bh	PORTB	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Ch	PORTC	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Dh	PORTD	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Eh	PORTE	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Fh	PORTF	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C030h	PORTG	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C032h	PORTJ	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C040h	PORT0	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C041h	PORT1	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C042h	PORT2	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C043h	PORT3	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C044h	PORT4	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C045h	PORT5	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (35/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C344h	ICU	Group 1 interrupt enable register	GEN01	32	32	1 to 2PCLKB	2 ICLK	ICUb
0008 C348h	ICU	Group 2 interrupt enable register	GEN02	32	32	1 to 2PCLKB	2 ICLK	
0008 C34Ch	ICU	Group 3 interrupt enable register	GEN03	32	32	1 to 2PCLKB	2 ICLK	
0008 C350h	ICU	Group 4 interrupt enable register	GEN04	32	32	1 to 2PCLKB	2 ICLK	
0008 C354h	ICU	Group 5 interrupt enable register	GEN05	32	32	1 to 2PCLKB	2 ICLK	
0008 C358h	ICU	Group 6 interrupt enable register	GEN06	32	32	1 to 2PCLKB	2 ICLK	
0008 C370h	ICU	Group 12 interrupt enable register	GEN12	32	32	1 to 2PCLKB	2 ICLK	
0008 C380h	ICU	Group 0 interrupt clear register	GCR00	32	32	1 to 2PCLKB	2 ICLK	
0008 C384h	ICU	Group 1 interrupt clear register	GCR01	32	32	1 to 2PCLKB	2 ICLK	
0008 C388h	ICU	Group 2 interrupt clear register	GCR02	32	32	1 to 2PCLKB	2 ICLK	
0008 C38Ch	ICU	Group 3 interrupt clear register	GCR03	32	32	1 to 2PCLKB	2 ICLK	
0008 C390h	ICU	Group 4 interrupt clear register	GCR04	32	32	1 to 2PCLKB	2 ICLK	
0008 C394h	ICU	Group 5 interrupt clear register	GCR05	32	32	1 to 2PCLKB	2 ICLK	
0008 C398h	ICU	Group 6 interrupt clear register	GCR06	32	32	1 to 2PCLKB	2 ICLK	
0008 C3C0h	ICU	Unit select register	SEL	32	32	1 to 2PCLKB	2 ICLK	
0008 C400h	RTC	64-Hz counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK	RTCa
0008 C402h	RTC	Second counter	RSECCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C404h	RTC	Minute counter	RMINCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C406h	RTC	Hour counter	RHRCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C408h	RTC	Day-of-week counter	RWKCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Ah	RTC	Date counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Ch	RTC	Month counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Eh	RTC	Year counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 C410h	RTC	Second alarm register	RSECAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C412h	RTC	Minute alarm register	RMINAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C414h	RTC	Hour alarm register	RHRAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C416h	RTC	Day-of-week alarm register	RWKAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C418h	RTC	Date alarm register	RDAYAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C41Ah	RTC	Month alarm register	RMONAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C41Ch	RTC	Year alarm register	RYRAR	16	16	2, 3 PCLKB	2 ICLK	
0008 C41Eh	RTC	Year alarm enable register	RYRAREN	8	8	2, 3 PCLKB	2 ICLK	
0008 C422h	RTC	RTC control register 1	RCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C424h	RTC	RTC control register 2	RCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 C426h	RTC	RTC control register 3	RCR3	8	8	2, 3 PCLKB	2 ICLK	
0008 C428h	RTC	RTC control register 4	RCR4	8	8	2, 3 PCLKB	2 ICLK	
0008 C42Ah	RTC	Frequency register H	RFRH	16	16	2, 3 PCLKB	2 ICLK	
0008 C42Ch	RTC	Frequency register L	RFRL	16	16	2, 3 PCLKB	2 ICLK	
0008 C42Eh	RTC	Time error adjustment register	RADJ	8	8	2, 3 PCLKB	2 ICLK	
0008 C440h	RTC	Time capture control register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK	
0008 C442h	RTC	Time capture control register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C444h	RTC	Time capture control register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 C452h	RTC	Second capture register 0	RSECCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C454h	RTC	Minute capture register 0	RMINCP0	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (43/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 00D0h	USB0	Device address 0 configuration register	DEVADD0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 00D2h	USB0	Device address 1 configuration register	DEVADD1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	USBa
000A 00D4h	USB0	Device address 2 configuration register	DEVADD2	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 00D6h	USB0	Device address 3 configuration register	DEVADD3	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 00D8h	USB0	Device address 4 configuration register	DEVADD4	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 00DAh	USB0	Device address 5 configuration register	DEVADD5	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0200h	USB1	System configuration control register	SYSCFG	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0204h	USB1	System configuration status register 0	SYSSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0208h	USB1	Device state control register 0	DVSTCTR0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0214h	USB1	CFIFO port register	CFIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 0218h	USB1	D0FIFO port register	D0FIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 021Ch	USB1	D1FIFO port register	D1FIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 0220h	USB1	CFIFO port select register	CFIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0222h	USB1	CFIFO port control register	CFIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0228h	USB1	D0FIFO port select register	D0FIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	USBa
000A 022Ah	USB1	D0FIFO port control register	D0FIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 022Ch	USB1	D1FIFO port select register	D1FIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 022Eh	USB1	D1FIFO port control register	D1FIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	

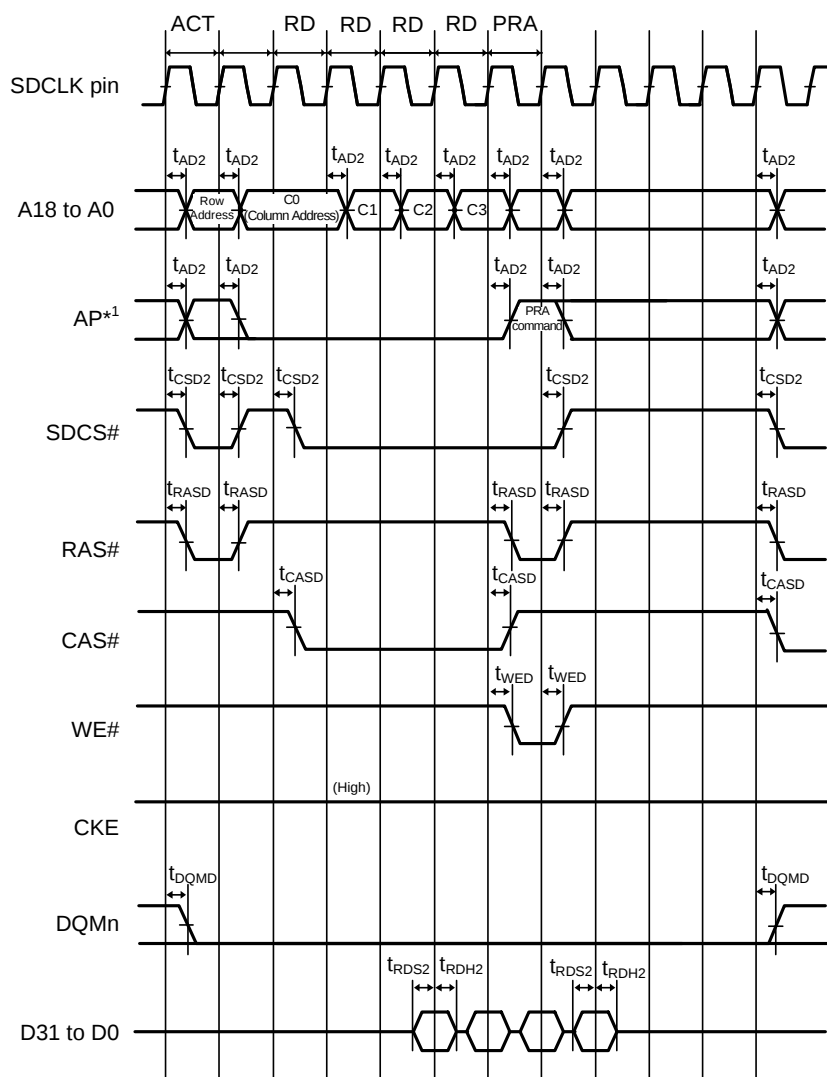
Table 4.1 List of I/O Registers (Address Order) (44/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK $\geq$ PCLK	ICLK<PCLK	
000A 0230h	USB1	Interrupt enable register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0236h	USB1	BRDY interrupt enable register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0238h	USB1	NRDY interrupt enable register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 023Ah	USB1	BEMP interrupt enable register	BEMPENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 023Ch	USB1	SOF output configuration register	SOFCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0240h	USB1	Interrupt status register 0	INTSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0246h	USB1	BRDY interrupt status register	BRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0248h	USB1	NRDY interrupt status register	NRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	USBa
000A 024Ah	USB1	BEMP interrupt status register	BEMPSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 024Ch	USB1	Frame number register	FRMNUM	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	

Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions		
Supply current*1	High-speed operating mode	Max.*2		I _{CC} *3	—	—	100	mA	ICLK = 100 MHz PCLKA = 100MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 100MHz		
		Normal*4	Peripheral function: clock signal supplied*4		—	52	—				
			Peripheral function: clock signal stopped*4		—	40	—				
		Sleep mode			—	25	65				
		All-module-clock-stop mode (reference value)			—	20	38				
		Increased by BGO operation*5			—	15	—				
	Low-speed operating mode 1*6				—	4	—			ICLK = 1 MHz	
	Low-speed operating mode 2				—	1	—				ICLK = 32.768 kHz
	Software standby mode				—	0.2	6				
	Deep software standby mode	Power supplied to RAM and USB resume detecting unit	Power not supplied to RAM and USB resume detecting unit		Power-on reset circuit and low-power consumption function disabled	—	22	200	μA		
					Power-on reset circuit and low-power	—	21	60			
						—	6.2	28			
		Increase when the RTC is operating	When a crystal oscillator for low clock loads is in use		—	1.0	—				
			When a crystal oscillator for standard clock loads is in use		—	3.0	—				
		RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)	When a crystal oscillator for low clock loads is in use		—	0.9	—	V _{BATT} = 2.0 V, VCC = 0V			
					—	1.6	—	V _{BATT} = 3.3 V, VCC = 0V			
			When a crystal oscillator for standard clock loads is in use		—	1.7	—	V _{BATT} = 2.0 V (for products with 100 pins or more), VBATT = 2.3 V (for the 64-pin product), VCC = 0V			
					—	3.3	—	V _{BATT} = 3.3 V, VCC = 0V			
Analog power supply current*7	During 12-bit A/D conversion (including temperature sensor)			I _{AVCC0}	—	2.3	3.2	mA			
	During 10-bit A/D conversion			I _{VREFH} *9	—	1.0	1.65				
	During D/A conversion (per unit)				—	0.7	1.0				
	Waiting for A/D, D/A conversion (all units)*10			—	—	25	35		μA		
	A/D, D/A converter in standby mode (all units)*10				—	0.1	4.0		μA		
Reference power supply current	During 12-bit A/D conversion			I _{VREFH0}	—	0.6	0.7	mA			
	Waiting for 12-bit A/D conversion (per unit)				—	0.5	0.6				
	12-bit A/D converter in standby mode (per unit)				—	0.1	2.0		μA		



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.26 SDRAM Space Multiple Read Bus Timing

Table 5.25 Timing of On-Chip Peripheral Modules (7)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

ICLK = 12.5 to 100 MHz, T_a = T_{opr}

High drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
ETHERC(RMII)	REF50CK cycle time	T _{ck}	20	—	ns	Figure 5.48 to Figure 5.51
	REF50CK frequency Typ. 50 MHz	—	—	50 + 100ppm	MHz	
	REF50CK duty	—	35	65	%	
	REF50CK rise/fall time	T _{ckr/ckf}	0.5	3.5	ns	
	RMII_XXXX*1 output delay time	T _{co}	2.5	15.0	ns	
	RMII_XXXX*2 setup time	T _{su}	3	—	ns	
	RMII_XXXX*2 hold time	T _{hd}	1	—	ns	
	RMII_XXXX*1, *2 rise/fall time	Tr/Tf	0.5	6	ns	
	ET_WOL output delay time	t _{WOLd}	1	23.5	ns	Figure 5.52
ETHERC(MII)	ET_TX_CLK cycle time	t _{Tcyc}	40	—	ns	—
	ET_TX_EN output delay time	t _{TEND}	1	20	ns	Figure 5.53
	ET_ETXD0 to ET_ETXD3 output delay time	t _{MTDd}	1	20	ns	
	ET_CRs setup time	t _{CRSs}	10	—	ns	
	ET_CRs hold time	t _{CRSh}	10	—	ns	
	ET_COL setup time	t _{COLs}	10	—	ns	Figure 5.54
	ET_COL hold time	t _{COLh}	10	—	ns	
	ET_RX_CLK cycle time	t _{TRcyc}	40	—	ns	—
	ET_RX_DV setup time	t _{RDVs}	10	—	ns	Figure 5.55
	ET_RX_DV hold time	t _{RDVh}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 setup time	t _{MRDs}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 hold time	t _{MRDh}	10	—	ns	
	ET_RX_ER setup time	t _{RERs}	10	—	ns	Figure 5.56
	ET_RX_ER hold time	t _{RESh}	10	—	ns	
	ET_WOL output delay time	t _{WOLd}	1	23.5	ns	Figure 5.57

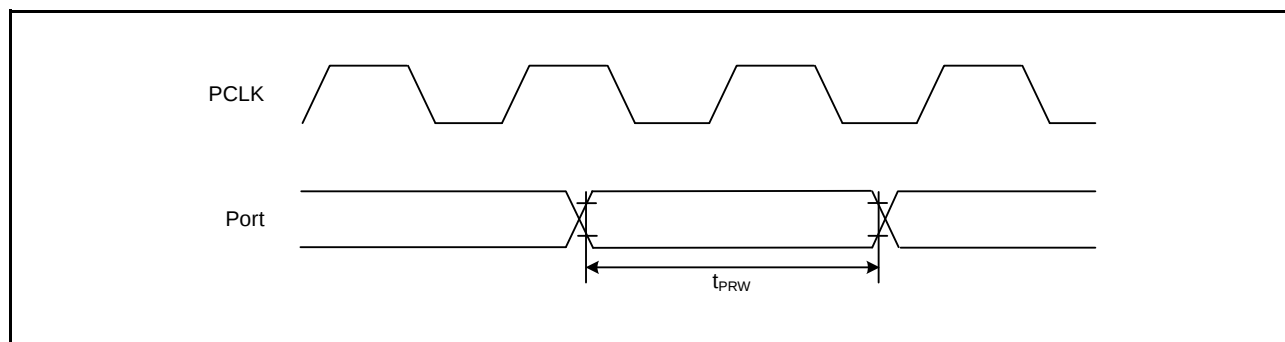
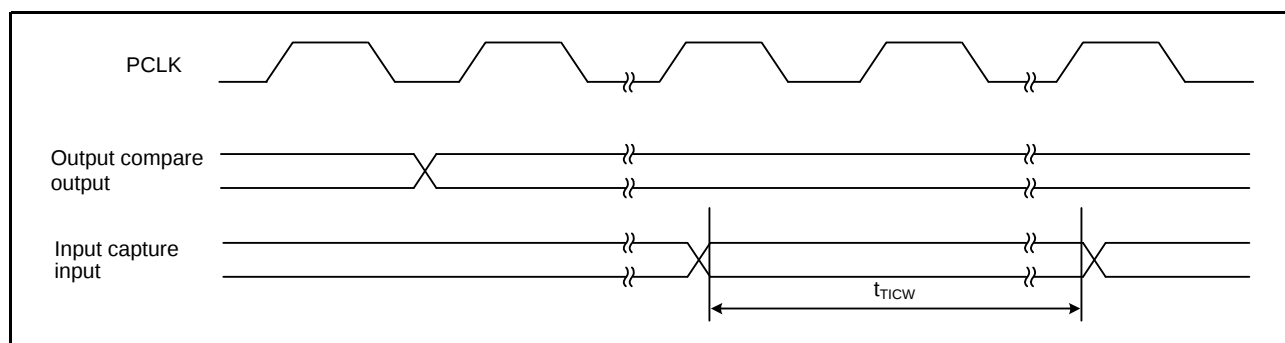
Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0.

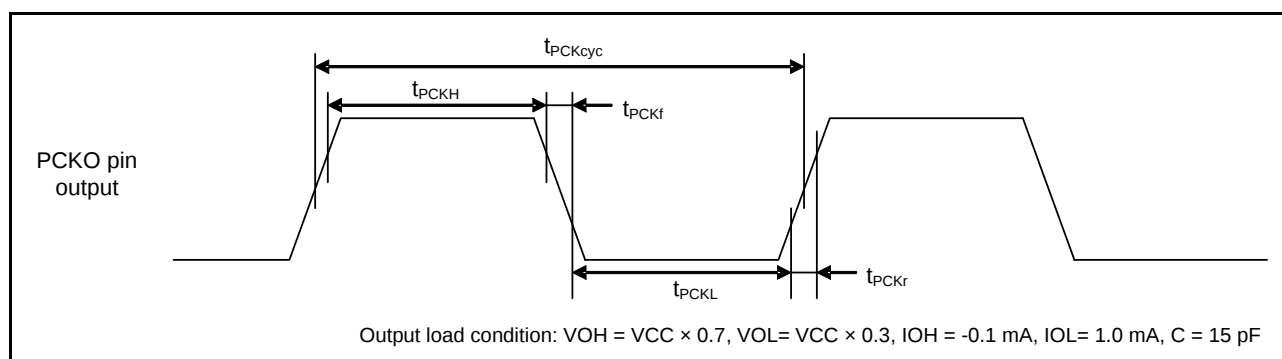
Note 2. RMII_CRs_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

Table 5.26 Timing of On-Chip Peripheral Modules (8)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V, PIXCLK = 27MHz, T_a = T_{opr}

	Item	Symbol	min	typ	max	Unit	Test Conditions
PDC	VSYN/HSYN input setup time	t _{SYNCSSETUP}	10	—	—	ns	Figure 5.58
	VSYN/HSYN input hold time	t _{SYNCHOLD}	5	—	—	ns	
	PIXD input setup time	t _{DATASETUP}	10	—	—	ns	
	PIXD input hold time	t _{DATAHOLD}	5	—	—	ns	
	PIXCLK input cycle time	t _{PIXcyc}	37	—	1000	ns	Figure 5.59
	PIXCLK input pulse width high level	t _{PIXH}	10	—	—	ns	
	PIXCLK input pulse width low level	t _{PIXL}	10	—	—	ns	
	PCKO pin output cycle time	t _{PCKcyc}	40	—	1000	ns	Figure 5.60
	PCKO pin output high level pulse width	t _{PCKH}	13	—	—	ns	
	PCKO pin output low level pulse width	t _{PCKL}	13	—	—	ns	
	PCKO pin output rising time	t _{PCKr}	—	—	5	ns	
	PCKO pin output falling time	t _{PCKf}	—	—	5	ns	

**Figure 5.34 I/O Port Input Timing****Figure 5.35 MTU Input/Output Timing**

**Figure 5.60 PDC Output Clock Characteristic**

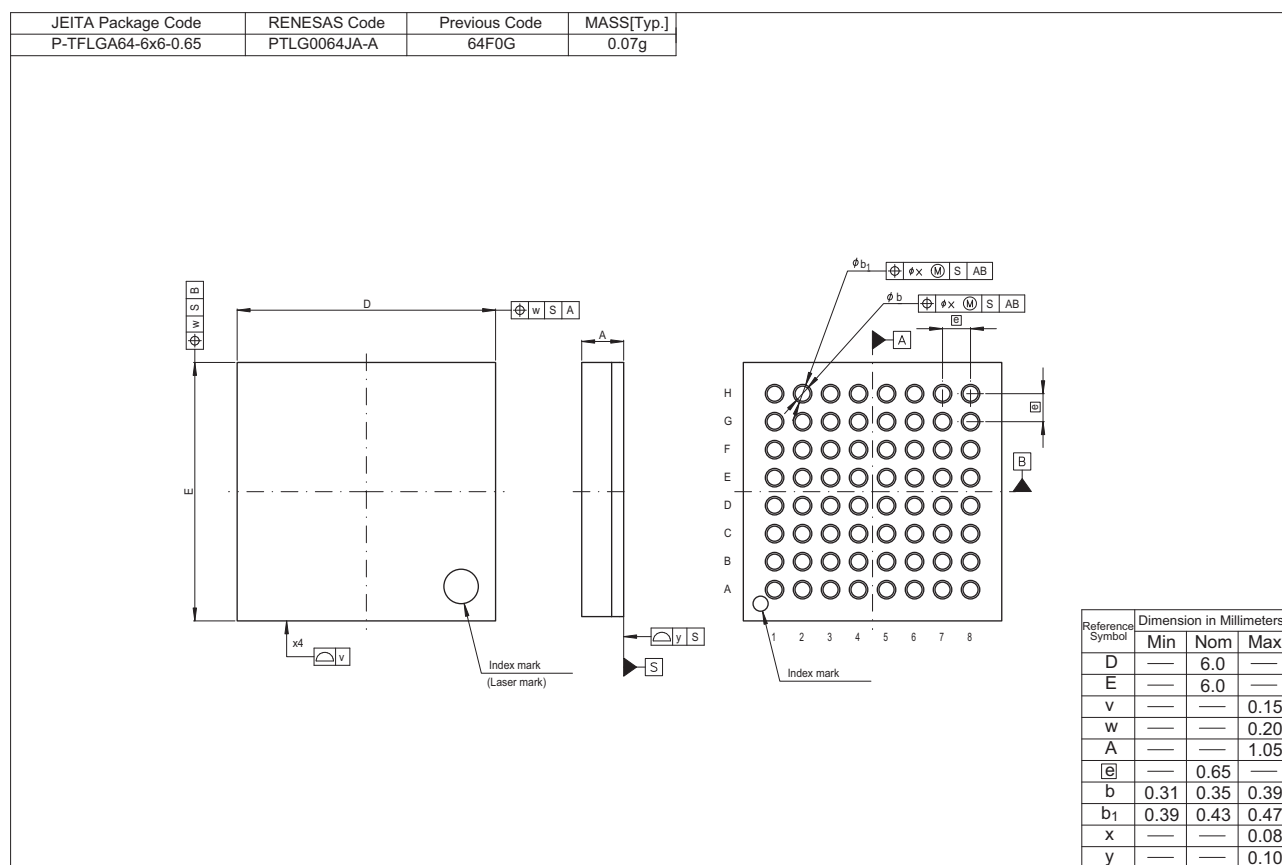


Figure H 64-pin TFLGA (PTLG0064JA-A)

REVISION HISTORY	RX63N Group, RX631 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.50	May 13, 2011	—	First Edition issued
0.90	Dec 27, 2011	All	— Package added (177-pin TFLGA, 176-pin LFBGA, 145-pin TFLGA), module name changed — Interrupt Controller (ICUb) module name changed 1. Overview 2 to 6 Table 1.1 Outline of Specifications, Reset, Realtime clock, Temperature sensor, Power supply voltage, changed 8 to 10 Table 1.3 List of Products, changed 10 Figure 1.1 How to Read the Product Part No., changed 12 to 17 Table 1.4 Pin Functions, BSCANP pin added 18 Figure 1.3 Pin Assignment (176-Pin TFLGA), added 19 Figure 1.4 Pin Assignment (176-Pin LFBGA), added 20 Figure 1.5 Pin Assignment (176-Pin LQFP), pin 18 changed 21 Figure 1.6 Pin Assignment (144-Pin TFLGA), added 22 Figure 1.7 Pin Assignment (144-Pin LQFP), pin 16 changed 23 Figure 1.8 Pin Assignment (100-Pin LQFP), pin 7 changed 24 to 28 Table 1.5 List of Pins and Pin Functions (177-pin TFLGA, 176-pin LFBGA), added 34 to 38 Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA), added 4. I/O Registers 56 to 99 Table 5.1 List of I/O Registers, changed Appendix 2. Package Dimensions 100 Figure A. 177-pin TFLGA (PTLG0177KA-A), added 101 Figure B. 176-pin LFBGA (PLBG0176GA-A), added 103 Figure D. 145-pin TFLGA (PTLG0145KA-A), added 105 Figure F. 100-pin TFLGA (PTLG0100KA-A), added
1.00	Jun 06, 2012	1. Overview	2 to 6 Table 1.1 Outline of Specifications: CPU, ROM, RAM, E2 DataFlash, clock generation circuit, temperature sensor, power supply voltage, changed. Low power consumption, deleted 8 to 10 Table 1.3 List of Products, changed 11 Figure 1.2 Block Diagram, changed 12 Table 1.4 Pin Functions, description of VCC, changed 24 to 28 Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA): SDRAMC, added to table header; BCLK in pin number line M8, moved to Power Supply Clock System Control column 29 to 33 Table 1.6 List of Pin and Pin Functions (176-Pin LQFP): SDRAMC, added to table header; BCLK in pin number line 68, moved to Power Supply Clock System Control column 34 to 38 Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA): SDRAMC, added to table header; MOSIB, added to pin number line D13; T_ERXD1 in pin number line H12, changed to ET_ERXD1; PO8, added to pin number line J4; BCLK in pin number line K6, moved to Power Supply Clock System Control column 39 to 43 Table 1.8 List of Pins and Pin Functions (144-Pin LQFP): SDRAMC, added to table header; PO8, added to pin number line 29; BCLK in pin number line 53, moved to Power Supply Clock System Control column; T_ERXD1 in pin number 87, changed to ET_ERXD1; MOSIB, added to pin number line 102 44 to 47 Table 1.9 List of Pins and Pin Functions (100-Pin LQFP): BCLK in pin number line 41, moved to Power Supply Clock System Control column 4. I/O Registers 57, 58 Table 4.1, MPU registers, added 5. Electrical Characteristics 105 to 163 Added