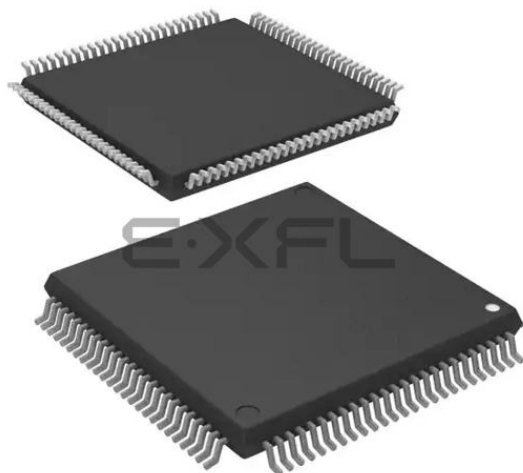




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Details

Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631dcdp-v0

Table 1.1 Outline of Specifications (5/6)

Classification	Module/Function	Description
Communication function	Ethernet controller (ETHERC)	- Input and output of Ethernet/IEEE 802.3 frames - Transfer at 10 or 100 Mbps - Full- and half-duplex modes - MII (Media Independent Interface) or RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u - Detection of Magic Packets^{TM*1} or output of a "wake-on-LAN" signal (WOL) - Compliance with flow control as defined in IEEE 802.3x standards Note 1. Magic PacketTM is a registered trademark of Advanced Micro Devices, Inc.
	DMA controller for Ethernet controller (EDMAC)	- Alleviation of CPU loads by the descriptor control method - Transmission FIFO: 2 Kbytes; Reception FIFO: 2 Kbytes
	USB 2.0 host/function module (USBa)	- Includes a UDC (USB Device Controller) and transceiver for USB 2.0 - Host/function module: one port, function module: one port - Compliance with the USB 2.0 specification - Transfer rate: Full speed (12 Mbps) - Self-power mode and bus-power mode are selectable - OTG (On the Go) operation is possible - Incorporates 2 Kbytes of RAM as a transfer buffer
	Serial communications interfaces (SCIC, SCId)	13 channels (SCIC: 12 channels + SCId: 1 channel) - SCIC - Serial communications modes: Asynchronous, clock synchronous, and smart-card interface - Multi-processor function - On-chip baud rate generator allows selection of the desired bit rate - Choice of LSB-first or MSB-first transfer - Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 - Simple I²C - Simple SPI - SCId (The following functions are added to SCIC) - Supports the serial communications protocol, which contains the start frame and information frame - Supports the LIN format
	I ² C bus interfaces (RIIC)	4 channels (one of them is FM+) - Communication formats - I²C bus format/SMBus format - Supports the multi-master - Max. transfer rate: 1 Mbps (channel 0)
	IEBus (IEB)	1 channel - Supports protocol control for the IEBus - Half-duplex asynchronous transfer - Multi-master operation - Broadcast communications function - Two selectable modes, differentiated by transfer rate
	CAN module (CAN)	3 channels - Compliance with the ISO11898-1 specification (standard frame and extended frame) 32 mailboxes each
	Serial peripheral interfaces (SPI)	3 channels - RSPI transfer facility - Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) - Capable of handling serial transfer as a master or slave - Data formats - Switching between MSB first and LSB first - The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception - Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) - Buffered structure - Double buffers for both transmission and reception

Table 1.4 Pin Functions (5/6)

Classifications	Pin Name	I/O	Description
Ethernet controller	ET_MDIO	I/O	Inputs or outputs bidirectional signals for exchange of management information between the RX63N Group and the PHY-LSI.
Parallel data capture unit (PDC)	PIXCLK	Input	Parallel data transfer clock
	VSYNC	Input	Vertical synchronization signal
	HSYNC	Input	Horizontal synchronization signal
	PIXD7 to PIXD0	Input	8-bit data
	PCKO	Output	Outputs parallel data transfer clock signal
USB power pins	VCC_USB	Input	Power supply pin. When the USB is not to be used, connect it to the VCC pin.
	VSS_USB	Input	Ground pin. When the USB is not to be used, connect it to the VSS pin.
USB 2.0 host/function module	USB0_DP, USB1_DP	I/O	Inputs or outputs USB transceiver D+ data.
	USB0_DM, USB1_DM	I/O	Inputs or outputs USB transceiver D- data.
	USB0_VBUS, USB1_VBUS	Input	Input pins for detection of connection and disconnection of the USB cable.
	USB0_EXICEN	Output	Output pin for control the low power of the OTG chip.
	USB0_VBUSEN	Output	Supply enable pin of VBUS (5 V) for the OTG chip.
	USB0_OVRCURA, USB0_OVRCURB,	Input	Input pin for detection of external over current.
	USB0_ID	Input	ID input pin of mini-AB connector at the OTG operation.
	USB0_DPUPE, USB1_DPUPE	Output	Pull-up control pins of the D+ signal at the function operation.
	USB0_DPRPD	Output	Pull-down control pins of the D+ signal at the host operation.
	USB0_DRPD	Output	Pull-down control pins of the D- signal at the host operation.
CAN module	CRX0 to CRX2	Input	Input pin.
	CTX0 to CTX2	Output	Output pin.
Serial peripheral interface	RSPCKA, RSPCKB, RSPCKC	I/O	Clock input/output pin.
	MOSIA, MOSIB, MOSIC	I/O	Inputs or outputs data output from the master.
	MISOA, MISOB, MISOC	I/O	Inputs or outputs data output from the slave.
	SSLA0, SSLB0, SSLC0	I/O	Input or output pins slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3, SSLC1 to SSLC3	Output	Output pins slave selection
IEBus controller	IERXD	Input	Input pin for data reception.
	IETXD	Output	Output pin for data transmission.
Realtime clock	RTCOUT	Output	Output pin for 1-Hz clock.
	RTCIC0 to RTCIC2	Input	Time capture event input pin
12-bit A/D converter	AN000 to AN020	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pins for the external trigger signals that start the A/D conversion.
10-bit A/D converter	AN0 to AN7	Input	Input pins for the analog signals to be processed by the A/D converter.
	ANEX0	Output	Extended analog output pin
	ANEX1	Input	Extended analog input pin
	ADTRG#	Input	Input pins for the external trigger signals that start the A/D conversion.
D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter.

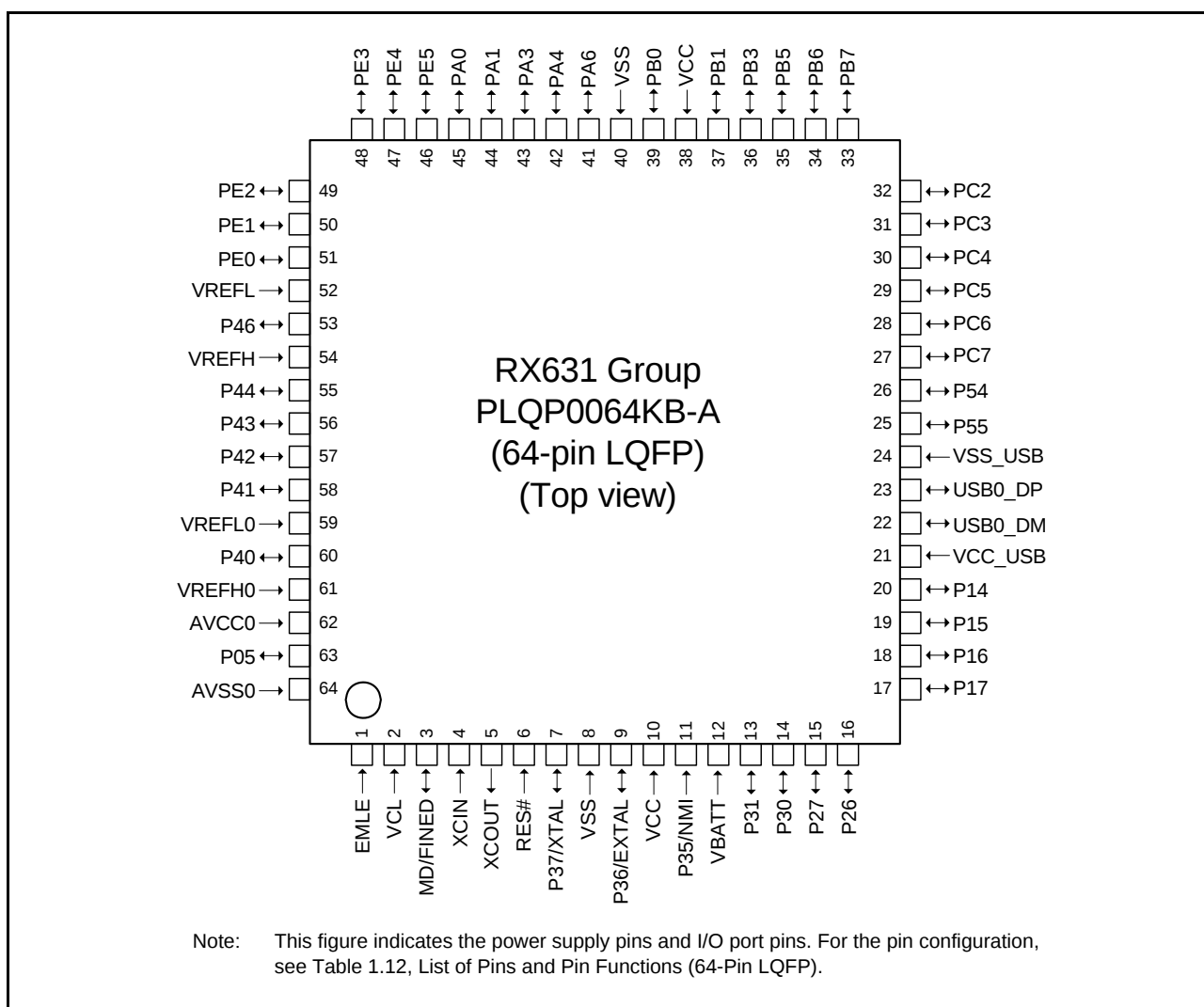


Figure 1.11 Pin Assignment (64-Pin LQFP)

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (4/5)

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
100		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	ET_ERXD0/RMII_RXD0/ TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6	IRQ4-DS	
101		P72	CS2#		ET_MDC		
102		P71	CS1#		ET_MDIO		
103	VCC						
104		PB0	A8	MTIC5W/TIOCA3/PO24	ET_ERXD1/RMII_RXD1/ RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA	IRQ12	
105	VSS						
106		PA7	A7	TIOCB2/PO23	ET_WOL/MISOA		
107		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	ET_EXOUT/CTS5#/ RTS5#/SS5#/MOSIA		
108		PA5	A5	TIOCB1/PO21	ET_LINKSTA/RSPCKA		
109		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	ET_MDC/TXD5/SMOSI5/ SSDA5/SSLA0	IRQ5-DS	
110		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	ET_MDIO/RXD5/SMISO5/ SSCL5	IRQ6-DS	
111	TRDATA3	PG7	D31				
112		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
113	TRDATA2	PG6	D30				
114		PA1	A1/DQM3	MTIOC0B/MTCLKC/ TIOCB0/PO17	ET_WOL/SCK5/SSLA2	IRQ11	
115	VCC						
116	TRCLK	PG5	D29				
117	VSS						
118		PA0	A0/BC0#/DQM2	MTIOC4A/TIOCA0/PO16	ET_TX_EN/ RMII_TXD_EN/SSLA1		
119	TRSYNC	PG4	D28				
120		P67	CS7#/DQM1		CRX2*2	IRQ15	
121	TRDATA1	PG3	D27				
122		P66	CS6#/DQM0		CTX2*2		
123	TRDATA0	PG2	D26				
124		P65	CS5#/CKE				
125		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
126		PE6	D14[A14/D14]	TIOCA11	MOSIB	IRQ6	AN4
127	VCC						
128	SDCLK	P70					
129	VSS						
130		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	ET_RX_CLK/REF50CK/ RSPCKB	IRQ5	AN3
131		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	ET_ERXD2/SSLB0		AN2
132		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/PO26/ POE8#	ET_ERXD3/CTS12#/ RTS12#/SS12#/MISOB		AN1
133		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/PO23	RXD12/SMISO12/ SSCL12/RXD12/SSLB3/ MOSIB	IRQ7-DS	AN0
134		PE1	D9[A9/D9]	MTIOC4C/TIOC0D/PO18	TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/SSLB2/RSPCKB		ANEX1
135		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (3/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCId, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
H12		PB0	A8	MTIOC5W/TIOCA3/PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA/T_ERXD1/ RMII_RXD1	IRQ12	
H13		PA7	A7	TIOCB2/PO23	MISOA/ET_WOL		
J1	TRST#	P34		MTIOC0A/TMC13/PO12/ POE2#	SCK6/SCK0/ USB0_DPRPD	IRQ4	
J2		P33		MTIOC0D/TIOCD0/ TMR13/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0/PCKO	IRQ3-DS	
J3		P32		MTIOC0C/TIOCC0/ TMO3/PO10/RTICOUT/ RTIC12	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC	IRQ2-DS	
J4	TDI	P30		MTIOC4B/TMR13/PO8/ RTIC10/POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
J10		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	SCK4/SCK6/ET_RX_ER/ RMII_RX_ER		
J11		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/SS9#/ ET_TX_EN/RMII_TXD_EN		
J12		PB2	A10	TIOCC3/TCLKC/PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET_RX_CLK/REF50CK		
J13		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6/ ET_ERXD0/RMII_RXD0	IRQ4-DS	
K1	TCK/FINEC	P27	CS7#	MTIOC2B/TMC13/PO7	SCK1/RSPCKB		
K2	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
K3	TMS	P31		MTIOC4D/TMC12/PO9/ RTIC11	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
K4		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/PIXD0	IRQ5	
K5	TRDATA2	P54	ALE/EDACK0	MTIOC4B/TMC11	CTS2#/RTS2#/SS2#/ CTX1/ET_LINKSTA		
K6		P53*1	BCLK				
K7		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
K8	VCC						
K9	TRDATA0	P80	EDREQ0	MTIOC3B/PO26	SCK10/ET_TX_EN/ RMII_TXD_EN		
K10		P76	CS6#	PO22	RXD11/SMISO11/SSCL11/ ET_RX_CLK/REF50CK		
K11		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/SMOSI9/SSDA9/ ET_CRS/RMII_CRS_DV		
K12		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/SMISO9/SSCL9/ ET_ETXD1/RMII_TXD1		
K13		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1#	SCK9/ET_ETXD0/ RMII_TXD0		
L1		P25	CS5#/EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC		ADTRG0#
L2		P23	EDACK0	MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7		

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (3/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
F7		PB2	A10	TIOCC3/ TCLKC/PO26	CTS6#/RTS6#/ SS6#/ET_RX_CLK/ REF50CK		
F8		PB0	A8	MTIC5W/ TIOCA3/PO24	RXD6/SMISO6/ SSCL6/RSPCKA/ ET_ERXD1/ RMII_RXD1	IRQ12	
F9		PA7	A7	TIOCB2/PO23	MISOA/ET_WOL		
F10	VSS						
G1		P33		MTIOC0D/ TIOC0D/ TMRI3/PO11/ POE3#	RXD6/RXD0/ SMISO6/SMISO0/ SSCL6/SSCL0/ CRX0*1	IRQ3-DS	
G2	TMS	P31		MTIOC4D/ TMC12/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0/ USB0_DPUPE	IRQ1-DS	
G3	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/MISOB/ USB0_DRPD	IRQ0-DS	
G4	TCK/FINEC	P27	CS7#	MTIOC2B/ TMC13/PO7	SCK1/RSPCKB		
G5	BCLK	P53*2					
G6		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3		
G7		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE1#	SCK9/ET_ETXD0/ RMII_TXD0		
G8		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/ SS9#/ET_TX_EN/ RMII_TXD_EN		
G9		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMC10/PO25	TXD6/SMOSI6/ SSDA6/ET_ERXD0/ RMII_RXD0	IRQ4-DS	
G10	VCC						
H1	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ MOSIB		
H2		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/ USB0_DPRPD		ADTRG0#
H3		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT	TXD1/RXD3/ SMOSI1/SMISO3/ SSDA1/SSCL3/ MOSIA/SCL2-DS/ IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#

Table 1.11 List of Pins and Pin Functions (64-Pin TFLGA) (1/2)

Pin No. 64-pin TFLGA	Power Supply Clock System Control	I/O Port	Timers (MTU2a, TPUa, TMR, PPG, RTCa, POE2a)	Communications (SClC, SClD, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
A1		P05			IRQ13	DA1
A2	AVCC0					
A3	VREFH0					
A4	VREFL0					
A5	VREFH					
A6	VREFL					
A7		PE2	MTIOC4A/PO23	RXD12/SMISO12/SSCL12/ RXDX12/SSLB3/MOSIB	IRQ7-DS	AN010
A8		PE3	MTIOC4B/PO26/POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN011
B1	VCL					
B2	AVSS0					
B3		P40			IRQ8-DS	AN000
B4		P42			IRQ10-DS	AN002
B5		P44			IRQ12-DS	AN004
B6		P46			IRQ14-DS	AN006
B7		PE1	MTIOC4C/PO18	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB		AN009
B8		PE4	MTIOC4D/MTIOC1A/PO28	SSLB0		AN012
C1	XCIN					
C2	MD/FINED					
C3	EMLE					
C4		P41			IRQ9-DS	AN001
C5		P43			IRQ11-DS	AN003
C6		PE0		SCK12/SSLB1		AN008
C7		PE5	MTIOC4C/MTIOC2B	RSPCKB	IRQ5	AN013
C8		PA0	MTIOC4A/TIOCA0/PO16	SSLA1		
D1	XCOUT					
D2	RES#					
D3	TCK FINEC	P27	MTIOC2B/TMCI3	SCK1/RSPCKB		
D4		P14	MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2	CTS1#/RTS1#/SS1#/CTX1/ USB0_DPUPE/ USB0_OVRCURA	IRQ4	
D5		PA6	MTIC5V/MTCLKB/TIOCA2/ TMCI3/PO22/POE2#	CTS5#/RTS5#/SS5#/ MOSIA		
D6		PA4	MTIC5U/MTCLKA/TIOCA1/ TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS	
D7		PA1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2/SCL2	IRQ11	
D8		PA3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/SSCL5/ SDA2	IRQ6-DS	
E1	VSS					
E2	VBATT					
E3	TDI	P30	MTIOC4B/TMRI3/POE8#/ RTIC0	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively. Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Table 4.1 List of I/O Registers (Address Order) (3/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 2818h	EXDMAC0	EXDMA offset register	EDMOFR	32	32	1, 2 BCLK		EXDMACa
0008 281Ch	EXDMAC0	EXDMA transfer enable register	EDMCNT	8	8	1, 2 BCLK		
0008 281Dh	EXDMAC0	EXDMA software start register	EDMREQ	8	8	1, 2 BCLK		
0008 281Eh	EXDMAC0	EXDMA status register	EDMSTS	8	8	1, 2 BCLK		
0008 2820h	EXDMAC0	EXDMA external request sense mode register	EDMRMD	8	8	1, 2 BCLK		
0008 2821h	EXDMAC0	EXDMA external request flag register	EDMERF	8	8	1, 2 BCLK		
0008 2822h	EXDMAC0	EXDMA peripheral request flag register	EDMPRF	8	8	1, 2 BCLK		
0008 2840h	EXDMAC1	EXDMA source address register	EDMSAR	32	32	1, 2 BCLK		
0008 2844h	EXDMAC1	EXDMA destination address register	EDMDAR	32	32	1, 2 BCLK		
0008 2848h	EXDMAC1	EXDMA transfer count register	EDMCRA	32	32	1, 2 BCLK		
0008 284Ch	EXDMAC1	EXDMA block transfer count register	EDMCRB	16	16	1, 2 BCLK		
0008 2850h	EXDMAC1	EXDMA transfer mode register	EDMTMD	16	16	1, 2 BCLK		
0008 2852h	EXDMAC1	EXDMA output setting register	EDMOMD	8	8	1, 2 BCLK		
0008 2853h	EXDMAC1	EXDMA interrupt setting register	EDMINT	8	8	1, 2 BCLK		
0008 2854h	EXDMAC1	EXDMA address mode register	EDMAMD	32	32	1, 2 BCLK		
0008 285Ch	EXDMAC1	EXDMA transfer enable register	EDMCNT	8	8	1, 2 BCLK		
0008 285Dh	EXDMAC1	EXDMA software start register	EDMREQ	8	8	1, 2 BCLK		
0008 285Eh	EXDMAC1	EXDMA status register	EDMSTS	8	8	1, 2 BCLK		
0008 2860h	EXDMAC1	EXDMA external request sense mode register	EDMRMD	8	8	1, 2 BCLK		
0008 2861h	EXDMAC1	EXDMA external request flag register	EDMERF	8	8	1, 2 BCLK		
0008 2862h	EXDMAC1	EXDMA peripheral request flag register	EDMPRF	8	8	1, 2 BCLK		
0008 2A00h	EXDMAC	EXDMA module start register	EDMAST	8	8	1, 2 BCLK		
0008 2BE0h	EXDMAC	Cluster buffer register 0	CLSBR0	32	32	1, 2 BCLK		
0008 2BE4h	EXDMAC	Cluster buffer register 1	CLSBR1	32	32	1, 2 BCLK		
0008 2BE8h	EXDMAC	Cluster buffer register 2	CLSBR2	32	32	1, 2 BCLK		
0008 2BECh	EXDMAC	Cluster buffer register 3	CLSBR3	32	32	1, 2 BCLK		
0008 2BF0h	EXDMAC	Cluster buffer register 4	CLSBR4	32	32	1, 2 BCLK		
0008 2BF4h	EXDMAC	Cluster buffer register 5	CLSBR5	32	32	1, 2 BCLK		
0008 2BF8h	EXDMAC	Cluster buffer register 6	CLSBR6	32	32	1, 2 BCLK		
0008 2BFCh	EXDMAC	Cluster buffer register 7	CLSBR7	32	32	1, 2 BCLK		
0008 3002h	BSC	CS0 mode register	CS0MOD	16	16	1, 2 BCLK		Buses
0008 3004h	BSC	CS0 wait control register 1	CS0WCR1	32	32	1, 2 BCLK		
0008 3008h	BSC	CS0 wait control register 2	CS0WCR2	32	32	1, 2 BCLK		
0008 3012h	BSC	CS1 mode register	CS1MOD	16	16	1, 2 BCLK		
0008 3014h	BSC	CS1 wait control register 1	CS1WCR1	32	32	1, 2 BCLK		
0008 3018h	BSC	CS1 wait control register 2	CS1WCR2	32	32	1, 2 BCLK		
0008 3022h	BSC	CS2 mode register	CS2MOD	16	16	1, 2 BCLK		
0008 3024h	BSC	CS2 wait control register 1	CS2WCR1	32	32	1, 2 BCLK		
0008 3028h	BSC	CS2 wait control register 2	CS2WCR2	32	32	1, 2 BCLK		
0008 3032h	BSC	CS3 mode register	CS3MOD	16	16	1, 2 BCLK		
0008 3034h	BSC	CS3 wait control register 1	CS3WCR1	32	32	1, 2 BCLK		
0008 3038h	BSC	CS3 wait control register 2	CS3WCR2	32	32	1, 2 BCLK		
0008 3042h	BSC	CS4 mode register	CS4MOD	16	16	1, 2 BCLK		
0008 3044h	BSC	CS4 wait control register 1	CS4WCR1	32	32	1, 2 BCLK		
0008 3048h	BSC	CS4 wait control register 2	CS4WCR2	32	32	1, 2 BCLK		
0008 3052h	BSC	CS5 mode register	CS5MOD	16	16	1, 2 BCLK		
0008 3054h	BSC	CS5 wait control register 1	CS5WCR1	32	32	1, 2 BCLK		
0008 3058h	BSC	CS5 wait control register 2	CS5WCR2	32	32	1, 2 BCLK		
0008 3062h	BSC	CS6 mode register	CS6MOD	16	16	1, 2 BCLK		
0008 3064h	BSC	CS6 wait control register 1	CS6WCR1	32	32	1, 2 BCLK		
0008 3068h	BSC	CS6 wait control register 2	CS6WCR2	32	32	1, 2 BCLK		

Table 4.1 List of I/O Registers (Address Order) (8/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 70CBh	ICU	Interrupt request register 203	IR203	8	8	2	ICLK	ICUb
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2	ICLK	
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2	ICLK	
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2	ICLK	
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2	ICLK	
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2	ICLK	
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2	ICLK	
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2	ICLK	
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2	ICLK	
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2	ICLK	
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2	ICLK	
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2	ICLK	
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2	ICLK	
0008 70E2h	ICU	Interrupt request register 226	IR226	8	8	2	ICLK	
0008 70E3h	ICU	Interrupt request register 227	IR227	8	8	2	ICLK	
0008 70E4h	ICU	Interrupt request register 228	IR228	8	8	2	ICLK	
0008 70E5h	ICU	Interrupt request register 229	IR229	8	8	2	ICLK	
0008 70E6h	ICU	Interrupt request register 230	IR230	8	8	2	ICLK	
0008 70E7h	ICU	Interrupt request register 231	IR231	8	8	2	ICLK	
0008 70E8h	ICU	Interrupt request register 232	IR232	8	8	2	ICLK	
0008 70E9h	ICU	Interrupt request register 233	IR233	8	8	2	ICLK	
0008 70EAh	ICU	Interrupt request register 234	IR234	8	8	2	ICLK	
0008 70EBh	ICU	Interrupt request register 235	IR235	8	8	2	ICLK	
0008 70ECh	ICU	Interrupt request register 236	IR236	8	8	2	ICLK	
0008 70EDh	ICU	Interrupt request register 237	IR237	8	8	2	ICLK	
0008 70EEh	ICU	Interrupt request register 238	IR238	8	8	2	ICLK	
0008 70EFh	ICU	Interrupt request register 239	IR239	8	8	2	ICLK	
0008 70F0h	ICU	Interrupt request register 240	IR240	8	8	2	ICLK	
0008 70F1h	ICU	Interrupt request register 241	IR241	8	8	2	ICLK	
0008 70F2h	ICU	Interrupt request register 242	IR242	8	8	2	ICLK	
0008 70F3h	ICU	Interrupt request register 243	IR243	8	8	2	ICLK	
0008 70F4h	ICU	Interrupt request register 244	IR244	8	8	2	ICLK	
0008 70F5h	ICU	Interrupt request register 245	IR245	8	8	2	ICLK	
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2	ICLK	
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2	ICLK	
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2	ICLK	
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2	ICLK	
0008 70FAh	ICU	Interrupt request register 250	IR250	8	8	2	ICLK	
0008 70FBh	ICU	Interrupt request register 251	IR251	8	8	2	ICLK	
0008 70FCh	ICU	Interrupt request register 252	IR252	8	8	2	ICLK	
0008 70FDh	ICU	Interrupt request register 253	IR253	8	8	2	ICLK	
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8	2	ICLK	
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8	2	ICLK	
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8	2	ICLK	
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8	2	ICLK	
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8	2	ICLK	
0008 7121h	ICU	DTC activation enable register 033	DTCER033	8	8	2	ICLK	
0008 7122h	ICU	DTC activation enable register 034	DTCER034	8	8	2	ICLK	
0008 7124h	ICU	DTC activation enable register 036	DTCER036	8	8	2	ICLK	
0008 7125h	ICU	DTC activation enable register 037	DTCER037	8	8	2	ICLK	
0008 7127h	ICU	DTC activation enable register 039	DTCER039	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (13/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7394h	ICU	Interrupt source priority register 148	IPR148	8	8	2 ICLK		ICUb
0008 7396h	ICU	Interrupt source priority register 150	IPR150	8	8	2 ICLK		
0008 7398h	ICU	Interrupt source priority register 152	IPR152	8	8	2 ICLK		
0008 739Ch	ICU	Interrupt source priority register 156	IPR156	8	8	2 ICLK		
0008 73A0h	ICU	Interrupt source priority register 160	IPR160	8	8	2 ICLK		
0008 73A1h	ICU	Interrupt source priority register 161	IPR161	8	8	2 ICLK		
0008 73A4h	ICU	Interrupt source priority register 164	IPR164	8	8	2 ICLK		
0008 73A6h	ICU	Interrupt source priority register 166	IPR166	8	8	2 ICLK		
0008 73AAh	ICU	Interrupt source priority register 170	IPR170	8	8	2 ICLK		
0008 73ADh	ICU	Interrupt source priority register 173	IPR173	8	8	2 ICLK		
0008 73B0h	ICU	Interrupt source priority register 176	IPR176	8	8	2 ICLK		
0008 73B3h	ICU	Interrupt source priority register 179	IPR179	8	8	2 ICLK		
0008 73B6h	ICU	Interrupt source priority register 182	IPR182	8	8	2 ICLK		
0008 73B7h	ICU	Interrupt source priority register 183	IPR183	8	8	2 ICLK		
0008 73B8h	ICU	Interrupt source priority register 184	IPR184	8	8	2 ICLK		
0008 73B9h	ICU	Interrupt source priority register 185	IPR185	8	8	2 ICLK		
0008 73BAh	ICU	Interrupt source priority register 186	IPR186	8	8	2 ICLK		
0008 73BBh	ICU	Interrupt source priority register 187	IPR187	8	8	2 ICLK		
0008 73BCh	ICU	Interrupt source priority register 188	IPR188	8	8	2 ICLK		
0008 73BDh	ICU	Interrupt source priority register 189	IPR189	8	8	2 ICLK		
0008 73BEh	ICU	Interrupt source priority register 190	IPR190	8	8	2 ICLK		
0008 73BFh	ICU	Interrupt source priority register 191	IPR191	8	8	2 ICLK		
0008 73C0h	ICU	Interrupt source priority register 192	IPR192	8	8	2 ICLK		
0008 73C1h	ICU	Interrupt source priority register 193	IPR193	8	8	2 ICLK		
0008 73C2h	ICU	Interrupt source priority register 194	IPR194	8	8	2 ICLK		
0008 73C3h	ICU	Interrupt source priority register 195	IPR195	8	8	2 ICLK		
0008 73C4h	ICU	Interrupt source priority register 196	IPR196	8	8	2 ICLK		
0008 73C5h	ICU	Interrupt source priority register 197	IPR197	8	8	2 ICLK		
0008 73C6h	ICU	Interrupt source priority register 198	IPR198	8	8	2 ICLK		
0008 73C7h	ICU	Interrupt source priority register 199	IPR199	8	8	2 ICLK		
0008 73C8h	ICU	Interrupt source priority register 200	IPR200	8	8	2 ICLK		
0008 73C9h	ICU	Interrupt source priority register 201	IPR201	8	8	2 ICLK		
0008 73CAh	ICU	Interrupt source priority register 202	IPR202	8	8	2 ICLK		
0008 73CBh	ICU	Interrupt source priority register 203	IPR203	8	8	2 ICLK		
0008 73CEh	ICU	Interrupt source priority register 206	IPR206	8	8	2 ICLK		
0008 73CFh	ICU	Interrupt source priority register 207	IPR207	8	8	2 ICLK		
0008 73D0h	ICU	Interrupt source priority register 208	IPR208	8	8	2 ICLK		
0008 73D6h	ICU	Interrupt source priority register 214	IPR214	8	8	2 ICLK		
0008 73D9h	ICU	Interrupt source priority register 217	IPR217	8	8	2 ICLK		
0008 73DCh	ICU	Interrupt source priority register 220	IPR220	8	8	2 ICLK		
0008 73DFh	ICU	Interrupt source priority register 223	IPR223	8	8	2 ICLK		
0008 73E2h	ICU	Interrupt source priority register 226	IPR226	8	8	2 ICLK		
0008 73E5h	ICU	Interrupt source priority register 229	IPR229	8	8	2 ICLK		
0008 73E8h	ICU	Interrupt source priority register 232	IPR232	8	8	2 ICLK		
0008 73EBh	ICU	Interrupt source priority register 235	IPR235	8	8	2 ICLK		
0008 73EEh	ICU	Interrupt source priority register 238	IPR238	8	8	2 ICLK		
0008 73F1h	ICU	Interrupt source priority register 241	IPR241	8	8	2 ICLK		
0008 73F4h	ICU	Interrupt source priority register 244	IPR244	8	8	2 ICLK		
0008 73F7h	ICU	Interrupt source priority register 247	IPR247	8	8	2 ICLK		
0008 73FAh	ICU	Interrupt source priority register 250	IPR250	8	8	2 ICLK		
0008 73FDh	ICU	Interrupt source priority register 253	IPR253	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (30/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C046h	PORT6	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C047h	PORT7	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C048h	PORT8	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C049h	PORT9	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Ah	PORTA	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Bh	PORTB	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Ch	PORTC	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Dh	PORTD	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Eh	PORTE	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Fh	PORTF	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C050h	PORTG	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C052h	PORTJ	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C060h	PORT0	Port input data register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C061h	PORT1	Port input data register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C062h	PORT2	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C063h	PORT3	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C064h	PORT4	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C065h	PORT5	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C066h	PORT6	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C067h	PORT7	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C068h	PORT8	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C069h	PORT9	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Ah	PORTA	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Bh	PORTB	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Ch	PORTC	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Dh	PORTD	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Eh	PORTE	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Fh	PORTF	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C070h	PORTG	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C072h	PORTJ	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C080h	PORT0	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C081h	PORT0	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C082h	PORT1	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C083h	PORT1	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C084h	PORT2	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C085h	PORT2	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C086h	PORT3	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C087h	PORT3	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C088h	PORT4	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C089h	PORT4	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Ah	PORT5	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Bh	PORT5	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Ch	PORT6	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Dh	PORT6	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Eh	PORT7	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Fh	PORT7	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C090h	PORT8	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C091h	PORT8	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C092h	PORT9	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C093h	PORT9	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C094h	PORTA	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (46/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 0268h	USB1	Pipe configuration register	PIPECFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 026Ch	USB1	Pipe maximum packet size register	PEMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 026Eh	USB1	Pipe cycle control register	PIPEPERI	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0270h	USB1	Pipe 1 control register	PIPE1CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	USBa
000A 0272h	USB1	Pipe 2 control register	PIPE2CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0274h	USB1	Pipe 3 control register	PIPE3CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0276h	USB1	Pipe 4 control register	PIPE4CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0278h	USB1	Pipe 5 control register	PIPE5CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 027Ah	USB1	Pipe 6 control register	PIPE6CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 027Ch	USB1	Pipe 7 control register	PIPE7CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	

Table 5.21 Timing of On-Chip Peripheral Modules (3)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V*1, $VREFH0 = 2.7$ V to $AVCC0$ *1,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V,
 $PCLK = 8$ to 50 MHz,
 $T_a = T_{opr}$
 High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit*2	Test Conditions
RSPI	Data output delay time	Master	Packages with 177 to 144 pins	t_{OD}	—	18	ns	Figure 5.43 to Figure 5.46 C = 30pF
			Packages with 100 pins or less		—	30		
		Slave	Packages with 177 to 144 pins		—	$3 \times t_{Pcyc} + 40$		
			Packages with 100 pins or less		—	$3 \times t_{Pcyc} + 50$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	Packages with 177 to 144 pins	t_{Dr}, t_{Df}	—	5	ns	
			Packages with 100 pins or less		—	10		
		Input			—	1	μs	
	SSL rise/fall time	Output	Packages with 177 to 144 pins	t_{SSLr}, t_{SSLf}	—	5	ns	
			Packages with 100 pins or less		—	10		
		Input			—	1	μs	
Slave access time				t_{SA}	—	4	t_{Pcyc}	Figure 5.45 and Figure 5.46 C = 30pF
Slave output release time				t_{REL}	—	3	t_{Pcyc}	

Note 1. When operation at 3.0 V or a lower voltage is needed, please contact a Renesas sales office.

Note 2. t_{Pcyc} : PCLK cycle

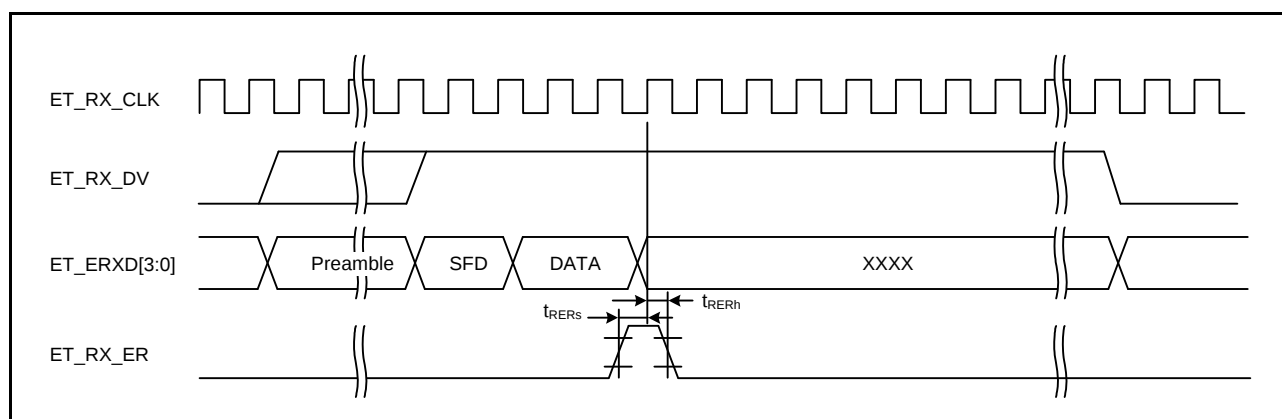


Figure 5.56 MII Reception Timing (Error Occurrence)

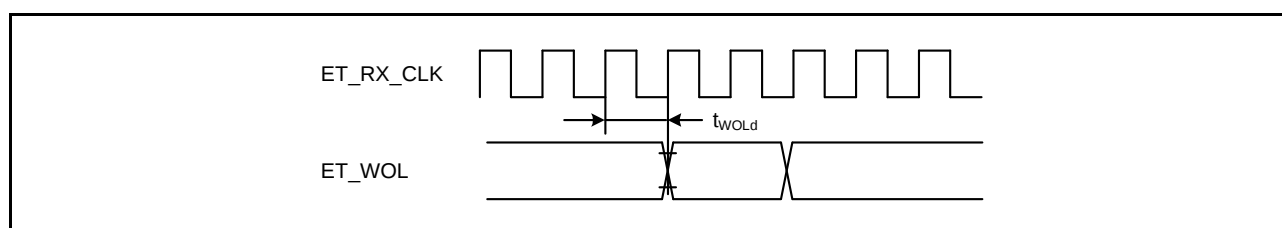


Figure 5.57 WOL Output Timing (MII)

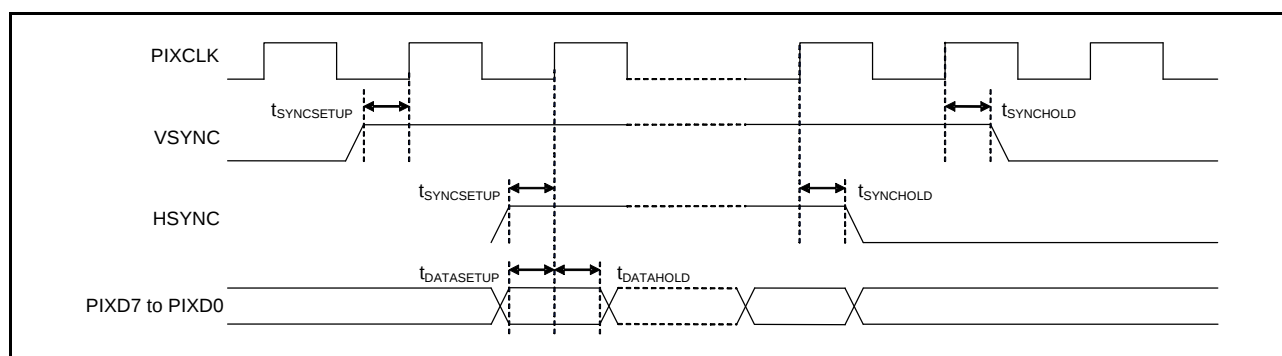


Figure 5.58 PDC Timing

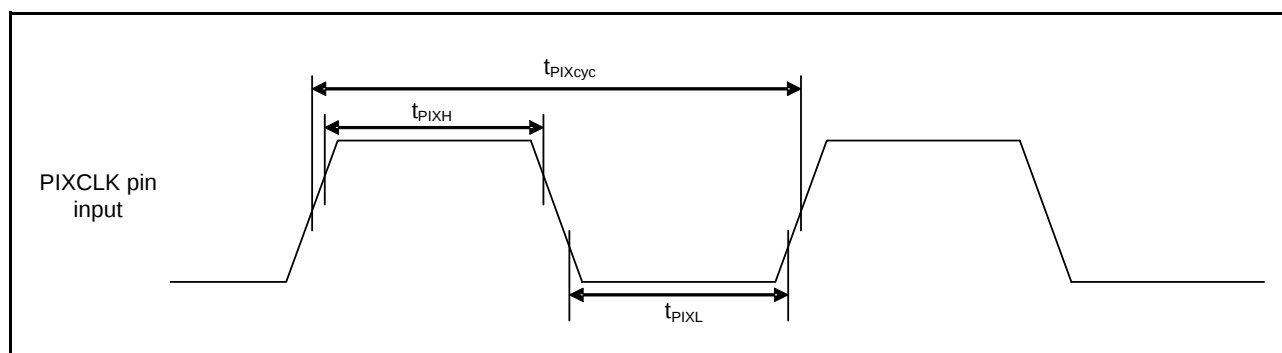


Figure 5.59 PDC Input Clock Characteristic

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

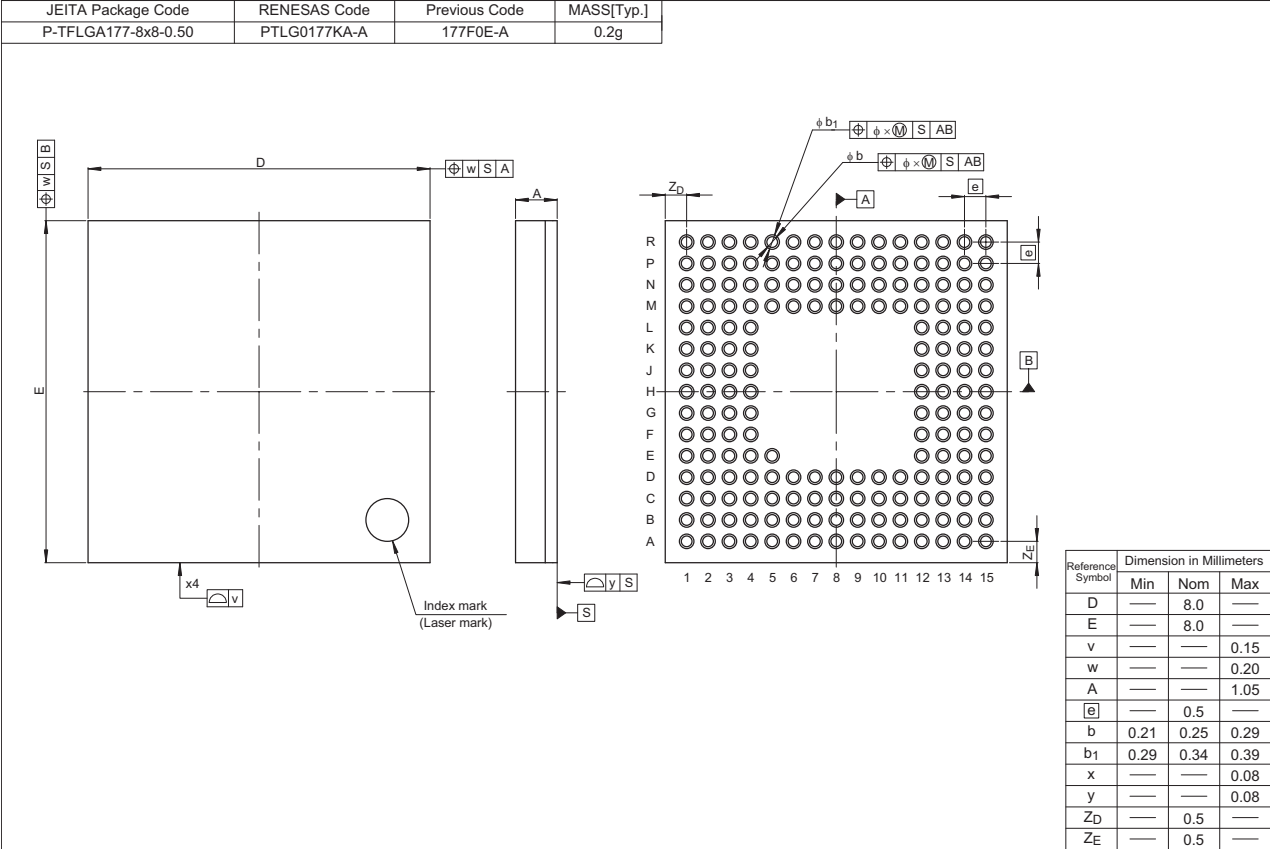


Figure A 177-pin TFLGA (PTLG0177KA-A)

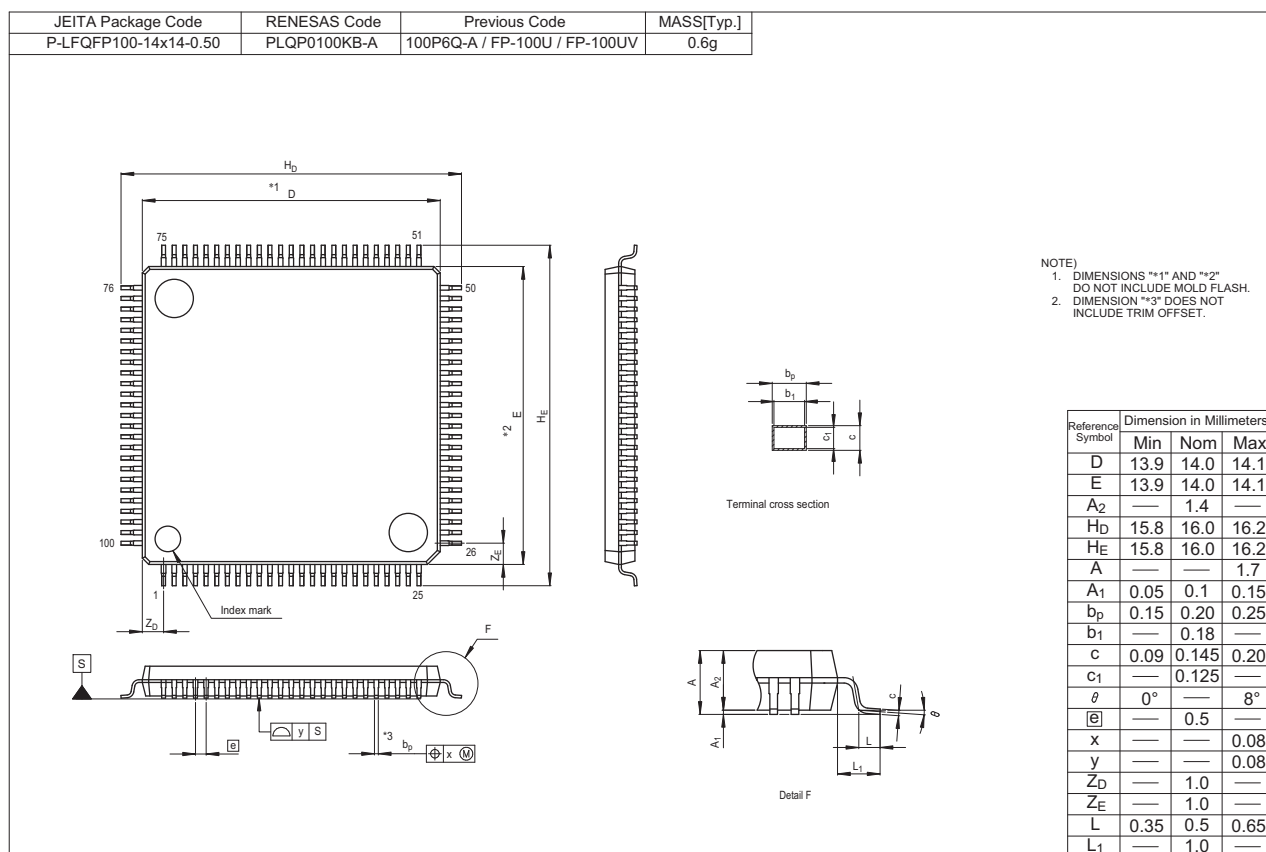


Figure G 100-pin LQFP (PLQP0100KB-A)

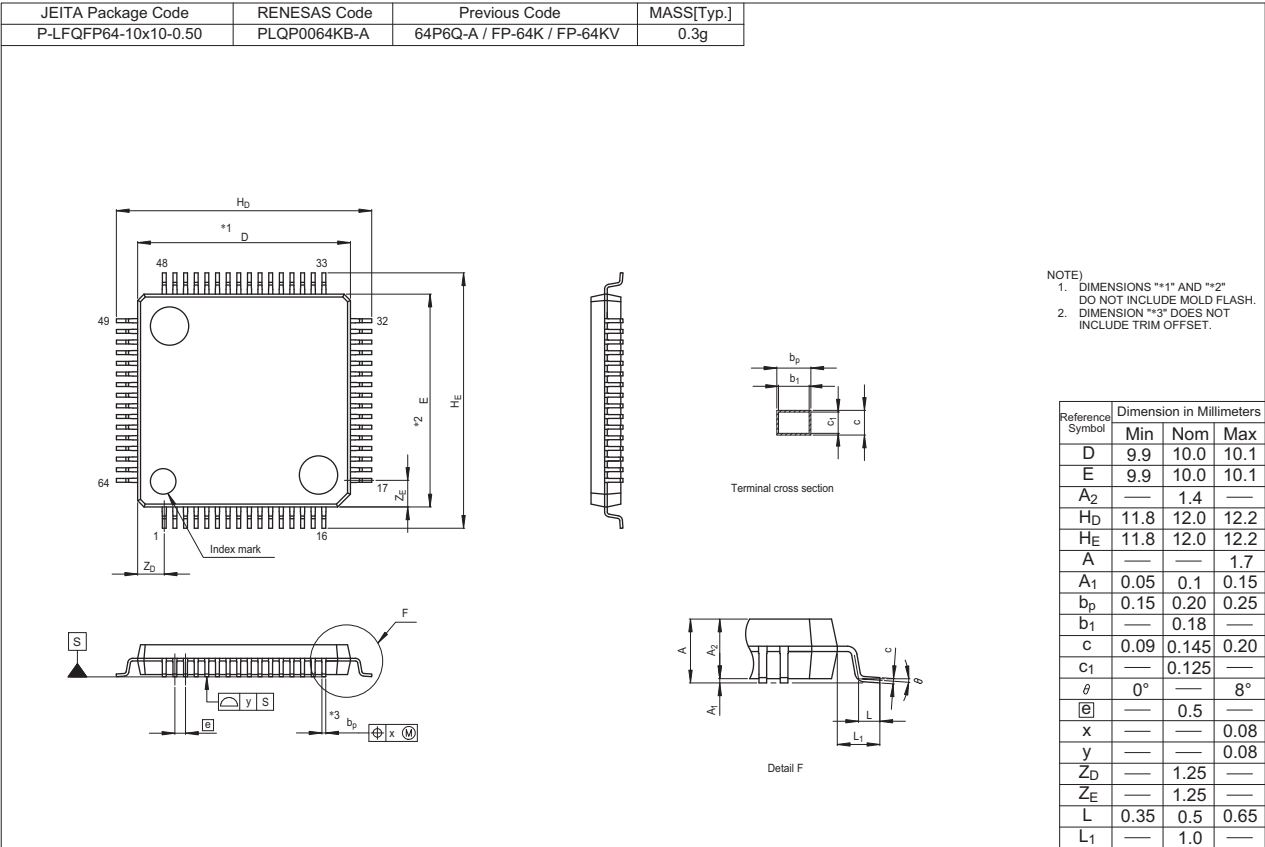


Figure I 64-pin LQFP (PLQP0064KB-A)

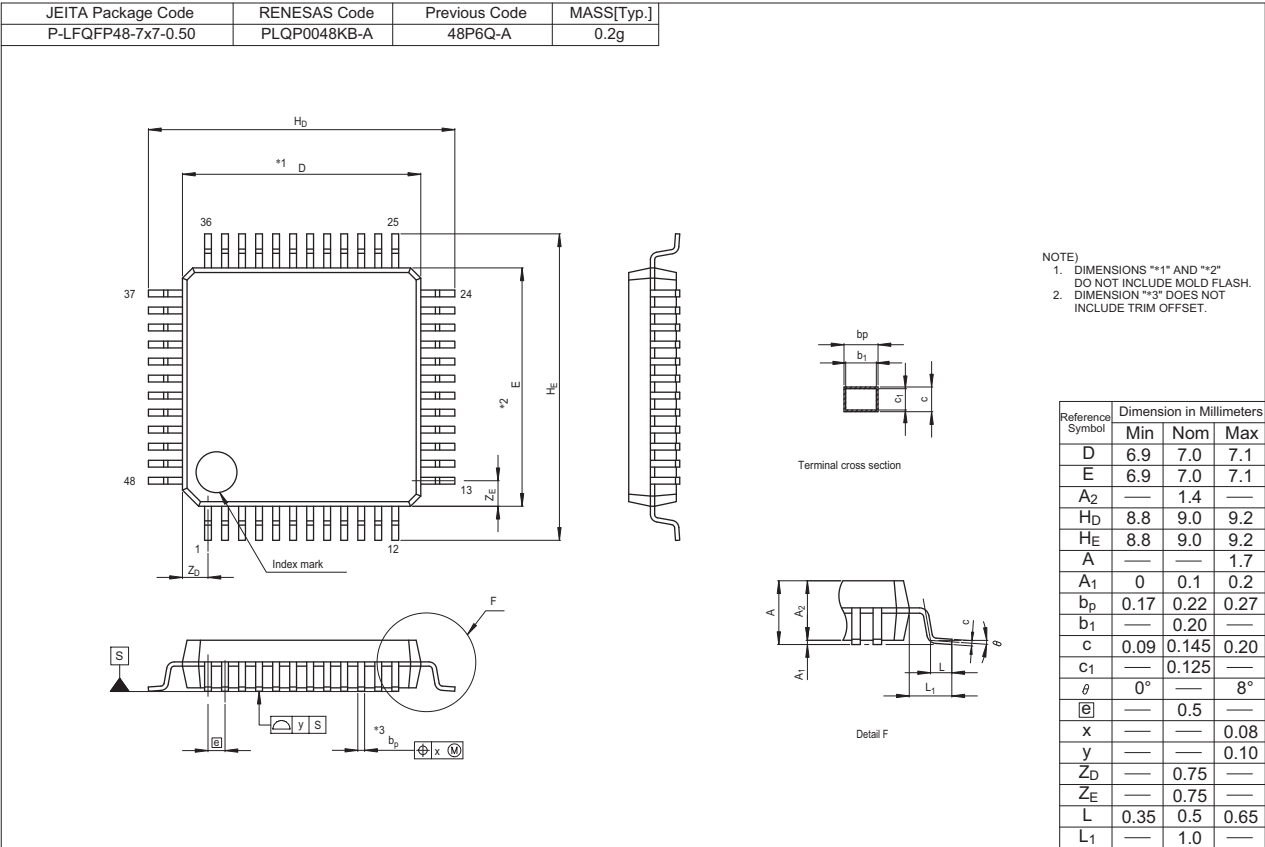


Figure J 48-pin LQFP (PLQP0048KB-A)

Rev.	Date	Description	
		Page	Summary
1.60	Mar 13. 2013	Feature	
		1	Changed
		1. Overview	
		2 to 7	Table 1.1 Outline of Specifications: changed, note added
		8	Table 1.2 Comparison of Functions for Different Packages in the RX63N/RX631 Group, changed
		9 to 15	Table 1.3 List of Products, changed
		16	Figure 1.1 How to Read the Product Part No., changed
		17	Figure 1.2 Block Diagram, changed
		24 to 32	Figure 1.3 to Figure 1.11 Pin Assignment: note, added
		53 to 57	Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA), added
		62 to 64	Table 1.11 List of Pins and Pin Functions (64-Pin LQFP), added
		65, 66	Table 1.12 List of Pins and Pin Functions (48-Pin LQFP), added
		3. Address Space	
		71	Figure 3.1 Memory Map in Each Operating Mode, changed
		4. I/O Registers	
		75 to 120	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics	
		All	Characteristics and timing conditions in the tables, changed
		124, 125	Table 5.4 DC Characteristics (3), changed
		126	Table 5.5 DC Characteristics (4), changed
		127	5.3 AC Characteristics, changed
		130, 131	Table 5.11, Clock Timing (Except for Sub-Clock Related): Condition and the table, changed, note, added
		132	Table 5.12 Clock Timing (Sub-Clock Related): Condition and the table, changed, note, added
		176	Table 5.33 Battery Backup Function Characteristics: Condition, changed
		Appendix 1. Package Dimensions	
		189	Figure H 64-pin LQFP (PLQP0064KB-A), added
		190	Figure I 48-pin LQFP (PLQP0048KB-A), added
1.70	Oct 08. 2013	Features	
		1	changed
		1. Overview	
		2 to 7	Table 1.1 Outline of Specifications, General I/O ports, Packages, changed, Parallel data capture unit (PDC), added.
		8	Table 1.2 Comparison of Functions for Different Packages in the RX63N/RX631 Group, 64-pin LQFP, changed, 64-pin TFLGA, Parallel data capture unit (PDC), added.
		9 to 16	Table 1.3 List of Products, changed.
		17	Figure 1.1 How to Read the Product Part No., changed
		18	Figure 1.2 Block Diagram, changed
		19 to 24	Table 1.4 Pin Functions, changed, Parallel data capture unit (PDC), added
		32	Figure 1.10 Pin Assignment (64-Pin TFLGA), added
		35 to 40	Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA), changed
		41 to 45	Table 1.6 List of Pin and Pin Functions (176-Pin LQFP), changed
		46 to 50	Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA), changed
		51 to 55	Table 1.8 List of Pins and Pin Functions (144-Pin LQFP), changed
		65 to 66	Table 1.11 List of Pins and Pin Functions (64-Pin TFLGA), added
		3. Address Space	
		76	Figure 3.1 Memory Map in Each Operating Mode, changed
		4. I/O Registers	
		79	(4) Restrictions in Relation to RMPA and String-Manipulation Instructions, added