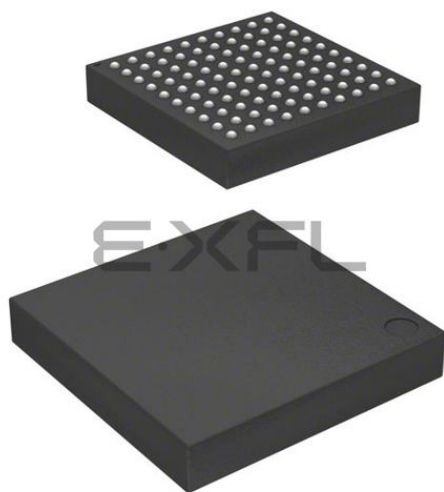




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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631dcdlj-u0

Table 1.4 Pin Functions (4/6)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCId)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for clock signals.
	RXD12	Input	Input pin for data reception.
	TXD12	Output	Output pin for data transmission.
	CTS12#	Input	Transmit/receive start control input pins
	RTS12#	Output	Transmit/receive start control output pins
	• Simple I ² C mode		
	SSCL12	I/O	Input/output pins for the I ² C clock
	SSDA12	I/O	Input/output pins for the I ² C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pins for the clock
	SMISO12	I/O	Input/output pins for slave transmit data.
	SMOSI12	I/O	Input/output pins for master transmit data.
	SS12#	Input	Input pins for chip select signals
	• Extended serial mode		
	RXDX12	Input	Input pin for receive data
	TXDX12	Output	Output pin for transmit data
	SIOX12	I/O	Input/output pin for Transmit/receive data
I ² C bus interface	SCL0[FM+], SCL1 to SCL3	I/O	Input/output pin for clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0[FM+], SDA1 to SDA3	I/O	Input/output pin for data. Bus can be directly driven by the N-channel open drain output.
Ethernet controller	REF50CK	Input	50-MHz reference clock. This pin inputs reference signals for transmission/reception timings in RMII mode.
	RMII_CRS_DV	Input	Indicates that there are carrier detection signals and valid receive data on RMII_RXD1 and RMII_RXD0 in RMII mode.
	RMII_TXD0, RMII_TXD1	Output	2-bit transmit data in RMII mode.
	RMII_RXD0, RMII_RXD1	Input	2-bit receive data in RMII mode.
	RMII_TXD_EN	Output	Output pin for data transmit enable signals in RMII mode.
	RMII_RX_ER	Input	Indicates an error has occurred during reception of data in RMII mode.
	ET_CRS	Input	Carrier detection/data reception enable pin.
	ET_RX_DV	Input	Indicates that there are valid receive data on ET_ERXD3 to ET_ERXD0.
	ET_EXOUT	Output	General-purpose external output pin.
	ET_LINKSTA	Input	Inputs link status from the PHY-LSI.
	ET_ETXD0 to ET_ETXD3	Output	4 bits of MII transmit data.
	ET_ERXD0 to ET_ERXD3	Input	4 bits of MII receive data.
	ET_TX_EN	Output	Transmit enable pin. Indicates that transmit data is ready on ET_ETXD3 to ET_ETXD0.
	ET_TX_ER	Output	Transmit error pin. Notifies the PHY_LSI of an error during transmission.
	ET_RX_ER	Input	Receive error pin. Recognizes an error during reception.
	ET_TX_CLK	Input	Transmit clock pin. This pin inputs reference signals for output timings from ET_TX_EN, ET_ETXD3 to ET_ETXD0, and ET_TX_ER.
	ET_RX_CLK	Input	Receive clock pin. This pin inputs reference signals for input timings to ET_RX_DV, ET_ERXD3 to ET_ERXD0, and ET_RX_ER.
	ET_COL	Input	Inputs collision detection signals.
	ET_WOL	Output	Receives Magic packets.
	ET_MDC	Output	Outputs reference clock signals for information transfer via ET_MDIO.

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
M2		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
M3		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/USB0_VBUSEN/ PIXCLK		
M4		P86		TIOCA0	PIXD1		
M5		P13		MTIOC0B/TIOCA5/TMO3/ PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
M6		P56	WR2#/BC2#/ EDACK1	MTIOC3C/TIOCA1			
M7		P54	ALE/EDACK0	MTIOC4B/TMCI1	ET_LINKSTA/CTS2#/ RTS2#/SS2#/CTX1		
M8		P53*2	BCLK				
M9		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
M10		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	ET_ETXD2/SCK8/ RSPCKA		
M11		P81	EDACK0	MTIOC3D/PO27	ET_ETXD0/RMII_TXD0/ RXD10/SMISO10/SSCL10		
M12		P77	CS7#	PO23	ET_RX_ER/RMII_RX_ER/ TXD11/SMOSI11/SSDA11		
M13		PB7	A15	MTIOC3B/TIOCB5/PO31	ET_CRS/RMII_CRS_DV/ TXD9/SMOSI9/SSDA9		
M14		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	ET_ETXD0/RMII_TXD0/ SCK9		
M15		PB4	A12	TIOCA4/PO28	ET_TX_EN/ RMII_TXD_EN/CTS9#/ RTS9#/SS9#		
N1	VCC						
N2		P23	EDACK0	MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7		
N3		P22	EDREQ0	MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0/USB0_DRPD/ PIXD6		
N4		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ USB1_DPUPE/PIXD0	IRQ5	
N5		P12		MTIC5U/TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
N6		P57	WAIT#/WR3#/ BC3#/EDREQ1				
N7		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	ET_EXOUT/CRX1	IRQ10	
N8	VCC_USB						
N9		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
N10		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	ET_COL/TXD8/SMOSI8/ SSDA8/MISOA	IRQ14	
N11		P82	EDREQ1	MTIOC4A/PO28	ET_ETXD1/RMII_TXD1/ TXD10/SMOSI10/SSDA10		
N12		PC3	A19	MTIOC4D/TCLKB/PO24	ET_TX_ER/TXD5/ SMOSI5/SSDA5/IETXD		
N13		PC0	A16	MTIOC3C/TCLKC/PO17	ET_ERXD3/CTS5#/ RTS5#/SS5#/SSLA1/ SCL3	IRQ14	
N14		P73	CS3#	PO16	ET_WOL		
N15	VSS						

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (5/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
P1	VSS						
P2		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/ IETXD/USB1_VBUS/ PIXD3	IRQ7	ADTRG#
P3		P87		TIOCA2	PIXD2		
P4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
P5		P10		MTIC5W/TMRI3		IRQ0	
P6	VCC_USB						
P7	VSS_USB						
P8					USB1_DP		
P9		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
P10		P83	EDACK1	MTIOC4C	ET_CRS/RMII_CRS_DV/ CTS10#/RTS10#/SS10#		
P11		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TIOCA6/TMC12/PO30	ET_ETXD3/RXD8/ SMISO8/SSCL8/MOSIA	IRQ13	
P12		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TIOCC6/TCLKE/TMC11/ PO25/POE0#	ET_TX_CLK/SCK5/ CTS8#/RTS8#/SS8#/ SSLA0		
P13		PC2	A18	MTIOC4B/TCLKA/PO21	ET_RX_DV/RXD5/ SMISO5/SSCL5/SSLA3/ IERXD		
P14		P75	CS5#	PO20	ET_ERXD0/RMII_RXD0/ SCK11		
P15	VCC						
R1		P21		MTIOC1B/TIOCA3/ TMC10/PO1	RXD0/SMISO0/SSCL0/ SCL1/USB0_EXICEN/ PIXD5	IRQ9	
R2		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/SSDA0/ SDA1/USB0_ID/PIXD4	IRQ8	
R3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOU	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
R4		P85					
R5		P11		MTIC5V/TMC13	SCK2	IRQ1	
R6					USB0_DM		
R7					USB0_DP		
R8					USB1_DM		
R9		P84					
R10	VSS						
R11	VCC						
R12		P80	EDREQ0	MTIOC3B/PO26	ET_TX_EN/ RMII_TXD_EN/SCK10		
R13		P76	CS6#	PO22	ET_RX_CLK/REF50CK/ RXD11/SMISO11/SSCL11		
R14		P74	CS4#	PO19	ET_ERXD1/RMII_RXD1/ CTS11#/RTS11#/SS11#		
R15		PC1	A17	MTIOC3A/TCLKD/PO18	ET_ERXD2/SCK5/SSLA2/ SDA3	IRQ12	

Note 1. 176-pin LFBGA does not have E5 pin

Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (1/5)

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
1	AVSS0						
2		P05				IRQ13	DA1
3	VREFH						
4		P03				IRQ11	DA0
5	VREFL						
6		P02		TMCI1	SCK6	IRQ10	AN020
7		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019
8		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
9		PF5				IRQ4	
10	EMLE						
11		PJ5					
12	VSS						
13		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
14	VCL						
15	VBATT						
16	NC						
17	TRST#	PF4					
18	MD/FINED						
19	XCIN						
20	XCOUT						
21	RES#						
22	XTAL	P37					
23	VSS						
24	EXTAL	P36					
25	VCC						
26		P35				NMI	
27		P34		MTIOC0A/TMCI3/PO12/ POE2#	SCK6/SCK0/ USB0_DPRPD	IRQ4	
28		P33		MTIOC0D/TIOC0D/ TMRI3/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0/PCKO	IRQ3-DS	
29		P32		MTIOC0C/TIOCC0/TMO3/ PO10/RTCOU/RTCIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC	IRQ2-DS	
30	TMS	PF3					
31	TDI	PF2			RXD1/SMISO1/SSCL1		
32		P31		MTIOC4D/TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
33		P30		MTIOC4B/TMRI3/PO8/ RTCIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
34	TCK/FINEC	PF1			SCK1		
35	TDO	PF0			TXD1/SMOSI1/SSDA1		
36		P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		
37		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
38		P25	CS5#/EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC		ADTRG0#
39	VCC						
40		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/USB0_VBUSEN/ PIXCLK		

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (2/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
D5	VCC						
D6		P93	A19		CTS7#/RTS7#/SS7#		AN017
D7		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
D8		P60	CS0#				
D9		P64	CS4#/WE#				
D10		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
D11	VCC						
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	RSPCKB/ET_RX_CLK/ REF50CK	IRQ5	AN3
D13		PE6	D14[A14/D14]	TIOCA11	MOSIB	IRQ6	AN4
E1	VSS						
E2	VCL						
E3		PJ5					
E4	EMLE						
E5		P44				IRQ12-DS	AN004
E10		PA0	A0/BC0#	MTIOC4A/TIOCA0/ PO16	SSLA1/ET_TX_EN/ RMII_TXD_EN		
E11		P66	CS6#/DQM0		CTX2*2		
E12		P65	CS5#/CKE				
E13		P67	CS7#/DQM1		CRX2*2	IRQ15	
F1	XCIN						
F2	XCOUT						
F3		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
F4	VBATT						
F10		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/SSCL5/ ET_MDIO	IRQ6-DS	
F11	VSS						
F12		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2/ET_WOL	IRQ11	
F13		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
G1	XTAL	P37					
G2	RES#						
G3	MD/FINED						
G4	BSCANP						
G10		PA5	A5	TIOCB1/PO21	RSPCKA/ET_LINKSTA		
G11		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	CTS5#/RTS5#/SS5# MOSIA/ET_EXOUT		
G12	VCC						
G13		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0/ET_MDC	IRQ5-DS	
H1	EXTAL	P36					
H2	VCC						
H3	VSS						
H4		P35				NMI	
H10		P72	CS2#		ET_MDC		
H11		P71	CS1#		ET_MDIO		

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (1/4)

Pin No. 100-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
1	VREFH						
2	EMLE						
3	VREFL						
4		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
5	VCL						
6	VBATT						
7	MD/FINED						
8	XCIN						
9	XCOUT						
10	RES#						
11	XTAL	P37					
12	VSS						
13	EXTAL	P36					
14	VCC						
15		P35				NMI	
16	TRST#	P34		MTIOC0A/TMC13/ PO12/POE2#	SCK6/SCK0/ USB0_DPRPD	IRQ4	
17		P33		MTIOC0D/TIOC0D/ TMR13/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0*1	IRQ3-DS	
18		P32		MTIOC0C/TIOC0C/ TMO3/PO10/RTCOU1/ RTIC12	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0*1/ USB0_VBUSEN	IRQ2-DS	
19	TMS	P31		MTIOC4D/TMC12/PO9/ RTIC11	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
20	TDI	P30		MTIOC4B/TMR13/PO8/ RTIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
21	TCK/FINEC	P27	CS7#	MTIOC2B/TMC13/PO7	SCK1/RSPCKB		
22	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
23		P25	CS5#/EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3/ USB0_DPRPD		ADTRG0#
24		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMR11/PO4	SCK3/USB0_VBUSEN		
25		P23	EDACK0	MTIOC3D/MTCLKD/ TIOC3D/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE		
26		P22	EDREQ0	MTIOC3B/MTCLKC/ TIOC3C/TMO0/PO2	SCK0/USB0_DRPD		
27		P21		MTIOC1B/TIOCA3/ TMC10/PO1	RXD0/SMISO0/SSCL0/ USB0_EXICEN	IRQ9	
28		P20		MTIOC1A/TIOCB3/ TMR10/PO0	TXD0/SMOSI0/SSDA0/ USB0_ID	IRQ8	
29		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2- DS/IETXD	IRQ7	ADTRG#
30		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOU1	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/MOSIA/SCL2- DS/IETXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively. Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

- Longword-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.L #SFR_DATA, [R1]
CMP [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

$$\begin{aligned} \text{Number of access cycles to I/O registers} = & \text{Number of bus cycles for internal main bus 1} + \\ & \text{Number of divided clock synchronization cycles} + \\ & \text{Number of bus cycles for internal peripheral busses 1 to 6} \end{aligned}$$

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.

The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.

In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.

When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

(4) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

Table 4.1 List of I/O Registers (Address Order) (6/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2	ICLK	ICUb
0008 7048h	ICU	Interrupt request register 072	IR072	8	8	2	ICLK	
0008 7049h	ICU	Interrupt request register 073	IR073	8	8	2	ICLK	
0008 704Ah	ICU	Interrupt request register 074	IR074	8	8	2	ICLK	
0008 704Bh	ICU	Interrupt request register 075	IR075	8	8	2	ICLK	
0008 704Ch	ICU	Interrupt request register 076	IR076	8	8	2	ICLK	
0008 704Dh	ICU	Interrupt request register 077	IR077	8	8	2	ICLK	
0008 704Eh	ICU	Interrupt request register 078	IR078	8	8	2	ICLK	
0008 704Fh	ICU	Interrupt request register 079	IR079	8	8	2	ICLK	
0008 705Ah	ICU	Interrupt request register 090	IR090	8	8	2	ICLK	
0008 705Bh	ICU	Interrupt request register 091	IR091	8	8	2	ICLK	
0008 705Ch	ICU	Interrupt request register 092	IR092	8	8	2	ICLK	
0008 705Dh	ICU	Interrupt request register 093	IR093	8	8	2	ICLK	
0008 7062h	ICU	Interrupt request register 098	IR098	8	8	2	ICLK	
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2	ICLK	
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2	ICLK	
0008 706Bh	ICU	Interrupt request register 107	IR107	8	8	2	ICLK	
0008 706Ch	ICU	Interrupt request register 108	IR108	8	8	2	ICLK	
0008 706Dh	ICU	Interrupt request register 109	IR109	8	8	2	ICLK	
0008 706Eh	ICU	Interrupt request register 110	IR110	8	8	2	ICLK	
0008 706Fh	ICU	Interrupt request register 111	IR111	8	8	2	ICLK	
0008 7070h	ICU	Interrupt request register 112	IR112	8	8	2	ICLK	
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2	ICLK	
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8	2	ICLK	
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8	2	ICLK	
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8	2	ICLK	
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8	2	ICLK	
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8	2	ICLK	
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8	2	ICLK	
0008 7080h	ICU	Interrupt request register 128	IR128	8	8	2	ICLK	
0008 7081h	ICU	Interrupt request register 129	IR129	8	8	2	ICLK	
0008 7082h	ICU	Interrupt request register 130	IR130	8	8	2	ICLK	
0008 7083h	ICU	Interrupt request register 131	IR131	8	8	2	ICLK	
0008 7084h	ICU	Interrupt request register 132	IR132	8	8	2	ICLK	
0008 7085h	ICU	Interrupt request register 133	IR133	8	8	2	ICLK	
0008 7086h	ICU	Interrupt request register 134	IR134	8	8	2	ICLK	
0008 7087h	ICU	Interrupt request register 135	IR135	8	8	2	ICLK	
0008 7088h	ICU	Interrupt request register 136	IR136	8	8	2	ICLK	
0008 7089h	ICU	Interrupt request register 137	IR137	8	8	2	ICLK	
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8	2	ICLK	
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8	2	ICLK	
0008 708Ch	ICU	Interrupt request register 140	IR140	8	8	2	ICLK	
0008 708Dh	ICU	Interrupt request register 141	IR141	8	8	2	ICLK	
0008 708Eh	ICU	Interrupt request register 142	IR142	8	8	2	ICLK	
0008 708Fh	ICU	Interrupt request register 143	IR143	8	8	2	ICLK	
0008 7090h	ICU	Interrupt request register 144	IR144	8	8	2	ICLK	
0008 7091h	ICU	Interrupt request register 145	IR145	8	8	2	ICLK	
0008 7092h	ICU	Interrupt request register 146	IR146	8	8	2	ICLK	
0008 7093h	ICU	Interrupt request register 147	IR147	8	8	2	ICLK	
0008 7094h	ICU	Interrupt request register 148	IR148	8	8	2	ICLK	
0008 7095h	ICU	Interrupt request register 149	IR149	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (17/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 81A8h	TPU8	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 81AAh	TPU8	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81B0h	TPU9	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B1h	TPU9	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B2h	TPU9	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 81B3h	TPU9	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 81B4h	TPU9	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81B5h	TPU9	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B6h	TPU9	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81B8h	TPU9	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81BAh	TPU9	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81BCh	TPU9	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 81BEh	TPU9	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 81C0h	TPU10	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C1h	TPU10	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C2h	TPU10	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C4h	TPU10	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81C5h	TPU10	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C6h	TPU10	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81C8h	TPU10	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81CAh	TPU10	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81D0h	TPU11	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D1h	TPU11	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D2h	TPU11	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D4h	TPU11	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81D5h	TPU11	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D6h	TPU11	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81D8h	TPU11	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81DAh	TPU11	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81E6h	PPG0	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E7h	PPG0	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81E8h	PPG0	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81E9h	PPG0	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EAh	PPG0	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EBh	PPG0	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81ECh ^{*1}	PPG0	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EDh ^{*2}	PPG0	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EEh ^{*1}	PPG0	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	
0008 81EFh ^{*2}	PPG0	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	
0008 81F0h	PPG1	PPG trigger select register	PTRSLR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F6h	PPG1	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F7h	PPG1	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F8h	PPG1	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81F9h	PPG1	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FAh	PPG1	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81FBh	PPG1	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FCh ^{*3}	PPG1	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FDh ^{*4}	PPG1	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FEh ^{*3}	PPG1	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	
0008 81FFh ^{*4}	PPG1	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (35/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C344h	ICU	Group 1 interrupt enable register	GEN01	32	32	1 to 2PCLKB	2 ICLK	ICUb
0008 C348h	ICU	Group 2 interrupt enable register	GEN02	32	32	1 to 2PCLKB	2 ICLK	
0008 C34Ch	ICU	Group 3 interrupt enable register	GEN03	32	32	1 to 2PCLKB	2 ICLK	
0008 C350h	ICU	Group 4 interrupt enable register	GEN04	32	32	1 to 2PCLKB	2 ICLK	
0008 C354h	ICU	Group 5 interrupt enable register	GEN05	32	32	1 to 2PCLKB	2 ICLK	
0008 C358h	ICU	Group 6 interrupt enable register	GEN06	32	32	1 to 2PCLKB	2 ICLK	
0008 C370h	ICU	Group 12 interrupt enable register	GEN12	32	32	1 to 2PCLKB	2 ICLK	
0008 C380h	ICU	Group 0 interrupt clear register	GCR00	32	32	1 to 2PCLKB	2 ICLK	
0008 C384h	ICU	Group 1 interrupt clear register	GCR01	32	32	1 to 2PCLKB	2 ICLK	
0008 C388h	ICU	Group 2 interrupt clear register	GCR02	32	32	1 to 2PCLKB	2 ICLK	
0008 C38Ch	ICU	Group 3 interrupt clear register	GCR03	32	32	1 to 2PCLKB	2 ICLK	
0008 C390h	ICU	Group 4 interrupt clear register	GCR04	32	32	1 to 2PCLKB	2 ICLK	
0008 C394h	ICU	Group 5 interrupt clear register	GCR05	32	32	1 to 2PCLKB	2 ICLK	
0008 C398h	ICU	Group 6 interrupt clear register	GCR06	32	32	1 to 2PCLKB	2 ICLK	
0008 C3C0h	ICU	Unit select register	SEL	32	32	1 to 2PCLKB	2 ICLK	
0008 C400h	RTC	64-Hz counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK	RTCa
0008 C402h	RTC	Second counter	RSECCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C404h	RTC	Minute counter	RMINCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C406h	RTC	Hour counter	RHRCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C408h	RTC	Day-of-week counter	RWKCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Ah	RTC	Date counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Ch	RTC	Month counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Eh	RTC	Year counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 C410h	RTC	Second alarm register	RSECAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C412h	RTC	Minute alarm register	RMINAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C414h	RTC	Hour alarm register	RHRAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C416h	RTC	Day-of-week alarm register	RWKAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C418h	RTC	Date alarm register	RDAYAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C41Ah	RTC	Month alarm register	RMONAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C41Ch	RTC	Year alarm register	RYRAR	16	16	2, 3 PCLKB	2 ICLK	
0008 C41Eh	RTC	Year alarm enable register	RYRAREN	8	8	2, 3 PCLKB	2 ICLK	
0008 C422h	RTC	RTC control register 1	RCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C424h	RTC	RTC control register 2	RCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 C426h	RTC	RTC control register 3	RCR3	8	8	2, 3 PCLKB	2 ICLK	
0008 C428h	RTC	RTC control register 4	RCR4	8	8	2, 3 PCLKB	2 ICLK	
0008 C42Ah	RTC	Frequency register H	RFRH	16	16	2, 3 PCLKB	2 ICLK	
0008 C42Ch	RTC	Frequency register L	RFRL	16	16	2, 3 PCLKB	2 ICLK	
0008 C42Eh	RTC	Time error adjustment register	RADJ	8	8	2, 3 PCLKB	2 ICLK	
0008 C440h	RTC	Time capture control register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK	
0008 C442h	RTC	Time capture control register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C444h	RTC	Time capture control register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 C452h	RTC	Second capture register 0	RSECCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C454h	RTC	Minute capture register 0	RMINCP0	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (40/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 0054h	USB0	USB request type register	USBREQ	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0056h	USB0	USB request value register	USBVAL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0058h	USB0	USB request index register	USBINDX	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 005Ah	USB0	USB request length register	USBLENG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 005Ch	USB0	DCP configuration register	DCPCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 005Eh	USB0	DCP maximum packet size register	DCPMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0060h	USB0	DCP control register	DCPCTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0064h	USB0	Pipe window select register	PIPESEL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	USBa
000A 0068h	USB0	Pipe configuration register	PIPECFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 006Ch	USB0	Pipe maximum packet size register	PIPEMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	

Table 4.1 List of I/O Registers (Address Order) (48/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 02A0h	USB1	Pipe 5 transaction counter enable register	PIPE5TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 02A2h	USB1	Pipe 5 transaction counter register	PIPE5TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0400h	USB	Deep standby USB transceiver control/pin monitor register	DPUSR0R	32	32	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0404h	USB	Deep standby USB suspend/resume interrupt register	DPUSR1R	32	32	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0500h	PDC	PDC Control Register 0	PCCR0	32	32	2, 3PCLKA	2 ICLK	PDC
000A 0504h	PDC	PDC Control Register 1	PCCR1	32	32	2, 3PCLKA	2 ICLK	
000A 0508h	PDC	PDC Status Register	PCSR	32	32	2, 3PCLKA	2 ICLK	
000A 050Ch	PDC	PDC Pin Monitor Register	PCMONR	32	32	2, 3PCLKA	2 ICLK	
000A 0510h	PDC	PDC Receive Data Register	PCDR	32	32	2, 3PCLKA	2 ICLK	
000A 0514h	PDC	Vertical Capture Register	VCR	32	32	2, 3PCLKA	2 ICLK	
000A 0518h	PDC	Horizontal Capture Register	HCR	32	32	2, 3PCLKA	2 ICLK	
000C 0000h	EDMAC	EDMAC mode register	EDMR	32	32	5, 6 PCLKA	—	EDMAC
000C 0008h	EDMAC	EDMAC transmit request register	EDTRR	32	32	5, 6 PCLKA	—	
000C 0010h	EDMAC	EDMAC receive request register	EDRRR	32	32	5, 6 PCLKA	—	
000C 0018h	EDMAC	Transmit descriptor list start address register	TDLAR	32	32	5, 6 PCLKA	—	
000C 0020h	EDMAC	Receive descriptor list start address register	RDLAR	32	32	5, 6 PCLKA	—	
000C 0028h	EDMAC	ETHERC/EDMAC status register	EESR	32	32	5, 6 PCLKA	—	
000C 0030h	EDMAC	ETHERC/EDMAC status interrupt permission register	EESIPR	32	32	5, 6 PCLKA	—	
000C 0038h	EDMAC	Transmit/receive status copy enable register	TRSCER	32	32	5, 6 PCLKA	—	
000C 0040h	EDMAC	Receive missed-frame counter register	RMFCR	32	32	5, 6 PCLKA	—	
000C 0048h	EDMAC	Transmit FIFO threshold register	TFTR	32	32	5, 6 PCLKA	—	
000C 0050h	EDMAC	FIFO depth register	FDR	32	32	5, 6 PCLKA	—	
000C 0058h	EDMAC	Receiving method control register	RMCR	32	32	5, 6 PCLKA	—	
000C 0064h	EDMAC	Transmit FIFO underrun counter	TFUCR	32	32	5, 6 PCLKA	—	
000C 0068h	EDMAC	Receive FIFO overflow counter	RFOCR	32	32	5, 6 PCLKA	—	
000C 006Ch	EDMAC	Independent output signal setting register	IOSR	32	32	5, 6 PCLKA	—	EDMAC
000C 0070h	EDMAC	Flow control start FIFO threshold setting register	FCFTR	32	32	5, 6 PCLKA	—	
000C 0078h	EDMAC	Receive data padding insert register	RPADIR	32	32	5, 6 PCLKA	—	
000C 007Ch	EDMAC	Transmit interrupt setting register	TRIMD	32	32	5, 6 PCLKA	—	
000C 00C8h	EDMAC	Receive buffer write address register	RBWAR	32	32	5, 6 PCLKA	—	
000C 00CCh	EDMAC	Receive descriptor fetch address register	RDFAR	32	32	5, 6 PCLKA	—	
000C 00D4h	EDMAC	Transmit buffer read address register	TBRAR	32	32	5, 6 PCLKA	—	
000C 00D8h	EDMAC	Transmit descriptor fetch address register	TDFAR	32	32	5, 6 PCLKA	—	

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, VCC_USB	−0.3 to +4.6	V
V _{BATT} power supply voltage		V _{BATT}	−0.3 to +4.6	V
Input voltage (except for ports for 5 V tolerant*1)		V _{in}	−0.3 to VCC + 0.3	V
Input voltage (ports for 5 V tolerant*1)		V _{in}	−0.3 to +5.8	V
Reference power supply voltage		VREFH	−0.3 to VCC + 0.3	V
Analog power supply voltage		AVCC*2	−0.3 to +4.6	V
Analog input voltage		V _{AN}	−0.3 to VCC + 0.3	V
Operating temperature	D version	T _{opr}	−40 to +85	°C
	G version		−40 to +105	°C
Storage temperature		T _{stg}	−55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 07, 12 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 2. Connect AVCC0 to VCC. When neither the A/D converter nor the D/A converter is in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V _{RAM}	2.7	—	—	V	
VCC rising gradient	SrVCC	8.4	—	20000	μs/V	
VCC falling gradient*8	SfVCC	8.4	—	—	μs/V	

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.

Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK:PCLK:BCLK:BCLK pin = 8:4:4:2)

I_{CC} Max. = 0.87 × f + 13 (max. operation in high-speed operating mode)

I_{CC} Typ. = 0.35 × f + 5 (normal operation in high-speed operating mode)

I_{CC} Typ. = 1.0 × f + 3 (low-speed operating mode 1)

I_{CC} Max. = 0.53 × f + 12 (sleep mode)

Note 4. This does not include the BGO operation.

Note 5. This is the increase for programming or erasure of the ROM or flash memory for data storage during program execution.

Note 6. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Note 7. The reference power supply current is included in the power supply current value for 10-bit A/D conversion and D/A conversion.

Note 8. When V_{BATT} is used

Note 9. The current values for 10-bit A/D converter and 10-bit D/A converter are included in the current from the VREFH pin.

Note 10. The values are the sum of I_{AVCC0} and I_{VREFH}.

5.3 AC Characteristics

Table 5.8 Operation Frequency Value (High-Speed Operating Mode)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operation frequency	System clock (ICLK)		f	—*1	—	100	MHz
	Peripheral module clock (PCLKA)			—*1	—	100	
	Peripheral module clock (PCLKB)			—*2	—	50	
	FlashIF clock (FCLK)			—*3	—	50	
	External bus clock (BCLK)	Packages with 177 to 144 pins		—	—	100	
		Packages with 100 pins or less		—	—	50	
	BCLK pin output	Packages with 177 to 144 pins		—	—	50	
		Packages with 100 pins or less		—	—	25	
	SDRAM clock (SDCLK)	Packages with 177 to 144 pins only		—	—	50	
	SDCLK pin output	Packages with 177 to 144 pins only		—	—	50	
	USB clock (UCLK)			—	—	48	
IEBUS clock (IECLK)		—	—	44.03			

Note 1. The ICLK and PCLKA frequencies must be the same and at least 12.5 MHz if the Ethernet controller is in use

Note 2. The PCLKB must run at a frequency of at least 24 MHz if the USB is in use.

Note 3. The FCLK must run at a frequency of at least 4 MHz when changing the ROM or E2 DataFlash memory contents.

Table 5.9 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operation frequency	System clock (ICLK)		f	—	—	1	MHz
	Peripheral module clock (PCLKA)			—	—	1	
	Peripheral module clock (PCLKB)			—	—	1	
	FlashIF clock (FCLK)			—	—	1	
	External bus clock (BCLK)	Packages with 177 to 144 pins		—	—	1	
		Packages with 100 pins or less		—	—	1	
	BCLK pin output	Packages with 177 to 144 pins		—	—	1	
		Packages with 100 pins or less		—	—	1	
	SDRAM clock (SDCLK)	Packages with 177 to 144 pins only		—	—	1	
	SDCLK pin output	Packages with 177 to 144 pins only		—	—	1	
	USB clock (UCLK)			—	—	1	
	IEBUS clock (IECLK)			—	—	1	

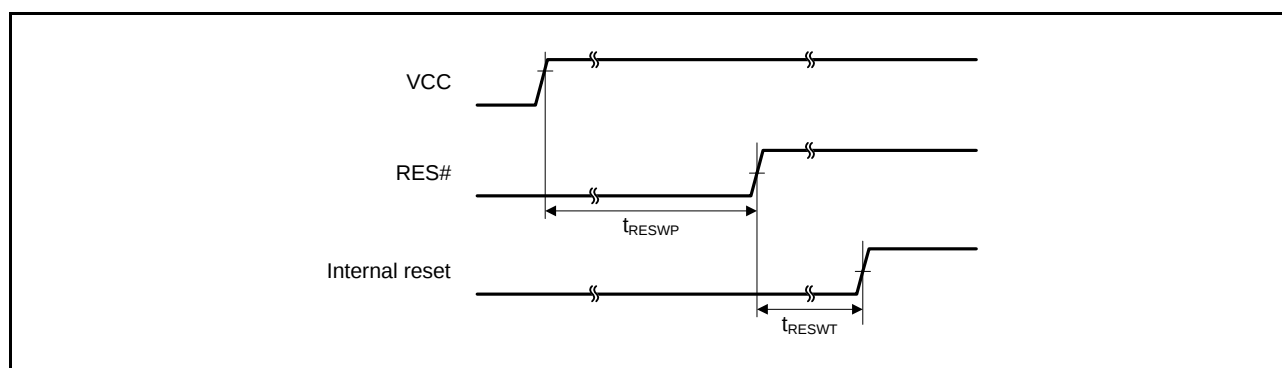


Figure 5.1 Reset Input Timing at Power-On

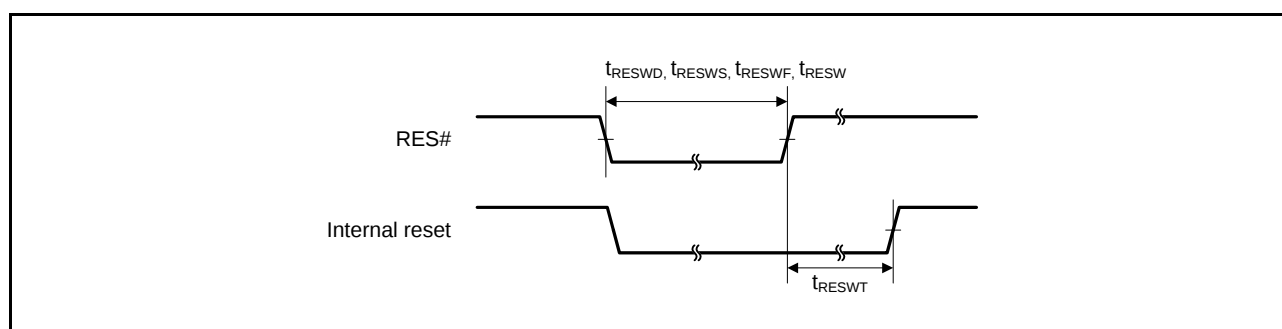
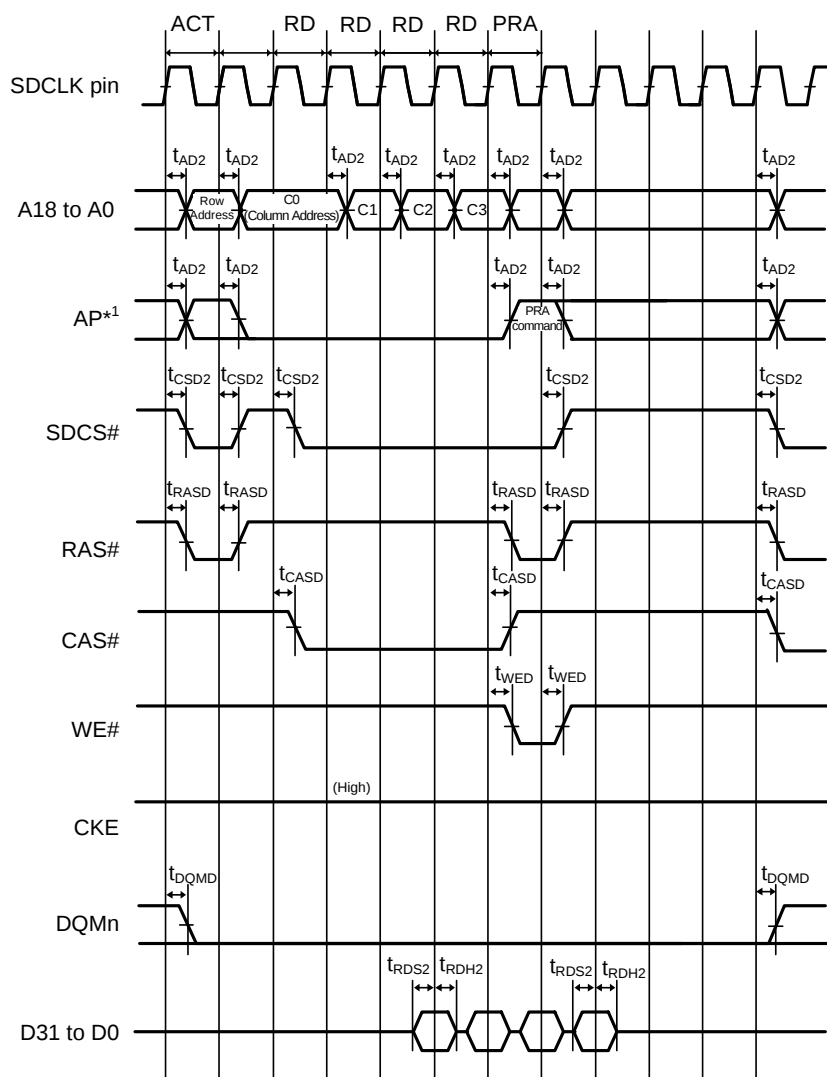
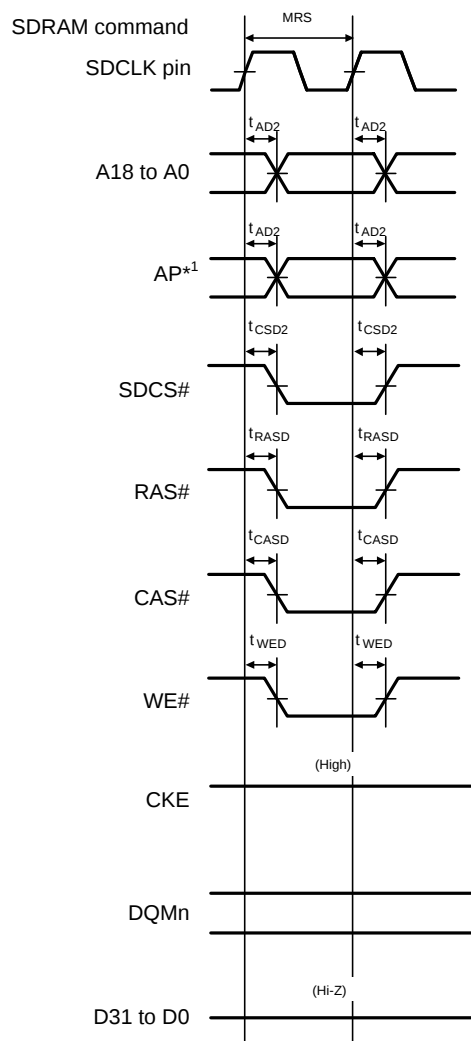


Figure 5.2 Reset Input Timing



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.26 SDRAM Space Multiple Read Bus Timing



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.29 SDRAM Space Mode Register Set Bus Timing

Table 5.21 Timing of On-Chip Peripheral Modules (3)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V*1, $VREFH0 = 2.7$ V to $AVCC0$ *1,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V,
 $PCLK = 8$ to 50 MHz,
 $T_a = T_{opr}$
 High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit*2	Test Conditions
RSPI	Data output delay time	Master	Packages with 177 to 144 pins	t_{OD}	—	18	ns	Figure 5.43 to Figure 5.46 C = 30pF
			Packages with 100 pins or less		—	30		
		Slave	Packages with 177 to 144 pins		—	$3 \times t_{Pcyc} + 40$		
			Packages with 100 pins or less		—	$3 \times t_{Pcyc} + 50$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	Packages with 177 to 144 pins	t_{Dr}, t_{Df}	—	5	ns	
			Packages with 100 pins or less		—	10		
		Input			—	1	μs	
	SSL rise/fall time	Output	Packages with 177 to 144 pins	t_{SSLr}, t_{SSLf}	—	5	ns	
			Packages with 100 pins or less		—	10		
		Input			—	1	μs	
Slave access time				t_{SA}	—	4	t_{Pcyc}	Figure 5.45 and Figure 5.46 C = 30pF
Slave output release time				t_{REL}	—	3	t_{Pcyc}	

Note 1. When operation at 3.0 V or a lower voltage is needed, please contact a Renesas sales office.

Note 2. t_{Pcyc} : PCLK cycle