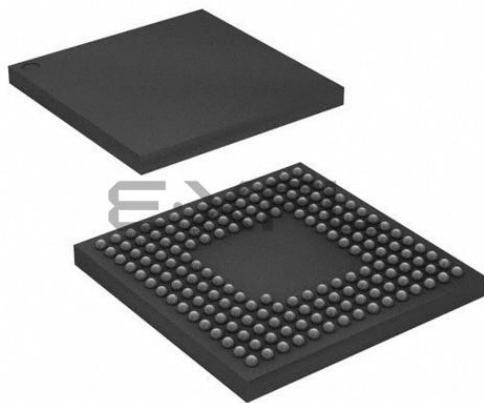




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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	177-TFLGA
Supplier Device Package	177-TFLGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631dddlc-u0

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX63N (D version)	R5F563NECDLC	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDLC	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDLC	PTLG0177KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDL	PTLG0177KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDLC	PTLG0177KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDL	PTLG0177KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDLC	PTLG0177KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDLC	PTLG0177KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDBG	PLBG0176GA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDBG	PLBG0176GA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDBG	PLBG0176GA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDBG	PLBG0176GA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDBG	PLBG0176GA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDBG	PLBG0176GA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDBG	PLBG0176GA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDBG	PLBG0176GA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFHDFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFDDFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKHDFC	PLQP0176KB-A*1	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKDDFC	PLQP0176KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDFC	PLQP0176KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDFC	PLQP0176KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJHDFC	PLQP0176KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJDDFC	PLQP0176KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGHDFC	PLQP0176KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGDDFC	PLQP0176KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDFC	PLQP0176KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDFC	PLQP0176KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYHDFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYDDFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWHDFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWDDFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWGDFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWCDFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDFC	PLQP0176KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDFC	PLQP0176KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDFC	PLQP0176KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDFC	PLQP0176KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDLK	PTLG0145KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDLK	PTLG0145KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

Table 1.3 List of Products (8/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX631 (G version) *2	R5F5631GDGFB	PLQP0144KA-A	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631DDGFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631YDGFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631WDGFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631BDGFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631ADGFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56318SGFB	PLQP0144KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56318DGFB	PLQP0144KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56317SGFB	PLQP0144KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56317DGFB	PLQP0144KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56316SGFB	PLQP0144KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56316DGFB	PLQP0144KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631FDGFP	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631KDGFP	PLQP0100KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631EDGFP	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631JDGFP	PLQP0100KB-A	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631GDGFP	PLQP0100KB-A	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631DDGFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631YDGFP	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631WDGFP	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631BDGFP	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631ADGFP	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56318DGFP	PLQP0100KB-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56317DGFP	PLQP0100KB-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56316DGFP	PLQP0100KB-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631PDGFM	PLQP0064KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631NDGFM	PLQP0064KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631MDGFM	PLQP0064KB-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631PDGFL	PLQP0048KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631NDGFL	PLQP0048KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631MDGFL	PLQP0048KB-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C

Note 1. In the planning stage

Note 2. The specifications of the temperature sensor calibration and unique ID for G-version products differ from those for other products. For details, see section 45.2.2, Temperature Sensor Calibration Data Registers (TSCDRH, TSCDRL), section 45.3, Using the Temperature Sensor, and section 47.2.22, Unique ID Registers n (UIDRn) (n = 0 to 15) in the User's manual: Hardware.

Table 1.4 Pin Functions (4/6)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCId)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for clock signals.
	RXD12	Input	Input pin for data reception.
	TXD12	Output	Output pin for data transmission.
	CTS12#	Input	Transmit/receive start control input pins
	RTS12#	Output	Transmit/receive start control output pins
	• Simple I ² C mode		
	SSCL12	I/O	Input/output pins for the I ² C clock
	SSDA12	I/O	Input/output pins for the I ² C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pins for the clock
	SMISO12	I/O	Input/output pins for slave transmit data.
	SMOSI12	I/O	Input/output pins for master transmit data.
	SS12#	Input	Input pins for chip select signals
	• Extended serial mode		
	RXDX12	Input	Input pin for receive data
	TXDX12	Output	Output pin for transmit data
	SIOX12	I/O	Input/output pin for Transmit/receive data
I ² C bus interface	SCL0[FM+], SCL1 to SCL3	I/O	Input/output pin for clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0[FM+], SDA1 to SDA3	I/O	Input/output pin for data. Bus can be directly driven by the N-channel open drain output.
Ethernet controller	REF50CK	Input	50-MHz reference clock. This pin inputs reference signals for transmission/reception timings in RMII mode.
	RMII_CRS_DV	Input	Indicates that there are carrier detection signals and valid receive data on RMII_RXD1 and RMII_RXD0 in RMII mode.
	RMII_TXD0, RMII_TXD1	Output	2-bit transmit data in RMII mode.
	RMII_RXD0, RMII_RXD1	Input	2-bit receive data in RMII mode.
	RMII_TXD_EN	Output	Output pin for data transmit enable signals in RMII mode.
	RMII_RX_ER	Input	Indicates an error has occurred during reception of data in RMII mode.
	ET_CRS	Input	Carrier detection/data reception enable pin.
	ET_RX_DV	Input	Indicates that there are valid receive data on ET_ERXD3 to ET_ERXD0.
	ET_EXOUT	Output	General-purpose external output pin.
	ET_LINKSTA	Input	Inputs link status from the PHY-LSI.
	ET_ETXD0 to ET_ETXD3	Output	4 bits of MII transmit data.
	ET_ERXD0 to ET_ERXD3	Input	4 bits of MII receive data.
	ET_TX_EN	Output	Transmit enable pin. Indicates that transmit data is ready on ET_ETXD3 to ET_ETXD0.
	ET_TX_ER	Output	Transmit error pin. Notifies the PHY_LSI of an error during transmission.
	ET_RX_ER	Input	Receive error pin. Recognizes an error during reception.
	ET_TX_CLK	Input	Transmit clock pin. This pin inputs reference signals for output timings from ET_TX_EN, ET_ETXD3 to ET_ETXD0, and ET_TX_ER.
	ET_RX_CLK	Input	Receive clock pin. This pin inputs reference signals for input timings to ET_RX_DV, ET_ERXD3 to ET_ERXD0, and ET_RX_ER.
	ET_COL	Input	Inputs collision detection signals.
	ET_WOL	Output	Receives Magic packets.
	ET_MDC	Output	Outputs reference clock signals for information transfer via ET_MDIO.

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	PE3	PE4	VSS	PE6	P67	PA2	PA4	PA7	PB1	PB5	VSS	VCC	P74	13
12	PE1	PE2	P70	PE5	P65	PA1	VCC	PB0	PB2	PB6	P73	PC1	P75	12
11	P62	P61	PE0	VCC	P66	VSS	PA6	P71	PB4	PB7	PC2	PC0	PC3	11
10	VSS	VCC	P63	PE7	PA0	PA3	PA5	P72	PB3	P76	PC4	P77	P82	10
9	PD6	PD4	PD7	P64	RX63N Group RX631 Group PTLG0145KA-A (145-pin TFLGA) (Top perspective view)					P80	PC5	P81	PC7	9
8	PD2	PD0	PD3	P60						VCC	P83	PC6	VSS	8
7	P92	P91	PD1	PD5						P51	P52	P50	P55	7
6	P90	P47	VSS	P93						P53	P56	VSS_ USB	USB0_ DP	6
5	P45	P43	P46	VCC	P44					P54	P13	VCC_ USB	USB0_ DM	5
4	P42	VREFL0	P41	P01	EMLE	VBATT	BSCANP	P35	P30	P15	P24	P12	P14	4
3	P40	P05	VREFH0	P03	PJ5	PJ3	MD/ FINED	VSS	P32	P31	P16	P86	P87	3
2	P07	AVCC0	P02	PF5	VCL	XCOUT	RES#	VCC	P33	P26	P23	P17	P20	2
1	AVSS0	VREFH	VREFL	P00	VSS	XCIN	XTAL	EXTAL	P34	P27	P25	P22	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pins and Pin Functions (145-Pin TFLGA).

Figure 1.6 Pin Assignment (145-Pin TFLGA)

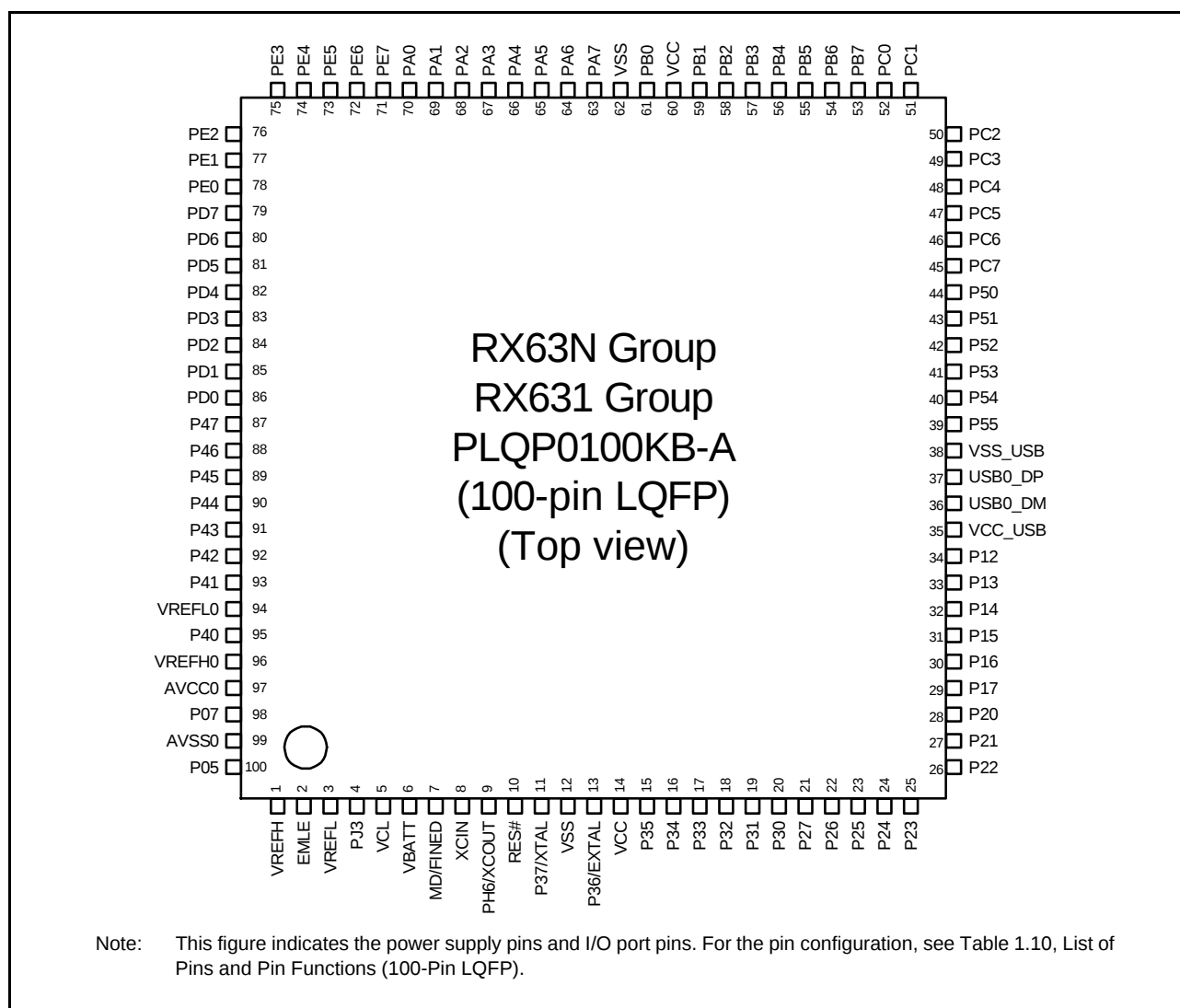
**Figure 1.9 Pin Assignment (100-Pin LQFP)**

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (5/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
N7	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET_EXOUT	IRQ10	
N8	VSS						
N9		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA/ET_COL	IRQ14	
N10	TRSYNC	P82	EDREQ1	MTIOC4A/PO28	TXD10/SMOSI10/SSDA10/ ET_ETXD1/RMII_TXD1		
N11		PC3	A19	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ IETXD/ET_TX_ER		
N12		P75	CS5#	PO20	SCK11/ET_ERXD0/ RMII_RXD0		
N13		P74	CS4#	PO19	CTS11#/RTS11#/SS11#/ ET_ERXD1/RMII_RXD1		

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 4.1 List of I/O Registers (Address Order) (4/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 3072h	BSC	CS7 mode register	CS7MOD	16	16	1, 2 BCLK		Buses
0008 3074h	BSC	CS7 wait control register 1	CS7WCR1	32	32	1, 2 BCLK		
0008 3078h	BSC	CS7 wait control register 2	CS7WCR2	32	32	1, 2 BCLK		
0008 3802h	BSC	CS0 control register	CS0CR	16	16	1, 2 BCLK		
0008 380Ah	BSC	CS0 recovery cycle register	CS0REC	16	16	1, 2 BCLK		
0008 3812h	BSC	CS1 control register	CS1CR	16	16	1, 2 BCLK		
0008 381Ah	BSC	CS1 recovery cycle register	CS1REC	16	16	1, 2 BCLK		
0008 3822h	BSC	CS2 control register	CS2CR	16	16	1, 2 BCLK		
0008 382Ah	BSC	CS2 recovery cycle register	CS2REC	16	16	1, 2 BCLK		
0008 3832h	BSC	CS3 control register	CS3CR	16	16	1, 2 BCLK		
0008 383Ah	BSC	CS3 recovery cycle register	CS3REC	16	16	1, 2 BCLK		
0008 3842h	BSC	CS4 control register	CS4CR	16	16	1, 2 BCLK		
0008 384Ah	BSC	CS4 recovery cycle register	CS4REC	16	16	1, 2 BCLK		
0008 3852h	BSC	CS5 control register	CS5CR	16	16	1, 2 BCLK		
0008 385Ah	BSC	CS5 recovery cycle register	CS5REC	16	16	1, 2 BCLK		
0008 3862h	BSC	CS6 control register	CS6CR	16	16	1, 2 BCLK		
0008 386Ah	BSC	CS6 recovery cycle register	CS6REC	16	16	1, 2 BCLK		
0008 3872h	BSC	CS7 control register	CS7CR	16	16	1, 2 BCLK		
0008 387Ah	BSC	CS7 recovery cycle register	CS7REC	16	16	1, 2 BCLK		
0008 3880h	BSC	CS recovery cycle insertion enable register	CSRECEN	16	16	1, 2 BCLK		
0008 3C00h	BSC	SDC control register	SDCCR	8	8	1, 2 BCLK		
0008 3C01h	BSC	SDC mode register	SDCMOD	8	8	1, 2 BCLK		
0008 3C02h	BSC	SDRAM access mode register	SDAMOD	8	8	1, 2 BCLK		
0008 3C10h	BSC	SDRAM self-refresh control register	SDSELF	8	8	1, 2 BCLK		
0008 3C14h	BSC	SDRAM refresh control register	SDRFCR	16	16	1, 2 BCLK		
0008 3C16h	BSC	SDRAM auto-refresh control register	SDRFEN	8	8	1, 2 BCLK		
0008 3C20h	BSC	SDRAM initialization sequence control register	SDICR	8	8	1, 2 BCLK		
0008 3C24h	BSC	SDRAM initialization register	SDIR	16	16	1, 2 BCLK		
0008 3C40h	BSC	SDRAM address register	SDADR	8	8	1, 2 BCLK		
0008 3C44h	BSC	SDRAM timing register	SDTR	32	32	1, 2 BCLK		
0008 3C48h	BSC	SDRAM mode register	SDMOD	16	16	1, 2 BCLK		
0008 3C50h	BSC	SDRAM status register	SDSR	8	8	1, 2 BCLK		
0008 6400h	MPU	Region-0 start page number register	RSPAGE0	32	32	1 ICLK		MPU
0008 6404h	MPU	Region-0 end page number register	REPAGE0	32	32	1 ICLK		
0008 6408h	MPU	Region-1 start page number register	RSPAGE1	32	32	1 ICLK		
0008 640Ch	MPU	Region-1 end page number register	REPAGE1	32	32	1 ICLK		
0008 6410h	MPU	Region-2 start page number register	RSPAGE2	32	32	1 ICLK		
0008 6414h	MPU	Region-2 end page number register	REPAGE2	32	32	1 ICLK		
0008 6418h	MPU	Region-3 start page number register	RSPAGE3	32	32	1 ICLK		
0008 641Ch	MPU	Region-3 end page number register	REPAGE3	32	32	1 ICLK		
0008 6420h	MPU	Region-4 start page number register	RSPAGE4	32	32	1 ICLK		
0008 6424h	MPU	Region-4 end page number register	REPAGE4	32	32	1 ICLK		
0008 6428h	MPU	Region-5 start page number register	RSPAGE5	32	32	1 ICLK		
0008 642Ch	MPU	Region-5 end page number register	REPAGE5	32	32	1 ICLK		
0008 6430h	MPU	Region-6 start page number register	RSPAGE6	32	32	1 ICLK		
0008 6434h	MPU	Region-6 end page number register	REPAGE6	32	32	1 ICLK		
0008 6438h	MPU	Region-7 start page number register	RSPAGE7	32	32	1 ICLK		
0008 643Ch	MPU	Region-7 end page number register	REPAGE7	32	32	1 ICLK		
0008 6500h	MPU	Memory-protection enable register	MPEN	32	32	1 ICLK		
0008 6504h	MPU	Background access control register	MPBAC	32	32	1 ICLK		
0008 6508h	MPU	Memory-protection error status-clearing register	MPECLR	32	32	1 ICLK		

Table 4.1 List of I/O Registers (Address Order) (7/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7096h	ICU	Interrupt request register 150	IR150	8	8	2	ICLK	ICUb
0008 7097h	ICU	Interrupt request register 151	IR151	8	8	2	ICLK	
0008 7098h	ICU	Interrupt request register 152	IR152	8	8	2	ICLK	
0008 7099h	ICU	Interrupt request register 153	IR153	8	8	2	ICLK	
0008 709Ah	ICU	Interrupt request register 154	IR154	8	8	2	ICLK	
0008 709Bh	ICU	Interrupt request register 155	IR155	8	8	2	ICLK	
0008 709Ch	ICU	Interrupt request register 156	IR156	8	8	2	ICLK	
0008 709Dh	ICU	Interrupt request register 157	IR157	8	8	2	ICLK	
0008 709Eh	ICU	Interrupt request register 158	IR158	8	8	2	ICLK	
0008 709Fh	ICU	Interrupt request register 159	IR159	8	8	2	ICLK	
0008 70A0h	ICU	Interrupt request register 160	IR160	8	8	2	ICLK	
0008 70A1h	ICU	Interrupt request register 161	IR161	8	8	2	ICLK	
0008 70A2h	ICU	Interrupt request register 162	IR162	8	8	2	ICLK	
0008 70A3h	ICU	Interrupt request register 163	IR163	8	8	2	ICLK	
0008 70A4h	ICU	Interrupt request register 164	IR164	8	8	2	ICLK	
0008 70A5h	ICU	Interrupt request register 165	IR165	8	8	2	ICLK	
0008 70A6h	ICU	Interrupt request register 166	IR166	8	8	2	ICLK	
0008 70A7h	ICU	Interrupt request register 167	IR167	8	8	2	ICLK	
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8	2	ICLK	
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2	ICLK	
0008 70ACh	ICU	Interrupt request register 172	IR172	8	8	2	ICLK	
0008 70ADh	ICU	Interrupt request register 173	IR173	8	8	2	ICLK	
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8	2	ICLK	
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8	2	ICLK	
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8	2	ICLK	
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8	2	ICLK	
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8	2	ICLK	
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8	2	ICLK	
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8	2	ICLK	
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8	2	ICLK	
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8	2	ICLK	
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8	2	ICLK	
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8	2	ICLK	
0008 70B9h	ICU	Interrupt request register 185	IR185	8	8	2	ICLK	
0008 70BAh	ICU	Interrupt request register 186	IR186	8	8	2	ICLK	
0008 70BBh	ICU	Interrupt request register 187	IR187	8	8	2	ICLK	
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8	2	ICLK	
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8	2	ICLK	
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8	2	ICLK	
0008 70BFh	ICU	Interrupt request register 191	IR191	8	8	2	ICLK	
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8	2	ICLK	
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8	2	ICLK	
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2	ICLK	
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2	ICLK	
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2	ICLK	
0008 70C5h	ICU	Interrupt request register 197	IR197	8	8	2	ICLK	
0008 70C6h	ICU	Interrupt request register 198	IR198	8	8	2	ICLK	
0008 70C7h	ICU	Interrupt request register 199	IR199	8	8	2	ICLK	
0008 70C8h	ICU	Interrupt request register 200	IR200	8	8	2	ICLK	
0008 70C9h	ICU	Interrupt request register 201	IR201	8	8	2	ICLK	
0008 70CAh	ICU	Interrupt request register 202	IR202	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (9/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7128h	ICU	DTC activation enable register 040	DTCE040	8	8	2	ICLK	ICUb
0008 712Ah	ICU	DTC activation enable register 042	DTCE042	8	8	2	ICLK	
0008 712Bh	ICU	DTC activation enable register 043	DTCE043	8	8	2	ICLK	
0008 712Dh	ICU	DTC activation enable register 045	DTCE045	8	8	2	ICLK	
0008 712Eh	ICU	DTC activation enable register 046	DTCE046	8	8	2	ICLK	
0008 7140h	ICU	DTC activation enable register 064	DTCE064	8	8	2	ICLK	
0008 7141h	ICU	DTC activation enable register 065	DTCE065	8	8	2	ICLK	
0008 7142h	ICU	DTC activation enable register 066	DTCE066	8	8	2	ICLK	
0008 7143h	ICU	DTC activation enable register 067	DTCE067	8	8	2	ICLK	
0008 7144h	ICU	DTC activation enable register 068	DTCE068	8	8	2	ICLK	
0008 7145h	ICU	DTC activation enable register 069	DTCE069	8	8	2	ICLK	
0008 7146h	ICU	DTC activation enable register 070	DTCE070	8	8	2	ICLK	
0008 7147h	ICU	DTC activation enable register 071	DTCE071	8	8	2	ICLK	
0008 7148h	ICU	DTC activation enable register 072	DTCE072	8	8	2	ICLK	
0008 7149h	ICU	DTC activation enable register 073	DTCE073	8	8	2	ICLK	
0008 714Ah	ICU	DTC activation enable register 074	DTCE074	8	8	2	ICLK	
0008 714Bh	ICU	DTC activation enable register 075	DTCE075	8	8	2	ICLK	
0008 714Ch	ICU	DTC activation enable register 076	DTCE076	8	8	2	ICLK	
0008 714Dh	ICU	DTC activation enable register 077	DTCE077	8	8	2	ICLK	
0008 714Eh	ICU	DTC activation enable register 078	DTCE078	8	8	2	ICLK	
0008 714Fh	ICU	DTC activation enable register 079	DTCE079	8	8	2	ICLK	
0008 7162h	ICU	DTC activation enable register 098	DTCE098	8	8	2	ICLK	
0008 7166h	ICU	DTC activation enable register 102	DTCE102	8	8	2	ICLK	
0008 717Eh	ICU	DTC activation enable register 126	DTCE126	8	8	2	ICLK	
0008 717Fh	ICU	DTC activation enable register 127	DTCE127	8	8	2	ICLK	
0008 7180h	ICU	DTC activation enable register 128	DTCE128	8	8	2	ICLK	
0008 7181h	ICU	DTC activation enable register 129	DTCE129	8	8	2	ICLK	
0008 7182h	ICU	DTC activation enable register 130	DTCE130	8	8	2	ICLK	
0008 7183h	ICU	DTC activation enable register 131	DTCE131	8	8	2	ICLK	
0008 7184h	ICU	DTC activation enable register 132	DTCE132	8	8	2	ICLK	
0008 7185h	ICU	DTC activation enable register 133	DTCE133	8	8	2	ICLK	
0008 7186h	ICU	DTC activation enable register 134	DTCE134	8	8	2	ICLK	
0008 7187h	ICU	DTC activation enable register 135	DTCE135	8	8	2	ICLK	
0008 7188h	ICU	DTC activation enable register 136	DTCE136	8	8	2	ICLK	
0008 7189h	ICU	DTC activation enable register 137	DTCE137	8	8	2	ICLK	
0008 718Ah	ICU	DTC activation enable register 138	DTCE138	8	8	2	ICLK	
0008 718Bh	ICU	DTC activation enable register 139	DTCE139	8	8	2	ICLK	
0008 718Ch	ICU	DTC activation enable register 140	DTCE140	8	8	2	ICLK	
0008 718Dh	ICU	DTC activation enable register 141	DTCE141	8	8	2	ICLK	
0008 718Eh	ICU	DTC activation enable register 142	DTCE142	8	8	2	ICLK	
0008 718Fh	ICU	DTC activation enable register 143	DTCE143	8	8	2	ICLK	
0008 7190h	ICU	DTC activation enable register 144	DTCE144	8	8	2	ICLK	
0008 7191h	ICU	DTC activation enable register 145	DTCE145	8	8	2	ICLK	
0008 7194h	ICU	DTC activation enable register 148	DTCE148	8	8	2	ICLK	
0008 7195h	ICU	DTC activation enable register 149	DTCE149	8	8	2	ICLK	
0008 7196h	ICU	DTC activation enable register 150	DTCE150	8	8	2	ICLK	
0008 7197h	ICU	DTC activation enable register 151	DTCE151	8	8	2	ICLK	
0008 7198h	ICU	DTC activation enable register 152	DTCE152	8	8	2	ICLK	
0008 7199h	ICU	DTC activation enable register 153	DTCE153	8	8	2	ICLK	
0008 719Ah	ICU	DTC activation enable register 154	DTCE154	8	8	2	ICLK	
0008 719Bh	ICU	DTC activation enable register 155	DTCE155	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (15/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 8036h	IWDT	IWDT reset control register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK	IWDTa
0008 8038h	IWDT	IWDT count stop control register	IWDTCSTPR	8	8	2, 3 PCLKB	2 ICLK	
0008 80C0h	DA	D/A data register 0	DADR0	16	16	2, 3 PCLKB	2 ICLK	DAa
0008 80C2h	DA	D/A data register 1	DADR1	16	16	2, 3 PCLKB	2 ICLK	
0008 80C4h	DA	D/A control register	DACR	8	8	2, 3 PCLKB	2 ICLK	
0008 80C5h	DA	DADRM format select register	DADPR	8	8	2, 3 PCLKB	2 ICLK	
0008 80C6h	DA	D/A A/D synchronous start control register	DAADSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8100h	TPUA	Timer start register	TSTR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8101h	TPUA	Timer synchronous register	TSYR	8	8	2, 3 PCLKB	2 ICLK	
0008 8108h	TPU0	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8109h	TPU1	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 810Ah	TPU2	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 810Bh	TPU3	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 810Ch	TPU4	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 810Dh	TPU5	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8110h	TPU0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8111h	TPU0	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8112h	TPU0	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8113h	TPU0	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8114h	TPU0	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8115h	TPU0	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8116h	TPU0	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8118h	TPU0	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 811Ah	TPU0	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 811Ch	TPU0	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 811Eh	TPU0	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 8120h	TPU1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8121h	TPU1	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8122h	TPU1	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8124h	TPU1	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8125h	TPU1	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8126h	TPU1	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8128h	TPU1	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 812Ah	TPU1	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8130h	TPU2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8131h	TPU2	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8132h	TPU2	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8134h	TPU2	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8135h	TPU2	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8136h	TPU2	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8138h	TPU2	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 813Ah	TPU2	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8140h	TPU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8141h	TPU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8142h	TPU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8143h	TPU3	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8144h	TPU3	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8145h	TPU3	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8146h	TPU3	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8148h	TPU3	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 814Ah	TPU3	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (37/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0009 1428h	CAN1	Mask invalid register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 142Ch	CAN1	Mailbox interrupt enable register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1820h to 0009 183Fh	CAN1	Message control registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	
0009 1840h	CAN1	Control register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 1842h	CAN1	Status register	STR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 1844h	CAN1	Bit configuration register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1848h	CAN1	Receive FIFO control register	RFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 1849h	CAN1	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 184Ah	CAN1	Transmit FIFO control register	TFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 184Bh	CAN1	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 184Ch	CAN1	Error interrupt enable register	EIER	8	8	2, 3 PCLKB	2 ICLK	
0009 184Dh	CAN1	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLKB	2 ICLK	
0009 184Eh	CAN1	Receive error count register	RECR	8	8	2, 3 PCLKB	2 ICLK	
0009 184Fh	CAN1	Transmit error count register	TECR	8	8	2, 3 PCLKB	2 ICLK	
0009 1850h	CAN1	Error code store register	ECSR	8	8	2, 3 PCLKB	2 ICLK	
0009 1851h	CAN1	Channel search support register	CSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 1852h	CAN1	Mailbox search status register	MSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 1853h	CAN1	Mailbox search mode register	MSMR	8	8	2, 3 PCLKB	2 ICLK	
0009 1854h	CAN1	Time stamp register	TSR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 1856h	CAN1	Acceptance filter support register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 1858h	CAN1	Test control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0009 2200h to 0009 23FFh	CAN2	Mailbox registers 0 to 31	MB0 to 31	128	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2400h to 0009 241Fh	CAN2	Mask register 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2420h	CAN2	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2424h	CAN2	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2428h	CAN2	Mask invalid register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 242Ch	CAN2	Mailbox interrupt enable register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2820h to 0009 283Fh	CAN2	Message control registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	
0009 2840h	CAN2	Control register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 2842h	CAN2	Status register	STR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 2844h	CAN2	Bit configuration register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2848h	CAN2	Receive FIFO control register	RFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 2849h	CAN2	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Ah	CAN2	Transmit FIFO control register	TFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Bh	CAN2	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Ch	CAN2	Error interrupt enable register	EIER	8	8	2, 3 PCLKB	2 ICLK	
0009 284Dh	CAN2	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Eh	CAN2	Receive error count register	RECR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Fh	CAN2	Transmit error count register	TECR	8	8	2, 3 PCLKB	2 ICLK	
0009 2850h	CAN2	Error code store register	ECSR	8	8	2, 3 PCLKB	2 ICLK	
0009 2851h	CAN2	Channel search support register	CSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 2852h	CAN2	Mailbox search status register	MSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 2853h	CAN2	Mailbox search mode register	MSMR	8	8	2, 3 PCLKB	2 ICLK	
0009 2854h	CAN2	Time stamp register	TSR	16	16	2, 3 PCLKB	2 ICLK	
0009 2856h	CAN2	Acceptance filter support register	AFSR	16	16	2, 3 PCLKB	2 ICLK	
0009 2858h	CAN2	Test control register	TCR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (50/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
007F C402h	FLASH	Flash mode register	FMODR	8	8	2 to 4 FCLK	2, 3 ICLK	Flash Memory
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2 to 4 FCLK	2, 3 ICLK	
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2 to 4 FCLK	2, 3 ICLK	
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2 to 4 FCLK	2, 3 ICLK	
007F C440h	FLASH	E2 DataFlash read enable register 0	DFLRE0	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C442h	FLASH	E2 DataFlash read enable register 1	DFLRE1	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C450h	FLASH	E2 DataFlash P/E enable register 0	DFLWE0	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C452h	FLASH	E2 DataFlash P/E enable register 1	DFLWE1	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2 to 4 FCLK	2, 3 ICLK	
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2 to 4 FCLK	2, 3 ICLK	
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFCAh	FLASH	E2 data flash blank check control register	DFLBCCNT	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFCEh	FLASH	E2 DataFlash blank check status register	DFLBCSTAT	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2 to 4 FCLK	2, 3 ICLK	
FEFF FAC0h	FLASH	Unique ID register 0*8	UIDR0	8	8	1 ICLK	1 ICLK	
FEFF FAC1h	FLASH	Unique ID register 1*8	UIDR1	8	8	1 ICLK	1 ICLK	
FEFF FAC2h	FLASH	Unique ID register 2*8	UIDR2	8	8	1 ICLK	1 ICLK	
FEFF FAC3h	FLASH	Unique ID register 3*8	UIDR3	8	8	1 ICLK	1 ICLK	
FEFF FAC4h	FLASH	Unique ID register 4*8	UIDR4	8	8	1 ICLK	1 ICLK	
FEFF FAC5h	FLASH	Unique ID register 5*8	UIDR5	8	8	1 ICLK	1 ICLK	
FEFF FAC6h	FLASH	Unique ID register 6*8	UIDR6	8	8	1 ICLK	1 ICLK	
FEFF FAC7h	FLASH	Unique ID register 7*8	UIDR7	8	8	1 ICLK	1 ICLK	
FEFF FAC8h	FLASH	Unique ID register 8*8	UIDR8	8	8	1 ICLK	1 ICLK	
FEFF FAC9h	FLASH	Unique ID register 9*8	UIDR9	8	8	1 ICLK	1 ICLK	
FEFF FACAh	FLASH	Unique ID register 10*8	UIDR10	8	8	1 ICLK	1 ICLK	
FEFF FACBh	FLASH	Unique ID register 11*8	UIDR11	8	8	1 ICLK	1 ICLK	
FEFF FACCh	FLASH	Unique ID register 12*8	UIDR12	8	8	1 ICLK	1 ICLK	
FEFF FACDh	FLASH	Unique ID register 13*8	UIDR13	8	8	1 ICLK	1 ICLK	
FEFF FACEh	FLASH	Unique ID register 14*8	UIDR14	8	8	1 ICLK	1 ICLK	
FEFF FACFh	FLASH	Unique ID register 15*8	UIDR15	8	8	1 ICLK	1 ICLK	
FEFF FAD2h	TEMPS	Temperature sensor calibration data register*8	TSCDRL	8	8	1 ICLK	1 ICLK	Temperature sensor
FEFF FAD3h	TEMPS	Temperature sensor calibration data register*8	TSCDRH	8	8	1 ICLK	1 ICLK	

- Note 1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 000881EEh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 000881EEh and 000881ECh, respectively.
- Note 2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRH address is 000881EDh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 0 and 1 are 000881EFh and 000881EDh, respectively.
- Note 3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 000881FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 000881FEh and 000881FCh, respectively.
- Note 4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRH address is 000881FDh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 4 and 5 are 000881FFh and 000881FDh, respectively.
- Note 5. Odd addresses should not be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register. Table 27.4 lists register allocation for 16-bit access in the User's manual: Hardware.
- Note 6. When the register is accessed while the USB is operating, a delay may be generated in accessing.
- Note 7. The addresses with odd number cannot be accessed in 16-bit units. 16-bit access to a register should be made to the addresses of the TMOCNL register. Allocation of registers to be accessed in 16-bit units is described in the Table 36.6, Allocation of Registers to be Accessed in 16-bit Units in the User's manual: Hardware.
- Note 8. These registers are only present in the G version.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, VCC_USB	−0.3 to +4.6	V
V _{BATT} power supply voltage		V _{BATT}	−0.3 to +4.6	V
Input voltage (except for ports for 5 V tolerant*1)		V _{in}	−0.3 to VCC + 0.3	V
Input voltage (ports for 5 V tolerant*1)		V _{in}	−0.3 to +5.8	V
Reference power supply voltage		VREFH	−0.3 to VCC + 0.3	V
Analog power supply voltage		AVCC*2	−0.3 to +4.6	V
Analog input voltage		V _{AN}	−0.3 to VCC + 0.3	V
Operating temperature	D version	T _{opr}	−40 to +85	°C
	G version		−40 to +105	°C
Storage temperature		T _{stg}	−55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 07, 12 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 2. Connect AVCC0 to VCC. When neither the A/D converter nor the D/A converter is in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1	V_{IH}	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V
	MTU input pin*1	V_{IL}	-0.3	—	$V_{CC} \times 0.2$	
	TMR input pin*1	ΔV_T	$V_{CC} \times 0.06$	—	—	
	SCI input pin*1					
	ADTRG# input pin*1					
	RES#, NMI					
	RIIC input pin (except for SMBus)	V_{IH}	$V_{CC} \times 0.7$	—	5.8	
		V_{IL}	-0.3	—	$V_{CC} \times 0.3$	
		ΔV_T	$V_{CC} \times 0.05$	—	—	
	Ports for 5 V tolerant*2	V_{IH}	$V_{CC} \times 0.8$	—	5.8	
		V_{IL}	-0.3	—	$V_{CC} \times 0.2$	
Input high voltage (except for Schmitt trigger input pin)	Other input pins excluding ports for 5 V tolerant*3	V_{IH}	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V
		V_{IL}	-0.3	—	$V_{CC} \times 0.2$	
		V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	
		V_{IL}	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	
		V_{IH}	2.3	—	$V_{CC} + 0.3$	
		V_{IL}	—	—	$V_{CC} + 0.3$	
		V_{IH}	$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	2.1	—	$V_{CC} + 0.3$	V
	EXTAL, RSPI, EXDMAC, WAIT#, TCK	V_{IL}	—	—	$V_{CC} + 0.3$	
	ETHERC	V_{IL}	—	—	$V_{CC} + 0.3$	
	XCIN	V_{IL}	—	—	$V_{CC} + 0.3$	
	D0 to D31	V_{IL}	—	—	$V_{CC} + 0.3$	
	RIIC (SMBus)	V_{IL}	—	—	$V_{CC} + 0.3$	
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	-0.3	—	$V_{CC} \times 0.1$	V
	EXTAL, RSPI, ETHERC, EXDMAC, WAIT#, TCK	V_{IL}	-0.3	—	$V_{CC} \times 0.2$	
	XCIN	V_{IL}	-0.3	—	—	
	D0 to D31	V_{IL}	-0.3	—	$V_{CC} \times 0.3$	
	RIIC (SMBus)	V_{IL}	-0.3	—	0.8	
		V_{IL}	-0.3	—	0.8	

Note 1. V_{IH} characteristics of the pins which are multiplexed with pin functions having 5-V tolerance are those of the pin functions for 5-V tolerance.

Note 2. Ports 07, 12 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 3. For P32, P31, P30, input as follows when the V_{BATT} power supply is selected.

V_{IH} Min. = $V_{BATT} \times 0.8$, V_{IH} Max. = $V_{BATT} + 0.3$, V_{IL} Min. = -0.3 , V_{IL} Max. = $V_{BATT} \times 0.2$

Table 5.3 DC Characteristics (2)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	V	$I_{OH} = -1$ mA
Output low voltage	All output pins (except for RIIC pins, and ETHERC)	V_{OL}	—	0.5	V	$I_{OL} = 1.0$ mA
	RIIC pins	—	—	0.4	V	$I_{OL} = 3.0$ mA
		—	—	0.6		$I_{OL} = 6.0$ mA
	RIIC pins (only P12 and P13 in channel 0)	V_{OL}	—	0.4	V	$I_{OL} = 15.0$ mA (ICFER.FMPE = 1)
		—	0.4	—		$I_{OL} = 20.0$ mA (ICFER.FMPE = 1)
	ETHERC	V_{OL}	—	0.4	V	$I_{OL} = 1.0$ mA
Input leakage current	RES#, MD pin, EMLE*1, NMI	$ I_{in} $	—	1.0	μ A	$V_{in} = 0$ V $V_{in} = V_{CC}$
Three-state leakage current (off state)	Other than ports for 5 V tolerant	$ I_{TSI} $	—	1.0	μ A	$V_{in} = 0$ V $V_{in} = V_{CC}$
	Ports for 5 V tolerant		—	5.0		$V_{in} = 0$ V $V_{in} = 5.5$ V
Input pull-up MOS current	Ports 0 to 2, 30 to 34, 36, 37, 4 to G, J3, J5	I_p	-10	—	-300	μ A $V_{CC} = 2.7$ to 3.6 V $V_{in} = 0$ V
Input capacitance	All input pins (except for ports 12, 13, 16, 17, 20, 21, 4, C0, C1, and EMLE)	C_{in}	—	—	15	pF $V_{in} = 0$ V $f = 1$ MHz $T_a = 25^\circ\text{C}$
	Ports 12, 13, 16, 17, 20, 21, 4, C0, C1, EMLE		—	—	30	
Input pull-down MOS current	EMLE, BSCANP	I_p	10	—	300	μ A $V_{in} = V_{CC}$

Note 1. The input leakage current value at the EMLE pin is only when $V_{in} = 0$ V.

Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions		
Supply current*1	High-speed operating mode	Max.*2		I _{CC} *3	—	—	100	mA	ICLK = 100 MHz PCLKA = 100MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 100MHz		
		Normal*4	Peripheral function: clock signal supplied*4		—	52	—				
			Peripheral function: clock signal stopped*4		—	40	—				
		Sleep mode			—	25	65				
		All-module-clock-stop mode (reference value)			—	20	38				
		Increased by BGO operation*5			—	15	—				
	Low-speed operating mode 1*6				—	4	—			ICLK = 1 MHz	
	Low-speed operating mode 2				—	1	—				ICLK = 32.768 kHz
	Software standby mode				—	0.2	6				
	Deep software standby mode	Power supplied to RAM and USB resume detecting unit			—	22	200	μA			
		Power not supplied to RAM and USB resume detecting unit	Power-on reset circuit and low-power consumption function disabled		—	21	60				
			Power-on reset circuit and low-power		—	6.2	28				
		Increase when the RTC is operating	When a crystal oscillator for low clock loads is in use		—	1.0	—				
			When a crystal oscillator for standard clock loads is in use		—	3.0	—				
		RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)	When a crystal oscillator for low clock loads is in use		—	0.9	—		V _{BATT} = 2.0 V, VCC = 0V		
	When a crystal oscillator for standard clock loads is in use		—		1.6	—	V _{BATT} = 3.3 V, VCC = 0V				
			—		1.7	—	V _{BATT} = 2.0 V(for products with 100 pins or more), VBATT = 2.3 V (for the 64-pin product), VCC = 0V				
			—		3.3	—	V _{BATT} = 3.3 V, VCC = 0V				
	Analog power supply current*7	During 12-bit A/D conversion (including temperature sensor)			I _{AVCC0}	—	2.3		3.2	mA	
During 10-bit A/D conversion			I _{VREFH} *9	—	1.0	1.65	mA				
During D/A conversion (per unit)				—	0.7	1.0		mA			
Waiting for A/D, D/A conversion (all units)*10			—	—	25	35	μA				
A/D, D/A converter in standby mode (all units)*10				—	0.1	4.0		μA			
Reference power supply current	During 12-bit A/D conversion			I _{VREFH0}	—	0.6	0.7		mA		
	Waiting for 12-bit A/D conversion (per unit)				—	0.5	0.6	mA			
	12-bit A/D converter in standby mode (per unit)				—	0.1	2.0			μA	

- Note 1. This is the time until the clock is used after setting P36 and P37 as inputs, and then clearing the main clock oscillator stop bit (MOSCCR.MOSTP) to 0 (selecting operation).
- Note 2. This is the time until the frequency of oscillation by the HOCO (fHOCO) reaches the range for guaranteed operation after release from the reset state.
- Note 3. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.
- Note 4. The number of cycles n selected by the value of the MOSCWTCR.MSTS[4:0] bits determines the main-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{\text{MAINOSCWT}} = t_{\text{MAINOSC}} + \frac{n + 16384}{f_{\text{MAIN}}}$$

- Note 5. The number of cycles n selected by the value of the PLLWTCR.PSTS[4:0] bits determines the PLL-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{\text{PLLWT1}} = t_{\text{PLL1}} + \frac{n + 131072}{f_{\text{PLL}}}$$

$$t_{\text{PLLWT2}} = t_{\text{PLL2}} + \frac{n + 131072}{f_{\text{PLL}}} = t_{\text{MAINOSC}} + t_{\text{PLL1}} + \frac{n + 131072}{f_{\text{PLL}}}$$

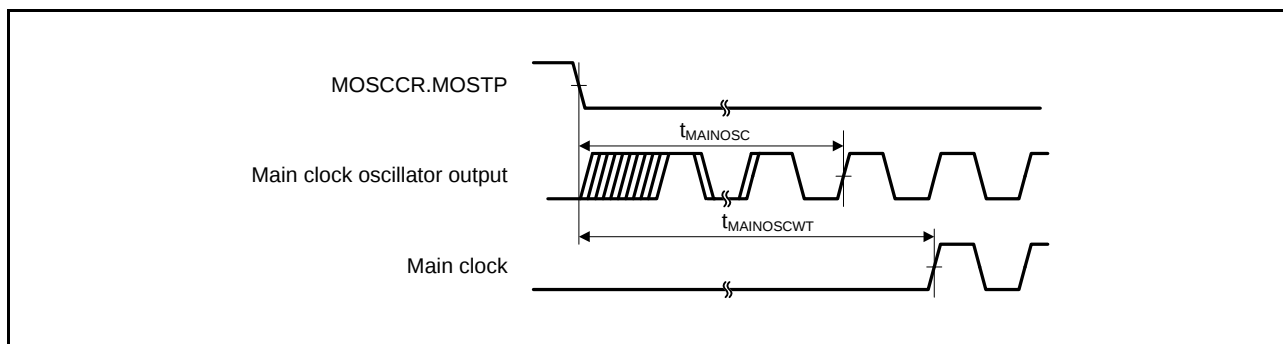


Figure 5.5 Main Clock Oscillation Start Timing

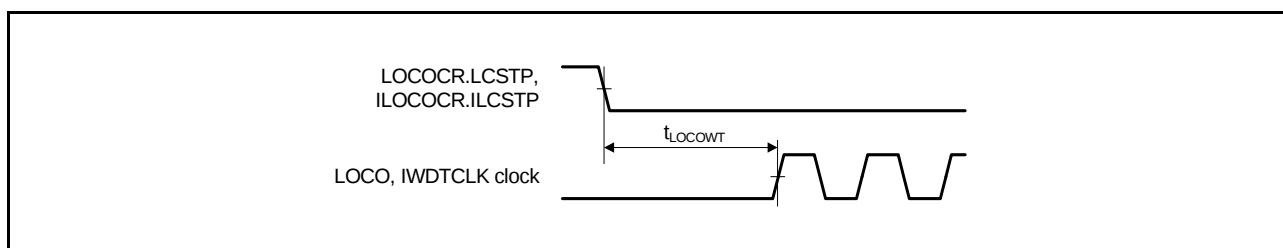


Figure 5.6 LOCO, IWDTCCLK Oscillation Start Timing

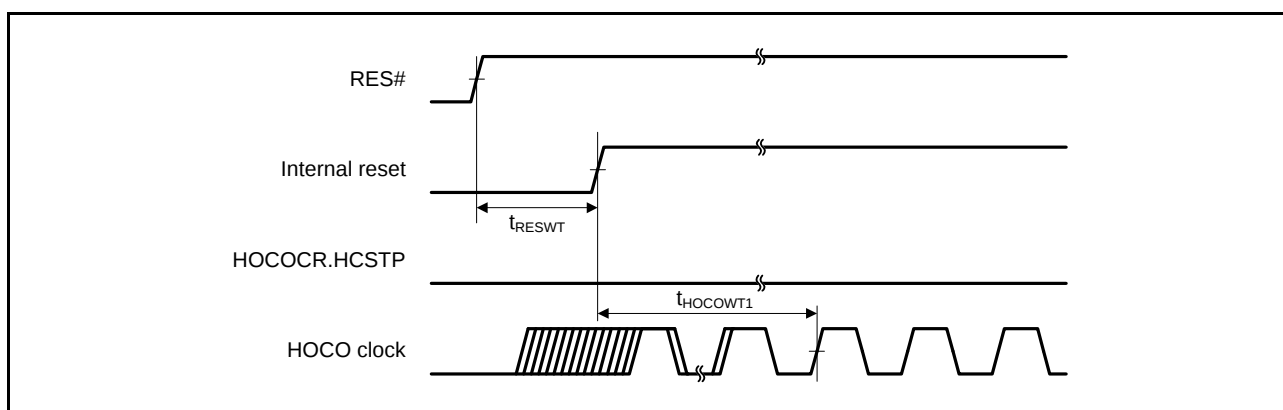


Figure 5.7 HOCO Oscillation Start Timing (After Reset is Canceled by Setting the OFS1.HOCOEN Bit to 0)

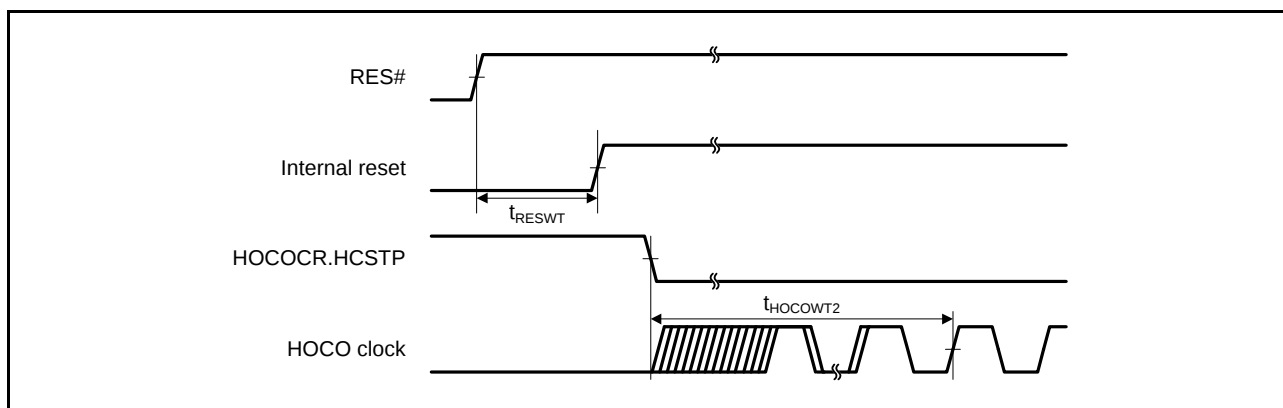


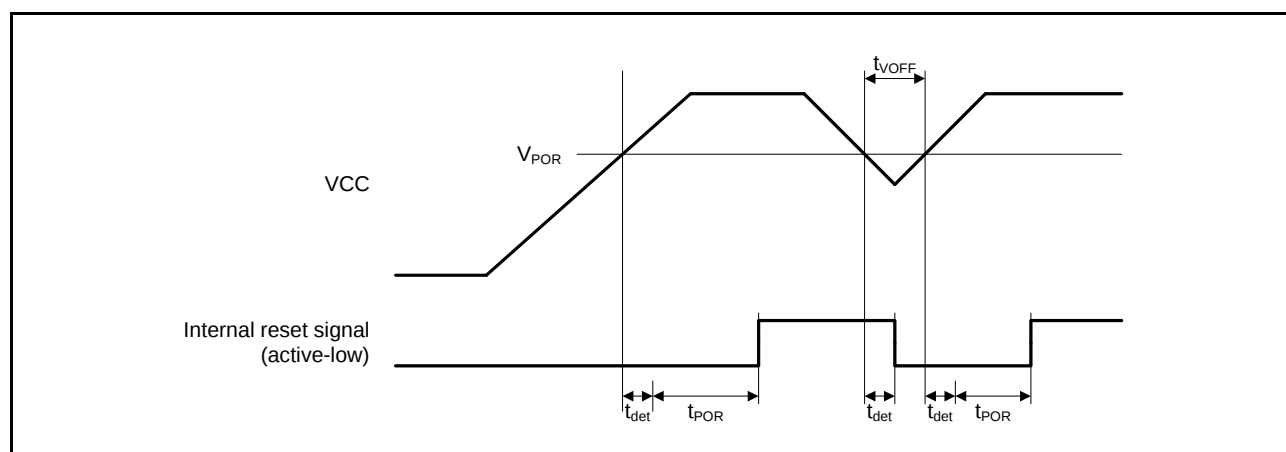
Figure 5.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

5.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.33 Power-on Reset Circuit and Voltage Detection Circuit CharacteristicsConditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled	V _{POR}	2.5	2.6	2.7	V	Figure 5.63
		Low power consumption function enabled		2.0	2.35	2.7		
	Voltage detection circuit (LVD0)		V _{det0}	2.7	2.80	2.9		Figure 5.64
	Voltage detection circuit (LVD1)		V _{det1_A}	2.75	2.95	3.15		Figure 5.65
	Voltage detection circuit (LVD2)		V _{det2_A}	2.75	2.95	3.15		Figure 5.66
Internal reset time	Power-on reset time		t _{POR}	—	4.6	—	ms	Figure 5.63
	LVD0 reset time		t _{LVD0}	—	4.6	—		Figure 5.64
	LVD1 reset time		t _{LVD1}	—	0.9	—		Figure 5.65
	LVD2 reset time		t _{LVD2}	—	0.9	—		Figure 5.66
Minimum VCC down time			t _{VOFF}	200	—	—	μs	Figure 5.63 and Figure 5.64
Response delay time			t _{det}	—	—	200	μs	Figure 5.63 to Figure 5.66
LVD operation stabilization time (after LVD is enabled)			Td _(E-A)	—	—	3	μs	Figure 5.65 and Figure 5.66
Hysteresis width (LVD1 and LVD2)			V _{LVH}	—	80	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det1} , and V_{det2} for the POR/ LVD.

**Figure 5.63 Power-on Reset Timing**

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