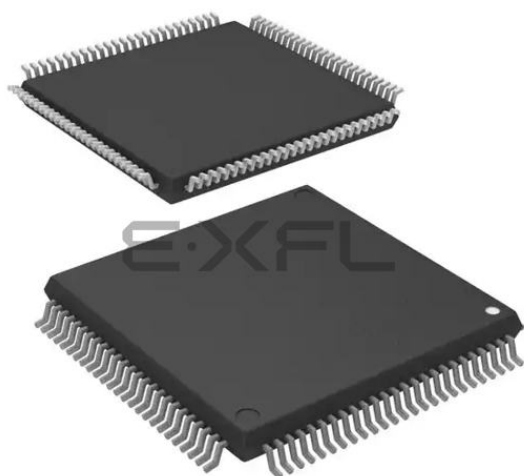




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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631fdgfp-v0

Table 1.3 List of Products (5/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX631 (D version)	R5F5631ADDFC	PLQP0176KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318CDFC	PLQP0176KB-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318DDFC	PLQP0176KB-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317CDFC	PLQP0176KB-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317DDFC	PLQP0176KB-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316CDFC	PLQP0176KB-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316DDFC	PLQP0176KB-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ECDLK	PTLG0145KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631EDDLK	PTLG0145KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631DCDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631DDDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631BCDLK	PTLG0145KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631BDDLK	PTLG0145KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ACDLK	PTLG0145KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ADDLK	PTLG0145KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318CDLK	PTLG0145KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318DDLK	PTLG0145KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317CDLK	PTLG0145KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317DDLK	PTLG0145KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316CDLK	PTLG0145KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316DDLK	PTLG0145KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631FHDFB	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631FDDFB	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631KHDFB	PLQP0144KA-A*1	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631KDDFB	PLQP0144KA-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ECDFB	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631EDDFB	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631JHDFB	PLQP0144KA-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631JDDFB	PLQP0144KA-A	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631GHDFB	PLQP0144KA-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631GDDFB	PLQP0144KA-A	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631DCDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631DDDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631YHDFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631YDDFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631WHDFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631WDDFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631BCDFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631BDDFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ACDFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ADDFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318CDFB	PLQP0144KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318DDFB	PLQP0144KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316CDFB	PLQP0144KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316DDFB	PLQP0144KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

RX631 Group
PTLG0064JA-A (64-pin TFLGA)
(Top perspective view)

	A	B	C	D	E	F	G	H	
8	PE3	PE4	PA0	PA3	PB0	PB3	PB6	PB7	8
7	PE2	PE1	PE5	PA1	VSS	PB5	PC3	PC2	7
6	VREFL	P46	PE0	PA4	VCC	PB1	PC6	USB1_DP	6
5	VREFH	P44	P43	PA6	PC4	P15	VCC_USB	USB1_DM	5
4	VREFL0	P42	P41	P14	P16	PC5	VSS_USB	USB0_DP	4
3	VREFH0	P40	EMLE	P27	P30	P31	VCC_USB	USB0_DM	3
2	AVCC0	AVSS0	MD/FINED	RES#	VBATT	P35	P26	P17	2
1	P05	VCL	XCIN	XCOUT	VSS	VCC	EXTAL	XTAL	1
	A	B	C	D	E	F	G	H	

Figure 1.10 Pin Assignment (64-pin TFLGA)

Note 3. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (3/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
72		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
73	VSS						
74		P83	EDACK1	MTIOC4C	ET_CRS/RMII_CRS_DV/ CTS10#/RTS10#/SS10#		
75	VCC						
76		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	ET_COL/TXD8/SMOSI8/ SSDA8/MISOA	IRQ14	
77		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TIOCA6/TMCI2/PO30	ET_ETXD3/RXD8/ SMISO8/SSCL8/MOSIA	IRQ13	
78		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	ET_ETXD2/SCK8/ RSPCKA		
79		P82	EDREQ1	MTIOC4A/PO28	ET_ETXD1/RMII_TXD1/ TXD10/SMOSI10/SSDA10		
80		P81	EDACK0	MTIOC3D/PO27	ET_ETXD0/RMII_TXD0/ RXD10/SMISO10/SSCL10		
81		P80	EDREQ0	MTIOC3B/PO26	ET_TX_EN/ RMII_TXD_EN/SCK10		
82		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TIOCC6/TCLKE/TMCI1/ PO25/POE0#	ET_TX_CLK/SCK5/ CTS8#/RTS8#/SS8#/ SSLA0		
83		PC3	A19	MTIOC4D/TCLKB/PO24	ET_TX_ER/TXD5/ SMOSI5/SSDA5/IETXD		
84		P77	CS7#	PO23	ET_RX_ER/RMII_RX_ER/ TXD11/SMOSI11/SSDA11		
85		P76	CS6#	PO22	ET_RX_CLK/REF50CK/ RXD11/SMISO11/SSCL11		
86		PC2	A18	MTIOC4B/TCLKA/PO21	ET_RX_DV/RXD5/ SMISO5/SSCL5/SSLA3/ IERXD		
87		P75	CS5#	PO20	ET_ERXD0/RMII_RXD0/ SCK11		
88		P74	CS4#	PO19	ET_ERXD1/RMII_RXD1/ CTS11#/RTS11#/SS11#		
89		PC1	A17	MTIOC3A/TCLKD/PO18	ET_ERXD2/SCK5/SSLA2/ SDA3	IRQ12	
90	VCC						
91		PC0	A16	MTIOC3C/TCLKC/PO17	ET_ERXD3/CTS5#/ RTS5#/SS5#/SSLA1/ SCL3	IRQ14	
92	VSS						
93		P73	CS3#	PO16	ET_WOL		
94		PB7	A15	MTIOC3B/TIOCB5/PO31	ET_CRS/RMII_CRS_DV/ TXD9/SMOSI9/SSDA9		
95		PB6	A14	MTIOC3D/TIOCA5/PO30	ET_ETXD1/RMII_TXD1/ RXD9/SMISO9/SSCL9		
96		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	ET_ETXD0/RMII_TXD0/ SCK9		
97		PB4	A12	TIOCA4/PO28	ET_TX_EN/ RMII_TXD_EN/CTS9#/ RTS9#/SS9#		
98		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	ET_RX_ER/RMII_RX_ER/ SCK4/SCK6		
99		PB2	A10	TIOCC3/TCLKC/PO26	ET_RX_CLK/REF50CK/ CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#		

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (5/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
N7	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET_EXOUT	IRQ10	
N8	VSS						
N9		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA/ET_COL	IRQ14	
N10	TRSYNC	P82	EDREQ1	MTIOC4A/PO28	TXD10/SMOSI10/SSDA10/ ET_ETXD1/RMII_TXD1		
N11		PC3	A19	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ IETXD/ET_TX_ER		
N12		P75	CS5#	PO20	SCK11/ET_ERXD0/ RMII_RXD0		
N13		P74	CS4#	PO19	CTS11#/RTS11#/SS11#/ ET_ERXD1/RMII_RXD1		

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (5/5)

Pin No. 144-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
125		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
126		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
127		P93	A19		CTS7#/RTS7#/SS7#		AN017
128		P92	A18		RXD7/SMISO7/SSCL7		AN016
129		P91	A17		SCK7		AN015
130	VSS						
131		P90	A16		TXD7/SMOSI7/SSDA7		AN014
132	VCC						
133		P47				IRQ15-DS	AN007
134		P46				IRQ14-DS	AN006
135		P45				IRQ13-DS	AN005
136		P44				IRQ12-DS	AN004
137		P43				IRQ11-DS	AN003
138		P42				IRQ10-DS	AN002
139		P41				IRQ9-DS	AN001
140	VREFL0						
141		P40				IRQ8-DS	AN000
142	VREFH0						
143	AVCC0						
144		P07				IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

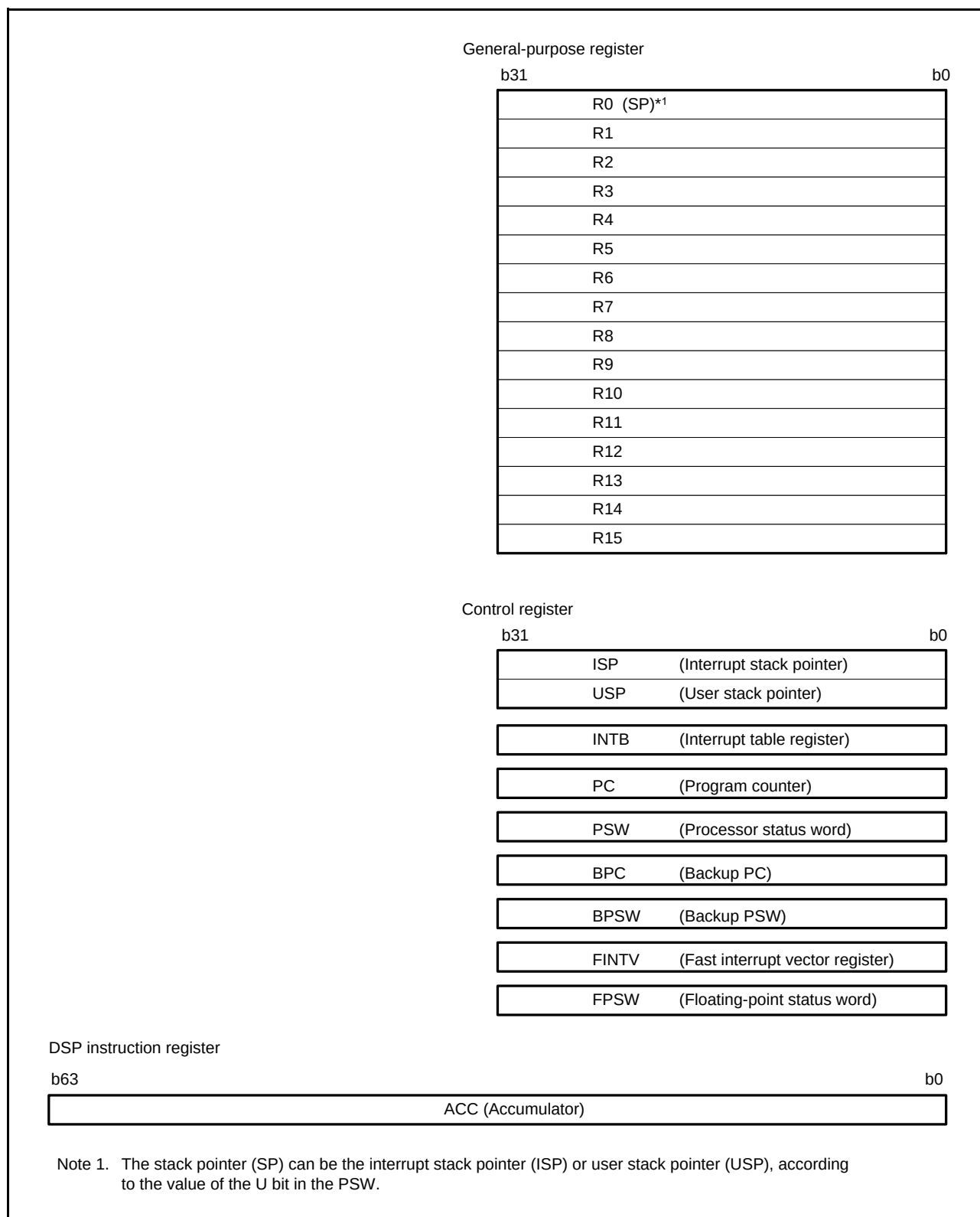


Figure 2.1 Register Set of the CPU

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

Table 4.1 List of I/O Registers (Address Order) (14/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK>PCLK	ICLK<PCLK	
0008 7400h	ICU	DMAC activation request select register 0	DMRSR0	8	8	2 ICLK		ICUb
0008 7404h	ICU	DMAC activation request select register 1	DMRSR1	8	8	2 ICLK		
0008 7408h	ICU	DMAC activation request select register 2	DMRSR2	8	8	2 ICLK		
0008 740Ch	ICU	DMAC activation request select register 3	DMRSR3	8	8	2 ICLK		
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8	2 ICLK		
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8	2 ICLK		
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8	2 ICLK		
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8	2 ICLK		
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8	2 ICLK		
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK		
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8	2 ICLK		
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8	2 ICLK		
0008 7508h	ICU	IRQ control register 8	IRQCR8	8	8	2 ICLK		
0008 7509h	ICU	IRQ control register 9	IRQCR9	8	8	2 ICLK		
0008 750Ah	ICU	IRQ control register 10	IRQCR10	8	8	2 ICLK		
0008 750Bh	ICU	IRQ control register 11	IRQCR11	8	8	2 ICLK		
0008 750Ch	ICU	IRQ control register 12	IRQCR12	8	8	2 ICLK		
0008 750Dh	ICU	IRQ control register 13	IRQCR13	8	8	2 ICLK		
0008 750Eh	ICU	IRQ control register 14	IRQCR14	8	8	2 ICLK		
0008 750Fh	ICU	IRQ control register 15	IRQCR15	8	8	2 ICLK		
0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8	2 ICLK		
0008 7511h	ICU	IRQ pin digital filter enable register 1	IRQFLTE1	8	8	2 ICLK		
0008 7514h	ICU	IRQ pin digital filter setting register 0	IRQFLTC0	16	16	2 ICLK		
0008 7516h	ICU	IRQ pin digital filter setting register 1	IRQFLTC1	16	16	2 ICLK		
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK		
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK		
0008 7582h	ICU	Non-maskable interrupt status clear register	NMICLR	8	8	2 ICLK		
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK		
0008 7590h	ICU	NMI pin digital filter enable register	NMIFLTE	8	8	2 ICLK		
0008 7594h	ICU	NMI pin digital filter setting register	NMIFLTC	16	16	2 ICLK		
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK	
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8020h	WDT	WDT refresh register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTA
0008 8022h	WDT	WDT control register	WDTCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8024h	WDT	WDT status register	WDTSR	16	16	2, 3 PCLKB	2 ICLK	
0008 8026h	WDT	WDT reset control register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (19/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 8313h	RIIC0	I ² C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIIC
0008 8320h	RIIC1	I ² C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8321h	RIIC1	I ² C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8322h	RIIC1	I ² C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8323h	RIIC1	I ² C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8324h	RIIC1	I ² C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8325h	RIIC1	I ² C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8326h	RIIC1	I ² C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8327h	RIIC1	I ² C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8328h	RIIC1	I ² C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8329h	RIIC1	I ² C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 832Ah	RIIC1	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 832Ah	RIIC1	Timeout Internal Counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK	
0008 832Bh	RIIC1	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 832Bh	RIIC1	Timeout Internal Counter U	TMOCNTU	8	8	2, 3 PCLKB	2 ICLK	
0008 832Ch	RIIC1	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 832Dh	RIIC1	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 832Eh	RIIC1	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 832Fh	RIIC1	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8330h	RIIC1	I ² C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8331h	RIIC1	I ² C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8332h	RIIC1	I ² C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8333h	RIIC1	I ² C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8340h	RIIC2	I ² C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8341h	RIIC2	I ² C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8342h	RIIC2	I ² C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8343h	RIIC2	I ² C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8344h	RIIC2	I ² C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8345h	RIIC2	I ² C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8346h	RIIC2	I ² C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8347h	RIIC2	I ² C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8348h	RIIC2	I ² C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8349h	RIIC2	I ² C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 834Ah	RIIC2	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 834Bh	RIIC2	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 834Ch	RIIC2	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 834Dh	RIIC2	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 834Eh	RIIC2	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 834Fh	RIIC2	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8350h	RIIC2	I ² C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8351h	RIIC2	I ² C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8352h	RIIC2	I ² C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8353h	RIIC2	I ² C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8360h	RIIC3	I ² C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8361h	RIIC3	I ² C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8362h	RIIC3	I ² C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8363h	RIIC3	I ² C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8364h	RIIC3	I ² C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8365h	RIIC3	I ² C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8366h	RIIC3	I ² C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8367h	RIIC3	I ² C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	

Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Supply current*1	High-speed operating mode	Max.*2		I _{CC} *3	—	—	100	mA	ICLK = 100 MHz PCLKA = 100MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 100MHz	
		Normal*4	Peripheral function: clock signal supplied*4		—	52	—			
			Peripheral function: clock signal stopped*4		—	40	—			
		Sleep mode			—	25	65			
		All-module-clock-stop mode (reference value)			—	20	38			
		Increased by BGO operation*5			—	15	—			
	Low-speed operating mode 1*6				—	4	—			ICLK = 1 MHz
	Low-speed operating mode 2				—	1	—			
	Software standby mode				—	0.2	6			
	Deep software standby mode	Power supplied to RAM and USB resume detecting unit			—	22	200			μA
		Power not supplied to RAM and USB resume detecting unit	Power-on reset circuit and low-power consumption function disabled	—	21	60				
			Power-on reset circuit and low-power	—	6.2	28				
		Increase when the RTC is operating	When a crystal oscillator for low clock loads is in use	—	1.0	—				
			When a crystal oscillator for standard clock loads is in use	—	3.0	—				
		RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)	When a crystal oscillator for low clock loads is in use	—	0.9	—	V _{BATT} = 2.0 V, VCC = 0V			
				—	1.6	—	V _{BATT} = 3.3 V, VCC = 0V			
			When a crystal oscillator for standard clock loads is in use	—	1.7	—	V _{BATT} = 2.0 V (for products with 100 pins or more), V _{BATT} = 2.3 V (for the 64-pin product), VCC = 0V			
				—	3.3	—	V _{BATT} = 3.3 V, VCC = 0V			
	Analog power supply current*7	During 12-bit A/D conversion (including temperature sensor)			I _{AVCC0}	—	2.3	3.2	mA	
		During 10-bit A/D conversion			I _{VREFH} *9	—	1.0	1.65		mA
During D/A conversion (per unit)			—	0.7		1.0	mA			
Waiting for A/D, D/A conversion (all units)*10			—	—	25	35		μA		
A/D, D/A converter in standby mode (all units)*10				—	0.1	4.0	μA			
Reference power supply current	During 12-bit A/D conversion			I _{VREFH0}	—	0.6		0.7	mA	
	Waiting for 12-bit A/D conversion (per unit)				—	0.5	0.6	mA		
	12-bit A/D converter in standby mode (per unit)				—	0.1	2.0			μA

Table 5.6 DC Characteristics (4)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible total power consumption*1	P_d	—	—	380	mW	*2

Note 1. This is the total power consumption of the chip as a whole (including the power consumed by the output buffers).

Note 2. Contact a Renesas sales office or agent regarding further details of the conditions of measurement.

Table 5.7 Permissible Output Currents

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	2.0	mA
	All output pins*2	High drive	I_{OL}			3.8	mA
Permissible output low current (max. value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	4.0	mA
	All output pins*2	High drive	I_{OL}			7.6	mA
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	−2.0	mA
	USB_DPUPE pin*2	High drive	I_{OH}	—	—	−3.8	mA
Permissible output high current (max. value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	−4.0	mA
	All output pins*2	High drive	I_{OH}	—	—	−7.6	mA
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	—	—	−80	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

Table 5.10 Operation Frequency Value (Low-Speed Operating Mode 2)

Conditions: $V_{CC} = AVCC0 = VREFH = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operation frequency	System clock (ICLK)		f	32	—	143.75	kHz
	Peripheral module clock (PCLKA)			—	—	143.75	
	Peripheral module clock (PCLKB)			—	—	143.75	
	FlashIF clock (FCLK)			32	—	143.75	
	External bus clock (BCLK)	Packages with 177 to 144 pins		—	—	143.75	
		Packages with 100 pins or less		—	—	143.75	
	BCLK pin output	Packages with 177 to 144 pins		—	—	143.75	
		Packages with 100 pins or less		—	—	143.75	
	SDRAM clock (SDCLK)	Packages with 177 to 144 pins only		—	—	143.75	
	SDCLK pin output	Packages with 177 to 144 pins only		—	—	143.75	
USB clock (UCLK)		—	—	143.75			
IEBUS clock (IECLK)		—	—	143.75			

5.3.1 Reset Timing

Table 5.11 Reset Timing

Conditions: $V_{CC} = AVCC0 = VREFH = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	2	—	—	ms	Figure 5.1
	Deep software standby mode	t_{RESWD}	1	—	—	ms	Figure 5.2
	Software standby mode, low-speed operating mode 2	t_{RESWS}	1	—	—	ms	
	Programming or erasure of the ROM or E2 data-flash memory or blank checking of the E2 DataFlash memory	t_{RESW}	200	—	—	μ s	
	Other than above	t_{RESW}	200	—	—	μ s	
Wait time after RES# cancellation		t_{RESWT}	59	—	60	t_{cyc}	Figure 5.1
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	112	—	120	t_{cyc}	

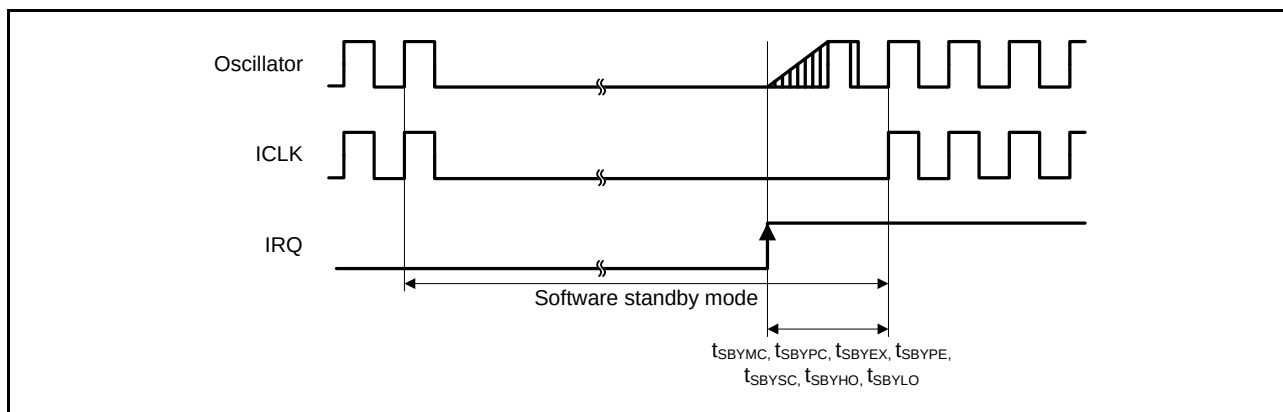


Figure 5.13 Software Standby Mode Cancellation Timing

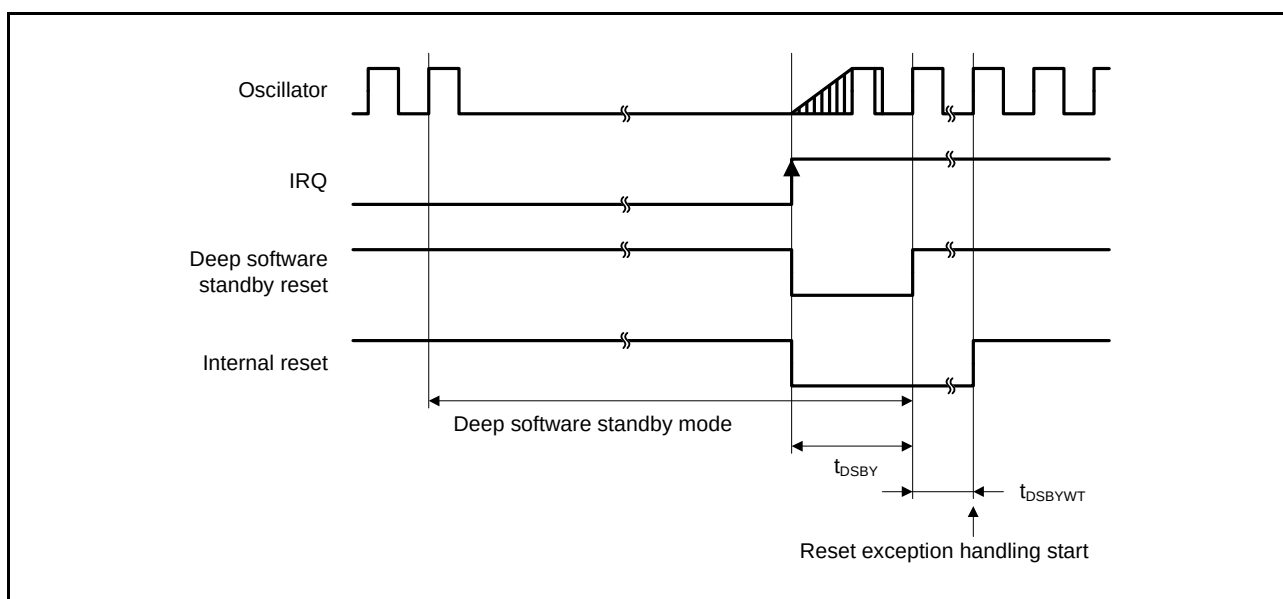


Figure 5.14 Deep Software Standby Mode Cancellation Timing

5.3.4 Control Signal Timing

Table 5.15 Control Signal Timing

Conditions: $V_{CC} = AVCC0 = VREFH = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_c (PCLK) \times 2 \leq 200$ ns Figure 5.15
		$t_c (PCLK) \times 2$				$t_c (PCLK) \times 2 > 200$ ns Figure 5.15
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_c (PCLK) \times 2 \leq 200$ ns Figure 5.16
		$t_c (PCLK) \times 2$				$t_c (PCLK) \times 2 > 200$ ns Figure 5.16

5.3.5 Bus Timing

Table 5.16 Bus Timing (packages with 177 to 144 pins)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V,
 $ICLK = 8$ to 100 MHz, $BCLK$ pin = 8 to 50 MHz, $SDCLK$ pin = 8 to 50 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, $I_{OH} = -1.0$ mA, $I_{OL} = 1.0$ mA, $C = 30$ pF
 High drive output is selected by the drive capacity control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	15	ns	Figure 5.17 to Figure 5.22
Byte control delay time	t_{BCD}	—	15	ns	
CS# delay time	t_{CSD}	—	15	ns	
ALE delay time	t_{ALED}	—	20	ns	
RD# delay time	t_{RSD}	—	15	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	15	ns	
Write data delay time	t_{WDD}	—	15	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.23
WAIT# hold time	t_{WTH}	0	—	ns	
Address delay time 2 (SDRAM)	t_{AD2}	1	15	ns	Figure 5.24 to Figure 5.30
CS# delay time 2 (SDRAM)	t_{CSD2}	1	15	ns	
DQM delay time (SDRAM)	t_{DQMD}	1	15	ns	
CKE delay time (SDRAM)	t_{CKED}	1	15	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	12	—	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	0	—	ns	
Write data delay time 2 (SDRAM)	t_{WDD2}	—	15	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	1	—	ns	
WE# delay time (SDRAM)	t_{WED}	1	15	ns	
RAS# delay time (SDRAM)	t_{RASD}	1	15	ns	
CAS# delay time (SDRAM)	t_{CASD}	1	15	ns	

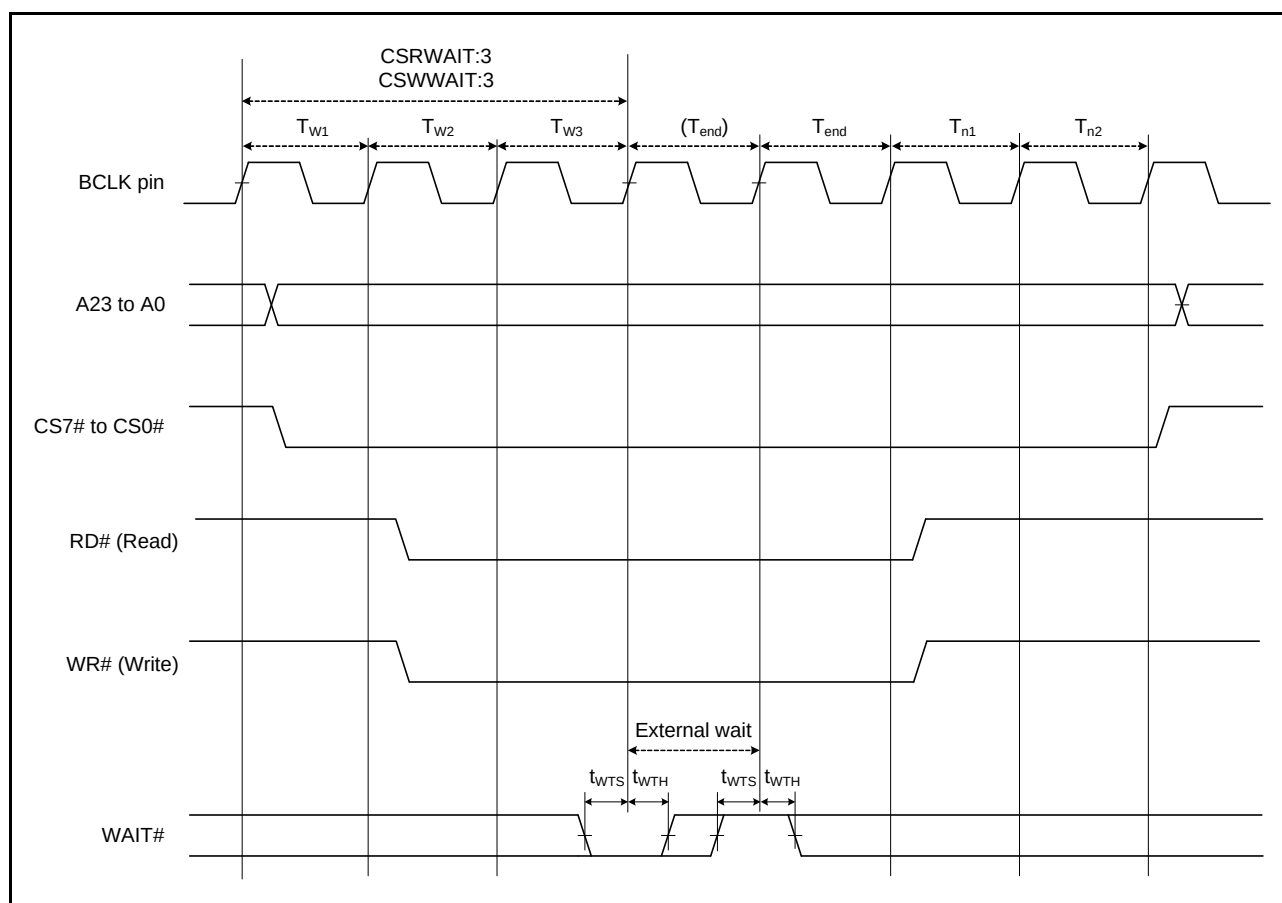


Figure 5.23 External Bus Timing/External Wait Control

Table 5.21 Timing of On-Chip Peripheral Modules (3)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V*1, $VREFH0 = 2.7$ V to $AVCC0$ *1,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V,
 $PCLK = 8$ to 50 MHz,
 $T_a = T_{opr}$
 High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit*2	Test Conditions
RSPI	Data output delay time	Master	Packages with 177 to 144 pins	t_{OD}	—	18	ns	Figure 5.43 to Figure 5.46 C = 30pF
			Packages with 100 pins or less		—	30		
		Slave	Packages with 177 to 144 pins		—	$3 \times t_{Pcyc} + 40$		
			Packages with 100 pins or less		—	$3 \times t_{Pcyc} + 50$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	Packages with 177 to 144 pins	t_{Dr}, t_{Df}	—	5	ns	
			Packages with 100 pins or less		—	10		
		Input			—	1	μs	
	SSL rise/fall time	Output	Packages with 177 to 144 pins	t_{SSLr}, t_{SSLf}	—	5	ns	
			Packages with 100 pins or less		—	10		
		Input			—	1	μs	
Slave access time				t_{SA}	—	4	t_{Pcyc}	Figure 5.45 and Figure 5.46 C = 30pF
Slave output release time				t_{REL}	—	3	t_{Pcyc}	

Note 1. When operation at 3.0 V or a lower voltage is needed, please contact a Renesas sales office.

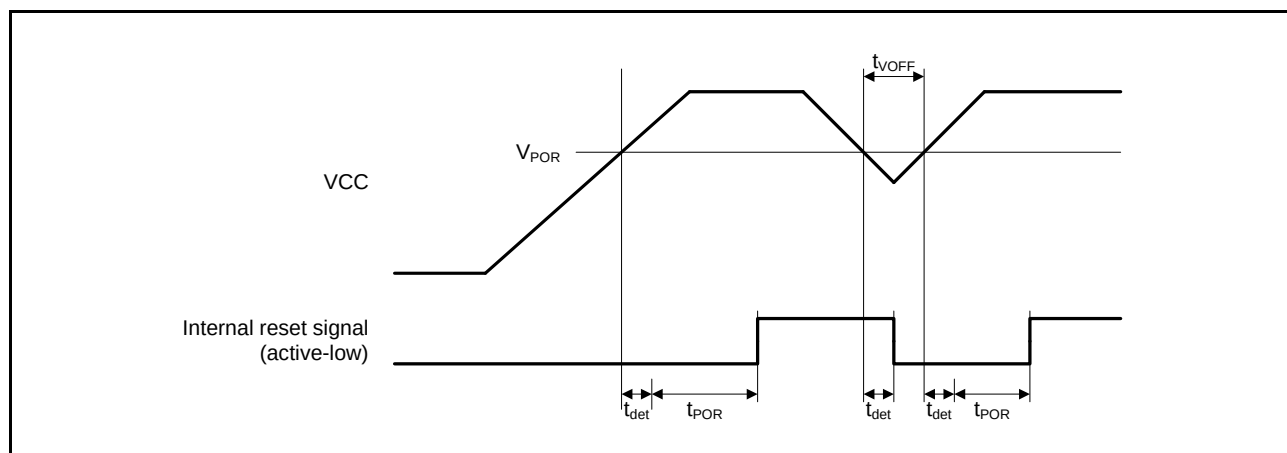
Note 2. t_{Pcyc} : PCLK cycle

5.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.33 Power-on Reset Circuit and Voltage Detection Circuit CharacteristicsConditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled	V _{POR}	2.5	2.6	2.7	V	Figure 5.63
		Low power consumption function enabled		2.0	2.35	2.7		
	Voltage detection circuit (LVD0)		V _{det0}	2.7	2.80	2.9		Figure 5.64
	Voltage detection circuit (LVD1)		V _{det1_A}	2.75	2.95	3.15		Figure 5.65
	Voltage detection circuit (LVD2)		V _{det2_A}	2.75	2.95	3.15		Figure 5.66
Internal reset time	Power-on reset time		t _{POR}	—	4.6	—	ms	Figure 5.63
	LVD0 reset time		t _{LVD0}	—	4.6	—		Figure 5.64
	LVD1 reset time		t _{LVD1}	—	0.9	—		Figure 5.65
	LVD2 reset time		t _{LVD2}	—	0.9	—		Figure 5.66
Minimum VCC down time			t _{VOFF}	200	—	—	μs	Figure 5.63 and Figure 5.64
Response delay time			t _{det}	—	—	200	μs	Figure 5.63 to Figure 5.66
LVD operation stabilization time (after LVD is enabled)			Td _(E-A)	—	—	3	μs	Figure 5.65 and Figure 5.66
Hysteresis width (LVD1 and LVD2)			V _{LVH}	—	80	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det1} , and V_{det2} for the POR/ LVD.

**Figure 5.63 Power-on Reset Timing**

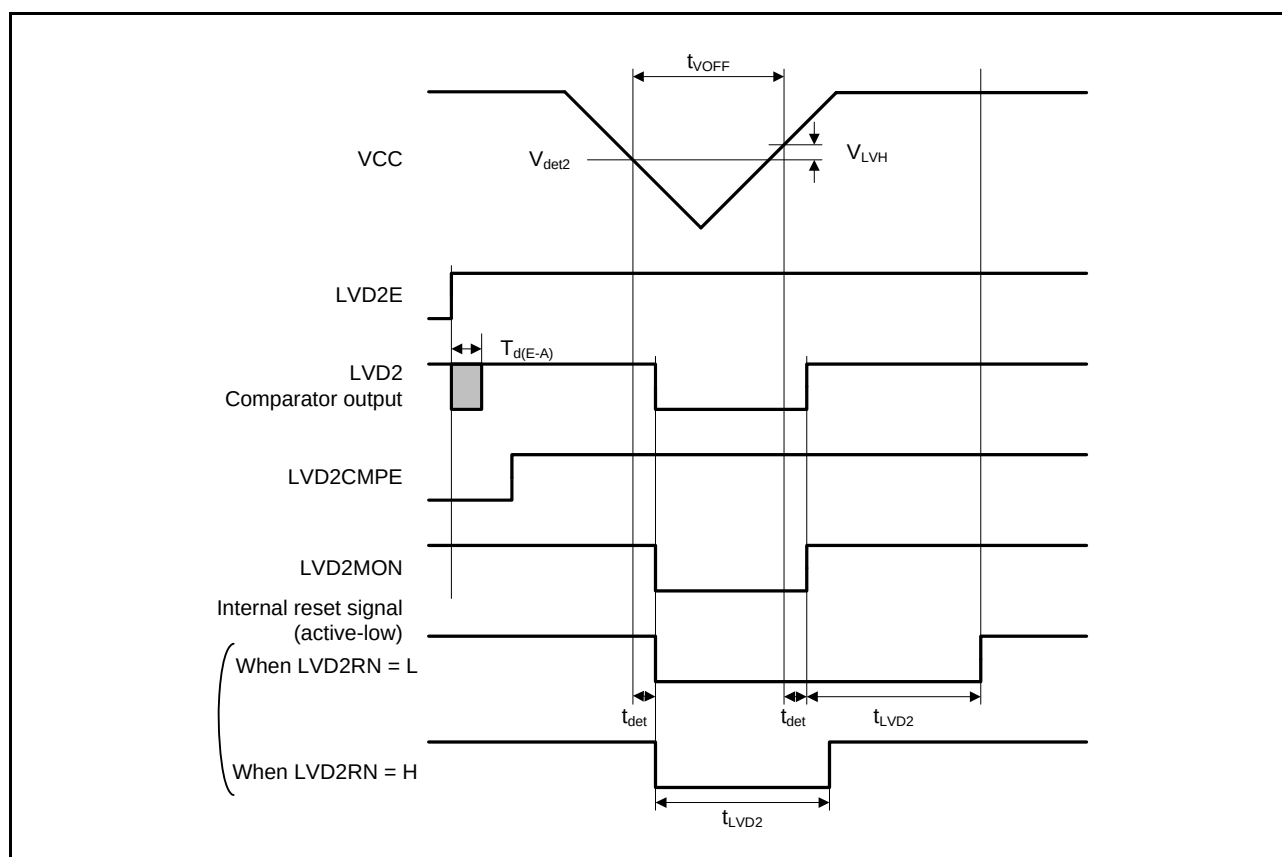
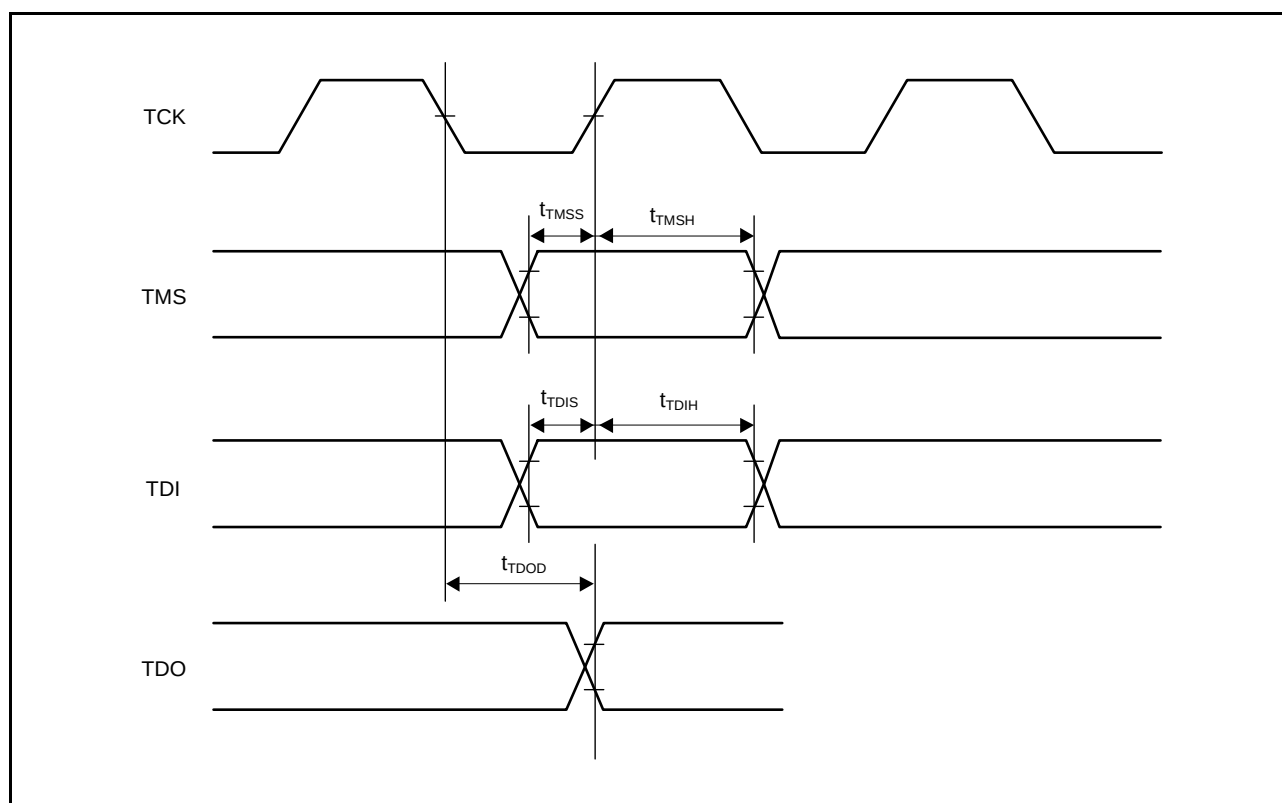


Figure 5.66 Voltage Detection Circuit Timing (V_{det2})

**Figure 5.72** Boundary Scan Input/Output Timing