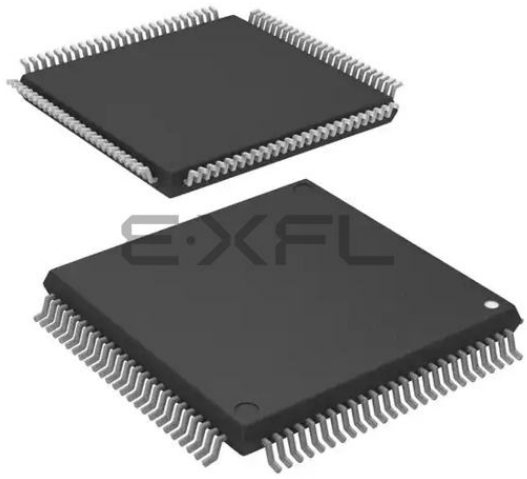
Renesas Electronics America Inc - R5F5631FHDFP#V0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631fhdfp-v0

Table 1.4 Pin Functions (4/6)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCId)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for clock signals.
	RXD12	Input	Input pin for data reception.
	TXD12	Output	Output pin for data transmission.
	CTS12#	Input	Transmit/receive start control input pins
	RTS12#	Output	Transmit/receive start control output pins
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pins for the I^2C clock
	SSDA12	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pins for the clock
	SMISO12	I/O	Input/output pins for slave transmit data.
	SMOSI12	I/O	Input/output pins for master transmit data.
	SS12#	Input	Input pins for chip select signals
	• Extended serial mode		
	RXDX12	Input	Input pin for receive data
	TXDX12	Output	Output pin for transmit data
	SIOX12	I/O	Input/output pin for Transmit/receive data
I^2C bus interface	SCL0[FM+], SCL1 to SCL3	I/O	Input/output pin for clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0[FM+], SDA1 to SDA3	I/O	Input/output pin for data. Bus can be directly driven by the N-channel open drain output.
Ethernet controller	REF50CK	Input	50-MHz reference clock. This pin inputs reference signals for transmission/reception timings in RMII mode.
	RMII_CRS_DV	Input	Indicates that there are carrier detection signals and valid receive data on RMII_RXD1 and RMII_RXD0 in RMII mode.
	RMII_TXD0, RMII_TXD1	Output	2-bit transmit data in RMII mode.
	RMII_RXD0, RMII_RXD1	Input	2-bit receive data in RMII mode.
	RMII_TXD_EN	Output	Output pin for data transmit enable signals in RMII mode.
	RMII_RX_ER	Input	Indicates an error has occurred during reception of data in RMII mode.
	ET_CRS	Input	Carrier detection/data reception enable pin.
	ET_RX_DV	Input	Indicates that there are valid receive data on ET_ERXD3 to ET_ERXD0.
	ET_EXOUT	Output	General-purpose external output pin.
	ET_LINKSTA	Input	Inputs link status from the PHY-LSI.
	ET_ETXD0 to ET_ETXD3	Output	4 bits of MII transmit data.
	ET_ERXD0 to ET_ERXD3	Input	4 bits of MII receive data.
	ET_TX_EN	Output	Transmit enable pin. Indicates that transmit data is ready on ET_ETXD3 to ET_ETXD0.
	ET_TX_ER	Output	Transmit error pin. Notifies the PHY_LSI of an error during transmission.
	ET_RX_ER	Input	Receive error pin. Recognizes an error during reception.
	ET_TX_CLK	Input	Transmit clock pin. This pin inputs reference signals for output timings from ET_TX_EN, ET_ETXD3 to ET_ETXD0, and ET_TX_ER.
	ET_RX_CLK	Input	Receive clock pin. This pin inputs reference signals for input timings to ET_RX_DV, ET_ERXD3 to ET_ERXD0, and ET_RX_ER.
	ET_COL	Input	Inputs collision detection signals.
	ET_WOL	Output	Receives Magic packets.
	ET_MDC	Output	Outputs reference clock signals for information transfer via ET_MDIO.

Table 1.4 Pin Functions (6/6)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH	Input	Reference voltage input pin for the 10-bit A/D converter and D/A converter. This is used as the analog power supply for the respective modules. Connect this pin to VCC if neither the 10-bit A/D converter nor the D/A converter is in use.
	VREFL	Input	Reference ground pin for the 10-bit A/D converter and D/A converter. This is used as the analog ground for the respective modules. Set this pin to the same potential as the VSS pin.
I/O ports	P00 to P03, P05, P07	I/O	6-bit input/output pins.
	P10 to P17	I/O	8-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 is an input pin)
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P57	I/O	8-bit input/output pins.
	P60 to P67	I/O	8-bit input/output pins.
	P70 to P77	I/O	8-bit input/output pins.
	P80 to P87	I/O	8-bit input/output pins.
	P90 to P97	I/O	8-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PF0 to PF5	I/O	6-bit input/output pins.
	PG0 to PG7	I/O	8-bit input/output pins.
	PJ3, PJ5	I/O	2-bit input/output pins.

1.5 Pin Assignments

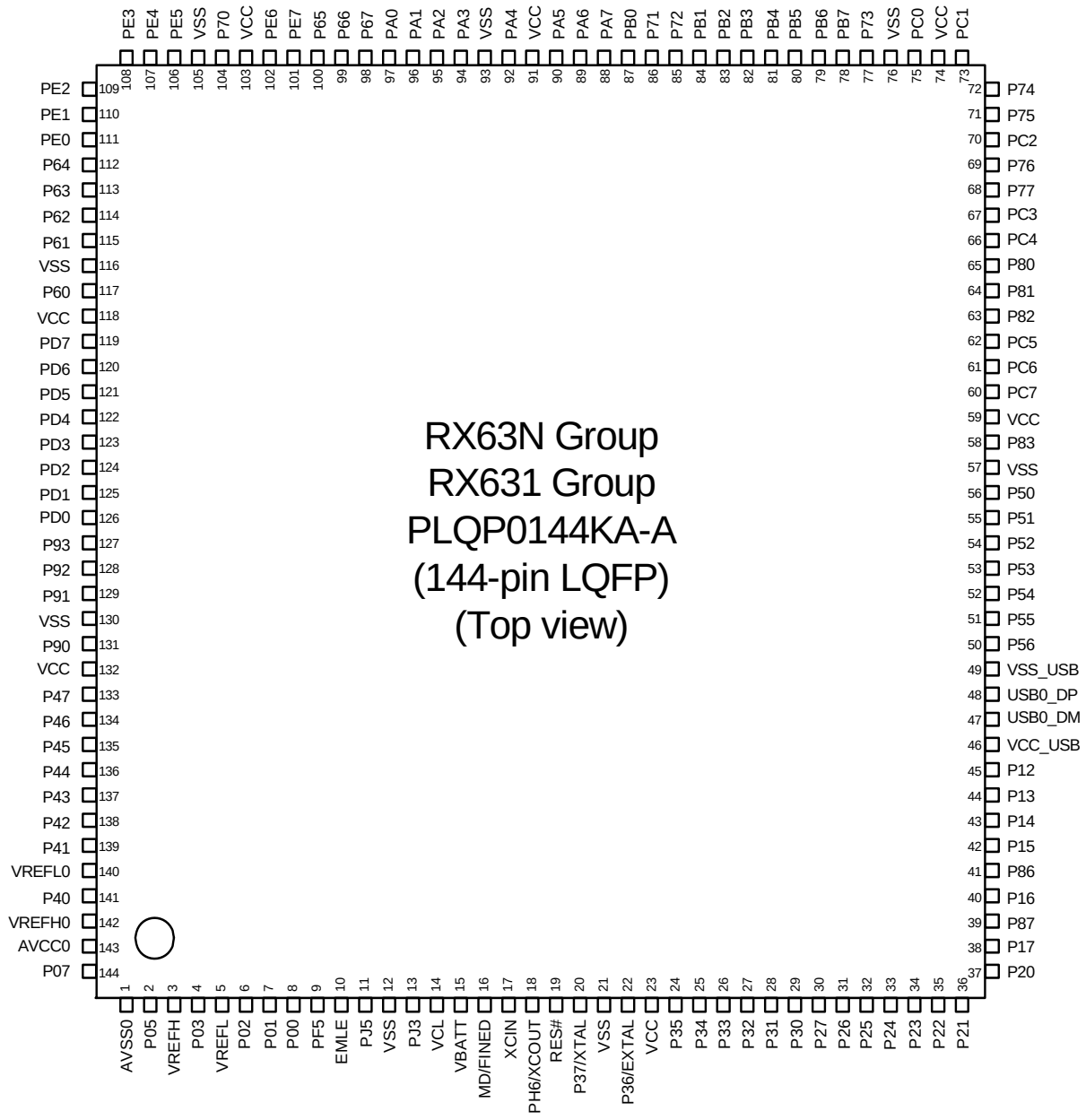
Figure 1.5 to Figure 1.12 show the pins assignments. Table 1.5 to Table 1.13 show the list of pins and pin functions. Power pins and I/O ports are shown in the pin assignment diagrams.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	VCC	P61								P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	VCC	P96	PD3	PD5								P50	P51	P52	P84	9
8	P94	PD1	PD2	VSS								P53	VCC_ USB	USB1_ DP	USB1_ DM	8
7	VSS	P92	PD0	P95								P54	P55	VSS_ USB	USB0_ DP	7
6	VCC	P91	P90	P93								P56	P57	VCC_ USB	USB0_ DM	6
5	P46	P47	P45	P44	NC							P13	P12	P10	P11	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P85	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	VREFH	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	VREFL	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

RX63N Group
RX631 Group
PTLG0177KA-A
(177-pin TFLGA)
(Top perspective view)

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.3 Pin Assignment (177-Pin TFLGA)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pins and Pin Functions (144-Pin LQFP).

Figure 1.7 Pin Assignment (144-Pin LQFP)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
M2		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3# SMOSI1/SS3#/SSDA1/ MOSIB		
M3		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/USB0_VBUSEN/ PIXCLK		
M4		P86		TIOCA0	PIXD1		
M5		P13		MTIOC0B/TIOCA5/TMO3/ PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
M6		P56	WR2#/BC2#/ EDACK1	MTIOC3C/TIOCA1			
M7		P54	ALE/EDACK0	MTIOC4B/TMCI1	ET_LINKSTA/CTS2#/ RTS2#/SS2#/CTX1		
M8		P53*2	BCLK				
M9		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
M10		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	ET_ETXD2/SCK8/ RSPCKA		
M11		P81	EDACK0	MTIOC3D/PO27	ET_ETXD0/RMII_TXD0/ RXD10/SMISO10/SSCL10		
M12		P77	CS7#	PO23	ET_RX_ER/RMII_RX_ER/ TXD11/SMOSI11/SSDA11		
M13		PB7	A15	MTIOC3B/TIOCB5/PO31	ET_CRS/RMII_CRS_DV/ TXD9/SMOSI9/SSDA9		
M14		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	ET_ETXD0/RMII_TXD0/ SCK9		
M15		PB4	A12	TIOCA4/PO28	ET_TX_EN/ RMII_TXD_EN/CTS9#/ RTS9#/SS9#		
N1	VCC						
N2		P23	EDACK0	MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7		
N3		P22	EDREQ0	MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0/USB0_DRPD/ PIXD6		
N4		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ USB1_DPUPE/PIXD0	IRQ5	
N5		P12		MTIC5U/TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
N6		P57	WAIT#/WR3#/ BC3#/EDREQ1				
N7		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	ET_EXOUT/CRX1	IRQ10	
N8	VCC_USB						
N9		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
N10		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	ET_COL/TXD8/SMOSI8/ SSDA8/MISOA	IRQ14	
N11		P82	EDREQ1	MTIOC4A/PO28	ET_ETXD1/RMII_TXD1/ TXD10/SMOSI10/SSDA10		
N12		PC3	A19	MTIOC4D/TCLKB/PO24	ET_TX_ER/TXD5/ SMOSI5/SSDA5/IETXD		
N13		PC0	A16	MTIOC3C/TCLKC/PO17	ET_ERXD3/CTS5#/ RTS5#/SS5#/SSLA1/ SCL3	IRQ14	
N14		P73	CS3#	PO16	ET_WOL		
N15	VSS						

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (1/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
A1	AVSS0						
A2		P07				IRQ15	ADTRG0#
A3		P40				IRQ8-DS	AN000
A4		P42				IRQ10-DS	AN002
A5		P45				IRQ13-DS	AN005
A6		P90	A16		TXD7/SMOSI7/SSDA7		AN014
A7		P92	A18		RXD7/SMISO7/SSCL7		AN016
A8		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
A9		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
A10	VSS						
A11		P62	CS2#/RAS#				
A12		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/ PO18	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB		ANEX1
A13		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/ PO26/POE8#	CTS12#/RTS12#/SS12#/ MISOB/ET_ERXD3		AN1
B1	VREFH						
B2	AVCC0						
B3		P05				IRQ13	DA1
B4	VREFL0						
B5		P43				IRQ11-DS	AN003
B6		P47				IRQ15-DS	AN007
B7		P91	A17		SCK7		AN015
B8		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
B9		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
B10	VCC						
B11		P61	CS1#/SDCS#				
B12		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/ PO23	RXD12/SMISO12/SSCL12/ RXDX12/SSLB3/MOSIB	IRQ7-DS	AN0
B13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0/ET_ERXD2		AN2
C1	VREFL						
C2		P02		TMCI1	SCK6	IRQ10	AN020
C3	VREFH0						
C4		P41				IRQ9-DS	AN001
C5		P46				IRQ14-DS	AN006
C6	VSS						
C7		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
C8		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
C9		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
C10		P63	CS3#/CAS#				
C11		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
C12	SDCLK	P70					
C13	VSS						
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
D2		PF5				IRQ4	
D3		P03				IRQ11	DA0
D4		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (4/5)

Pin No. 144-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
89		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	CTS5#/RTS5#/SS5# MOSIA/ET_EXOUT		
90		PA5	A5	TIOCB1/PO21	RSPCKA/ET_LINKSTA		
91	VCC						
92		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0/ET_MDC	IRQ5-DS	
93	VSS						
94		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/SSCL5/ ET_MDIO	IRQ6-DS	
95		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
96		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2/ET_WOL	IRQ11	
97		PA0	A0/BC0#	MTIOC4A/TIOCA0/ PO16	SSLA1/ET_TX_EN/ RMII_TXD_EN		
98		P67	CS7#/DQM1		CRX2*2	IRQ15	
99		P66	CS6#/DQM0		CTX2*2		
100		P65	CS5#/CKE				
101		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
102		PE6	D14[A14/D14]	TIOCA11	MOSIB	IRQ6	AN4
103	VCC						
104	SDCLK	P70					
105	VSS						
106		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	RSPCKB/ET_RX_CLK/ REF50CK	IRQ5	AN3
107		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0/ET_ERXD2		AN2
108		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/ PO26/POE8#	CTS12#/RTS12#/ SS12#/MISOB/ ET_ERXD3		AN1
109		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/ PO23	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3/MOSIB	IRQ7-DS	AN0
110		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/ PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/ RSPCKB		ANEX1
111		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
112		P64	CS4#/WE#				
113		P63	CS3#/CAS#				
114		P62	CS2#/RAS#				
115		P61	CS1#/SDCS#				
116	VSS						
117		P60	CS0#				
118	VCC						
119		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
120		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
121		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
122		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
123		PD3	D3[A3/D3]	TIOCB8/TCLKH/ POE8#	RSPCKC	IRQ3	AN011
124		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (2/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
D2	XCOUT						
D3	MD/FINED						
D4	VBATT						
D5		P45				IRQ13-DS	AN005
D6		P46				IRQ14-DS	AN006
D7		PE6	D14[A14/D14]		MOSIB	IRQ6	AN4
D8		PE7	D15[A15/D15]		MISOB	IRQ7	AN5
D9		PA1	A1	MTIOC0B/ MTCLKC/ TIOCB0/PO17	SCK5/SSLA2/ ET_WOL	IRQ11	
D10		PA0	A0/BC0#	MTIOC4A/ TIOCA0/PO16	SSLA1/ET_TX_EN/ RMII_TXD_EN		
E1	XTAL	P37					
E2	VSS						
E3	RES#						
E4	TRST#	P34		MTIOC0A/ TMCI3/PO12/ POE2#	SCK6/SCK0/ USB0_DPRPD	IRQ4	
E5		P41				IRQ9-DS	AN001
E6		PA2	A2	PO18	RXD5/SMISO5/ SSCL5/SSLA3		
E7		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE2#	CTS5#/RTS5#/ SS5#/MOSIA/ ET_EXOUT		
E8		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0/ ET_MDC	IRQ5-DS	
E9		PA5	A5	TIOCB1/PO21	RSPCKA/ ET_LINKSTA		
E10		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET_MDIO	IRQ6-DS	
F1	EXTAL	P36					
F2	VCC						
F3		P35				NMI	
F4		P32		MTIOC0C/ TIOCC0/TMO3/ PO10/ RTCOUT/ RTCIC2	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0*1/ USB0_VBUSEN	IRQ2-DS	
F5		P12		TMCI1	RXD2/SMISO2/ SSCL2/SCL0[FM+]	IRQ2	
F6		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE3#	SCK6/ET_RX_ER/ RMII_RX_ER		

Table 1.12 List of Pins and Pin Functions (64-Pin LQFP) (2/3)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	Timer (MTU2a, TPUa, TMR, PPG, RTCa, POE2a)	Timer Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
32		PC2	MTIOC4B/TCLKA/ PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD		
33		PB7/ PC1	MTIOC3B/TIOCB5/ PO31	TXD9/SMOSI9/SSDA9		
34		PB6/ PC0	MTIOC3D/TIOCA5/ PO30	RXD9/SMISO9/SSCL9		
35		PB5	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	SCK9		
36		PB3	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	SCK6		
37		PB1	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD6/SMOSI6/SSDA6	IRQ4-DS	
38	VCC					
39		PB0	MTIC5W/TIOCA3/PO24	RXD6/SMISO6/SSCL6/ RSPCKA	IRQ12	
40	VSS					
41		PA6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	CTS5#/RTS5#/SS5#/ MOSIA		
42		PA4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS	
43		PA3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/SSCL5	IRQ6-DS	
44		PA1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2/SCL2	IRQ11	
45		PA0	MTIOC4A/TIOCA0/ PO16	SSLA1		
46		PE5	MTIOC4C/MTIOC2B	RSPCKB	IRQ5	AN013
47		PE4	MTIOC4D/MTIOC1A/ PO28	SSLB0		AN012
48		PE3	MTIOC4B/PO26/POE8#	CTS12#/RTS12#/ SS12#/MISOB		AN011
49		PE2	MTIOC4A/PO23	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3/MOSIB	IRQ7-DS	AN010
50		PE1	MTIOC4C/PO18	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB		AN009
51		PE0		SCK12/SSLB1		AN008
52	VREFL					
53		P46			IRQ14-DS	AN006
54	VREFH					
55		P44			IRQ12-DS	AN004
56		P43			IRQ11-DS	AN003
57		P42			IRQ10-DS	AN002
58		P41			IRQ9-DS	AN001
59	VREFL0					
60		P40			IRQ8-DS	AN000

4. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral busses 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.
In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

(4) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

Table 4.1 List of I/O Registers (Address Order) (5/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 650Ch	MPU	Memory-protection error status register	MPESTS	32	32	1 ICLK		MPU
0008 6514h	MPU	Data memory-protection error address register	MPDEA	32	32	1 ICLK		
0008 6520h	MPU	Region search address register	MPSA	32	32	1 ICLK		
0008 6524h	MPU	Region search operation register	MPOPS	16	16	1 ICLK		
0008 6526h	MPU	Region invalidation operation register	MPOPI	16	16	1 ICLK		
0008 6528h	MPU	Instruction-hit region register	MHITI	32	32	1 ICLK		
0008 652Ch	MPU	Data-hit region register	MHITD	32	32	1 ICLK		
0008 7010h	ICU	Interrupt request register 016	IR016	8	8	2 ICLK		ICUb
0008 7015h	ICU	Interrupt request register 021	IR021	8	8	2 ICLK		
0008 7017h	ICU	Interrupt request register 023	IR023	8	8	2 ICLK		
0008 701Bh	ICU	Interrupt request register 027	IR027	8	8	2 ICLK		
0008 701Ch	ICU	Interrupt request register 028	IR028	8	8	2 ICLK		
0008 701Dh	ICU	Interrupt request register 029	IR029	8	8	2 ICLK		
0008 701Eh	ICU	Interrupt request register 030	IR030	8	8	2 ICLK		
0008 701Fh	ICU	Interrupt request register 031	IR031	8	8	2 ICLK		
0008 7020h	ICU	Interrupt request register 032	IR032	8	8	2 ICLK		
0008 7021h	ICU	Interrupt request register 033	IR033	8	8	2 ICLK		
0008 7022h	ICU	Interrupt request register 034	IR034	8	8	2 ICLK		
0008 7023h	ICU	Interrupt request register 035	IR035	8	8	2 ICLK		
0008 7024h	ICU	Interrupt request register 036	IR036	8	8	2 ICLK		
0008 7025h	ICU	Interrupt request register 037	IR037	8	8	2 ICLK		
0008 7026h	ICU	Interrupt request register 038	IR038	8	8	2 ICLK		
0008 7027h	ICU	Interrupt request register 039	IR039	8	8	2 ICLK		
0008 7028h	ICU	Interrupt request register 040	IR040	8	8	2 ICLK		
0008 7029h	ICU	Interrupt request register 041	IR041	8	8	2 ICLK		
0008 702Ah	ICU	Interrupt request register 042	IR042	8	8	2 ICLK		
0008 702Bh	ICU	Interrupt request register 043	IR043	8	8	2 ICLK		
0008 702Ch	ICU	Interrupt request register 044	IR044	8	8	2 ICLK		
0008 702Dh	ICU	Interrupt request register 045	IR045	8	8	2 ICLK		
0008 702Eh	ICU	Interrupt request register 046	IR046	8	8	2 ICLK		
0008 702Fh	ICU	Interrupt request register 047	IR047	8	8	2 ICLK		
0008 7030h	ICU	Interrupt request register 048	IR048	8	8	2 ICLK		
0008 7031h	ICU	Interrupt request register 049	IR049	8	8	2 ICLK		
0008 7032h	ICU	Interrupt request register 050	IR050	8	8	2 ICLK		
0008 7033h	ICU	Interrupt request register 051	IR051	8	8	2 ICLK		
0008 7034h	ICU	Interrupt request register 052	IR052	8	8	2 ICLK		
0008 7035h	ICU	Interrupt request register 053	IR053	8	8	2 ICLK		
0008 7036h	ICU	Interrupt request register 054	IR054	8	8	2 ICLK		
0008 7037h	ICU	Interrupt request register 055	IR055	8	8	2 ICLK		
0008 7038h	ICU	Interrupt request register 056	IR056	8	8	2 ICLK		
0008 7039h	ICU	Interrupt request register 057	IR057	8	8	2 ICLK		
0008 703Ah	ICU	Interrupt request register 058	IR058	8	8	2 ICLK		
0008 703Bh	ICU	Interrupt request register 059	IR059	8	8	2 ICLK		
0008 703Eh	ICU	Interrupt request register 062	IR062	8	8	2 ICLK		
0008 7040h	ICU	Interrupt request register 064	IR064	8	8	2 ICLK		
0008 7041h	ICU	Interrupt request register 065	IR065	8	8	2 ICLK		
0008 7042h	ICU	Interrupt request register 066	IR066	8	8	2 ICLK		
0008 7043h	ICU	Interrupt request register 067	IR067	8	8	2 ICLK		
0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2 ICLK		
0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2 ICLK		
0008 7046h	ICU	Interrupt request register 070	IR070	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (6/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK		ICUb
0008 7048h	ICU	Interrupt request register 072	IR072	8	8	2 ICLK		
0008 7049h	ICU	Interrupt request register 073	IR073	8	8	2 ICLK		
0008 704Ah	ICU	Interrupt request register 074	IR074	8	8	2 ICLK		
0008 704Bh	ICU	Interrupt request register 075	IR075	8	8	2 ICLK		
0008 704Ch	ICU	Interrupt request register 076	IR076	8	8	2 ICLK		
0008 704Dh	ICU	Interrupt request register 077	IR077	8	8	2 ICLK		
0008 704Eh	ICU	Interrupt request register 078	IR078	8	8	2 ICLK		
0008 704Fh	ICU	Interrupt request register 079	IR079	8	8	2 ICLK		
0008 705Ah	ICU	Interrupt request register 090	IR090	8	8	2 ICLK		
0008 705Bh	ICU	Interrupt request register 091	IR091	8	8	2 ICLK		
0008 705Ch	ICU	Interrupt request register 092	IR092	8	8	2 ICLK		
0008 705Dh	ICU	Interrupt request register 093	IR093	8	8	2 ICLK		
0008 7062h	ICU	Interrupt request register 098	IR098	8	8	2 ICLK		
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK		
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2 ICLK		
0008 706Bh	ICU	Interrupt request register 107	IR107	8	8	2 ICLK		
0008 706Ch	ICU	Interrupt request register 108	IR108	8	8	2 ICLK		
0008 706Dh	ICU	Interrupt request register 109	IR109	8	8	2 ICLK		
0008 706Eh	ICU	Interrupt request register 110	IR110	8	8	2 ICLK		
0008 706Fh	ICU	Interrupt request register 111	IR111	8	8	2 ICLK		
0008 7070h	ICU	Interrupt request register 112	IR112	8	8	2 ICLK		
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK		
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8	2 ICLK		
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8	2 ICLK		
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8	2 ICLK		
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8	2 ICLK		
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8	2 ICLK		
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8	2 ICLK		
0008 7080h	ICU	Interrupt request register 128	IR128	8	8	2 ICLK		
0008 7081h	ICU	Interrupt request register 129	IR129	8	8	2 ICLK		
0008 7082h	ICU	Interrupt request register 130	IR130	8	8	2 ICLK		
0008 7083h	ICU	Interrupt request register 131	IR131	8	8	2 ICLK		
0008 7084h	ICU	Interrupt request register 132	IR132	8	8	2 ICLK		
0008 7085h	ICU	Interrupt request register 133	IR133	8	8	2 ICLK		
0008 7086h	ICU	Interrupt request register 134	IR134	8	8	2 ICLK		
0008 7087h	ICU	Interrupt request register 135	IR135	8	8	2 ICLK		
0008 7088h	ICU	Interrupt request register 136	IR136	8	8	2 ICLK		
0008 7089h	ICU	Interrupt request register 137	IR137	8	8	2 ICLK		
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8	2 ICLK		
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8	2 ICLK		
0008 708Ch	ICU	Interrupt request register 140	IR140	8	8	2 ICLK		
0008 708Dh	ICU	Interrupt request register 141	IR141	8	8	2 ICLK		
0008 708Eh	ICU	Interrupt request register 142	IR142	8	8	2 ICLK		
0008 708Fh	ICU	Interrupt request register 143	IR143	8	8	2 ICLK		
0008 7090h	ICU	Interrupt request register 144	IR144	8	8	2 ICLK		
0008 7091h	ICU	Interrupt request register 145	IR145	8	8	2 ICLK		
0008 7092h	ICU	Interrupt request register 146	IR146	8	8	2 ICLK		
0008 7093h	ICU	Interrupt request register 147	IR147	8	8	2 ICLK		
0008 7094h	ICU	Interrupt request register 148	IR148	8	8	2 ICLK		
0008 7095h	ICU	Interrupt request register 149	IR149	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (50/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
007F C402h	FLASH	Flash mode register	FMODR	8	8	2 to 4 FCLK	2, 3 ICLK	Flash Memory
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2 to 4 FCLK	2, 3 ICLK	
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2 to 4 FCLK	2, 3 ICLK	
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2 to 4 FCLK	2, 3 ICLK	
007F C440h	FLASH	E2 DataFlash read enable register 0	DFLRE0	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C442h	FLASH	E2 DataFlash read enable register 1	DFLRE1	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C450h	FLASH	E2 DataFlash P/E enable register 0	DFLWE0	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C452h	FLASH	E2 DataFlash P/E enable register 1	DFLWE1	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2 to 4 FCLK	2, 3 ICLK	
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2 to 4 FCLK	2, 3 ICLK	
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFCAh	FLASH	E2 data flash blank check control register	DFLBCCNT	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFCEh	FLASH	E2 DataFlash blank check status register	DFLBCSTAT	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2 to 4 FCLK	2, 3 ICLK	
FEFF FAC0h	FLASH	Unique ID register 0*8	UIDR0	8	8	1 ICLK	1 ICLK	
FEFF FAC1h	FLASH	Unique ID register 1*8	UIDR1	8	8	1 ICLK	1 ICLK	
FEFF FAC2h	FLASH	Unique ID register 2*8	UIDR2	8	8	1 ICLK	1 ICLK	
FEFF FAC3h	FLASH	Unique ID register 3*8	UIDR3	8	8	1 ICLK	1 ICLK	
FEFF FAC4h	FLASH	Unique ID register 4*8	UIDR4	8	8	1 ICLK	1 ICLK	
FEFF FAC5h	FLASH	Unique ID register 5*8	UIDR5	8	8	1 ICLK	1 ICLK	
FEFF FAC6h	FLASH	Unique ID register 6*8	UIDR6	8	8	1 ICLK	1 ICLK	
FEFF FAC7h	FLASH	Unique ID register 7*8	UIDR7	8	8	1 ICLK	1 ICLK	
FEFF FAC8h	FLASH	Unique ID register 8*8	UIDR8	8	8	1 ICLK	1 ICLK	
FEFF FAC9h	FLASH	Unique ID register 9*8	UIDR9	8	8	1 ICLK	1 ICLK	
FEFF FACAh	FLASH	Unique ID register 10*8	UIDR10	8	8	1 ICLK	1 ICLK	
FEFF FACBh	FLASH	Unique ID register 11*8	UIDR11	8	8	1 ICLK	1 ICLK	
FEFF FACCh	FLASH	Unique ID register 12*8	UIDR12	8	8	1 ICLK	1 ICLK	
FEFF FACDh	FLASH	Unique ID register 13*8	UIDR13	8	8	1 ICLK	1 ICLK	
FEFF FACEh	FLASH	Unique ID register 14*8	UIDR14	8	8	1 ICLK	1 ICLK	
FEFF FACFh	FLASH	Unique ID register 15*8	UIDR15	8	8	1 ICLK	1 ICLK	
FEFF FAD2h	TEMPS	Temperature sensor calibration data register*8	TSCDRL	8	8	1 ICLK	1 ICLK	Temperature sensor
FEFF FAD3h	TEMPS	Temperature sensor calibration data register*8	TSCDRH	8	8	1 ICLK	1 ICLK	

Note 1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 000881ECh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 000881EEh and 000881ECh, respectively.

Note 2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRL address is 000881EDh. When different output triggers are specified, the PPG0.NDRL addresses for pulse output groups 0 and 1 are 000881EFh and 000881EDh, respectively.

Note 3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 000881FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 000881FEh and 000881FCh, respectively.

Note 4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRL address is 000881FDh. When different output triggers are specified, the PPG1.NDRL addresses for pulse output groups 4 and 5 are 000881FFh and 000881FDh, respectively.

Note 5. Odd addresses should not be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register. Table 27.4 lists register allocation for 16-bit access in the User's manual: Hardware.

Note 6. When the register is accessed while the USB is operating, a delay may be generated in accessing.

Note 7. The addresses with odd number cannot be accessed in 16-bit units. 16-bit access to a register should be made to the addresses of the TMOCNTL register. Allocation of registers to be accessed in 16-bit units is described in the Table 36.6, Allocation of Registers to be Accessed in 16-bit Units in the User's manual: Hardware.

Note 8. These registers are only present in the G version.

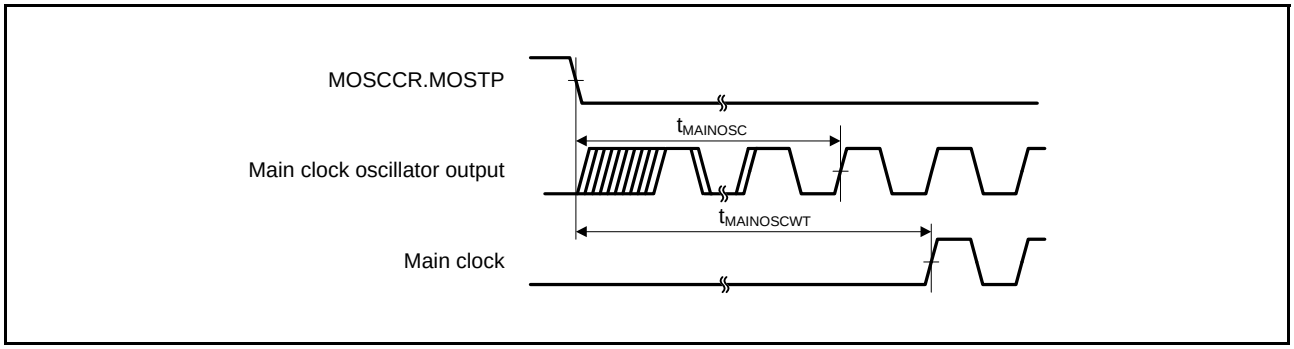


Figure 5.5 Main Clock Oscillation Start Timing

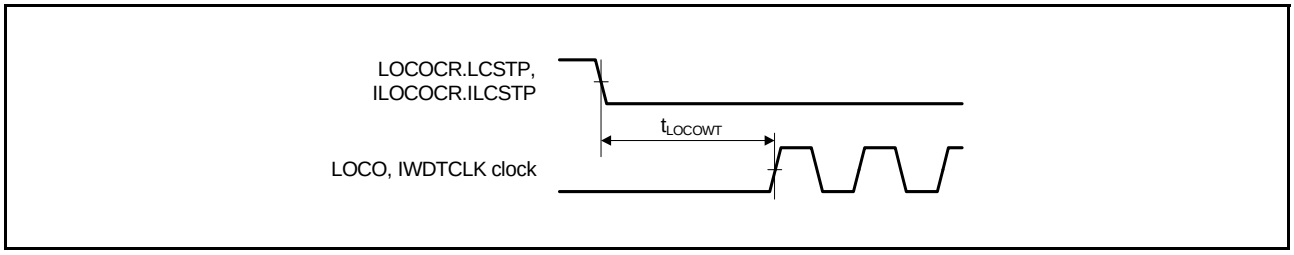


Figure 5.6 LOCO, IWDTCLK Oscillation Start Timing

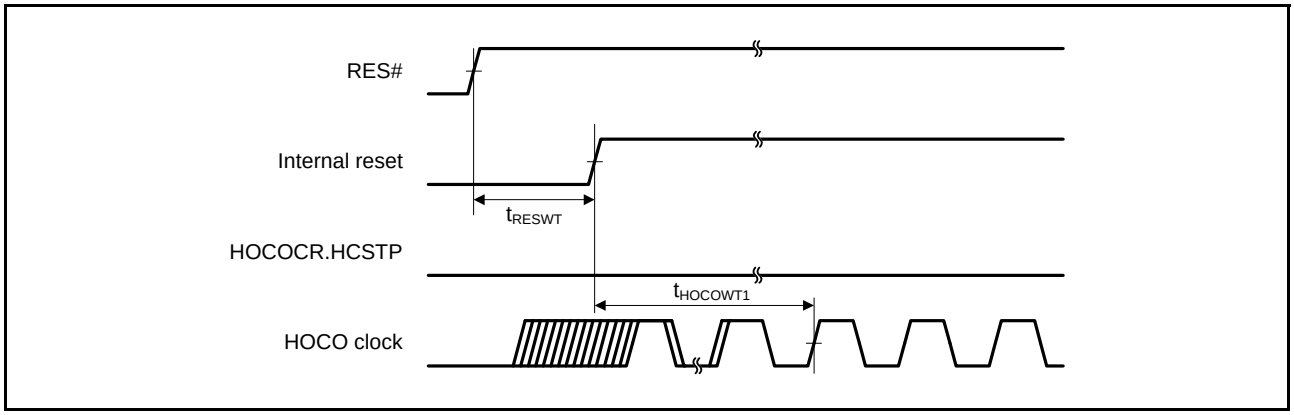


Figure 5.7 HOCO Oscillation Start Timing (After Reset is Canceled by Setting the OFS1.HOCOEN Bit to 0)

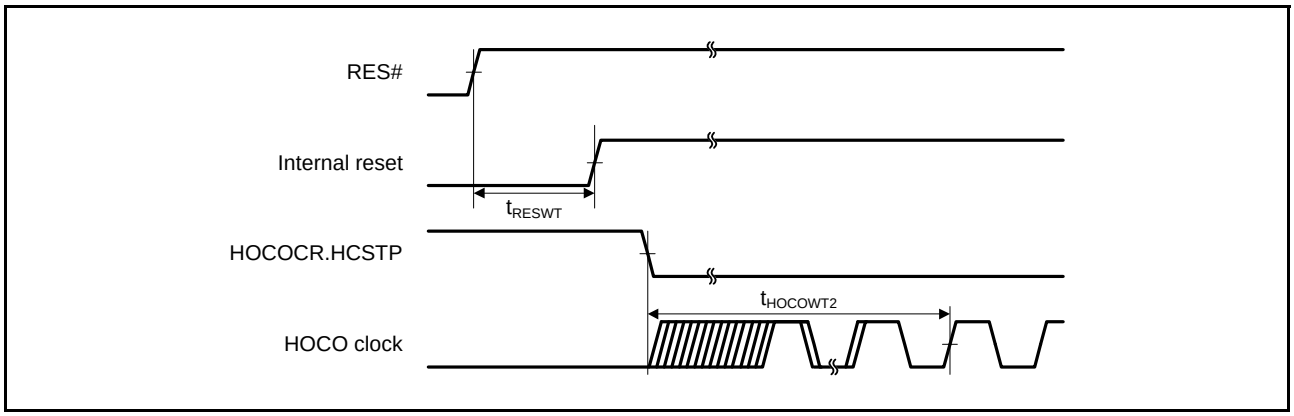
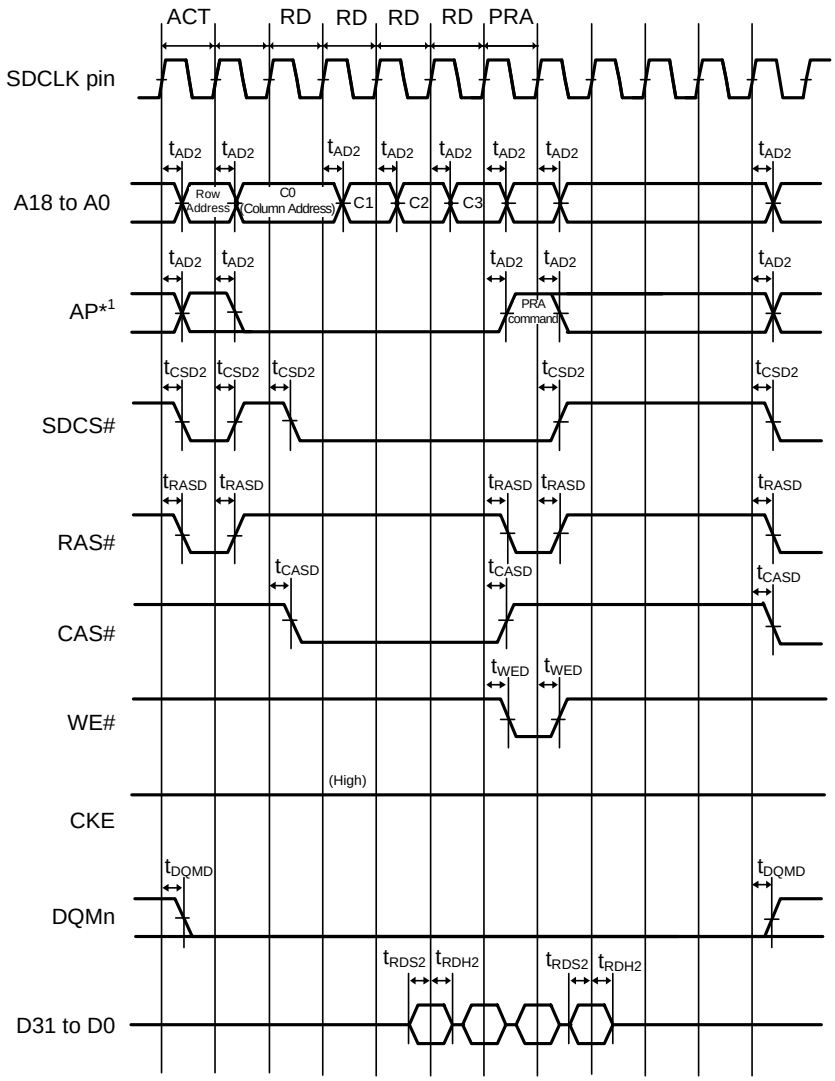


Figure 5.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.26 SDRAM Space Multiple Read Bus Timing

Table 5.26 Timing of On-Chip Peripheral Modules (8)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V, PIXCLK = 27MHz, $T_a = T_{opr}$

Item		Symbol	min	typ	max	Unit	Test Conditions
PDC	VSYNC/HSYNC input setup time	$t_{SYNCSETUP}$	10	—	—	ns	Figure 5.58
	VSYNC/HSYNC input hold time	$t_{SYNCHOLD}$	5	—	—	ns	
	PIXD input setup time	$t_{DATASETUP}$	10	—	—	ns	
	PIXD input hold time	$t_{DATAHOLD}$	5	—	—	ns	
	PIXCLK input cycle time	t_{PIXcyc}	37	—	1000	ns	Figure 5.59
	PIXCLK input pulse width high level	t_{PIXH}	10	—	—	ns	
	PIXCLK input pulse width low level	t_{PIXL}	10	—	—	ns	
	PCKO pin output cycle time	t_{PCKcyc}	40	—	1000	ns	Figure 5.60
	PCKO pin output high level pulse width	t_{PCKH}	13	—	—	ns	
	PCKO pin output low level pulse width	t_{PCKL}	13	—	—	ns	
	PCKO pin output rising time	t_{PCKr}	—	—	5	ns	
	PCKO pin output falling time	t_{PCKf}	—	—	5	ns	

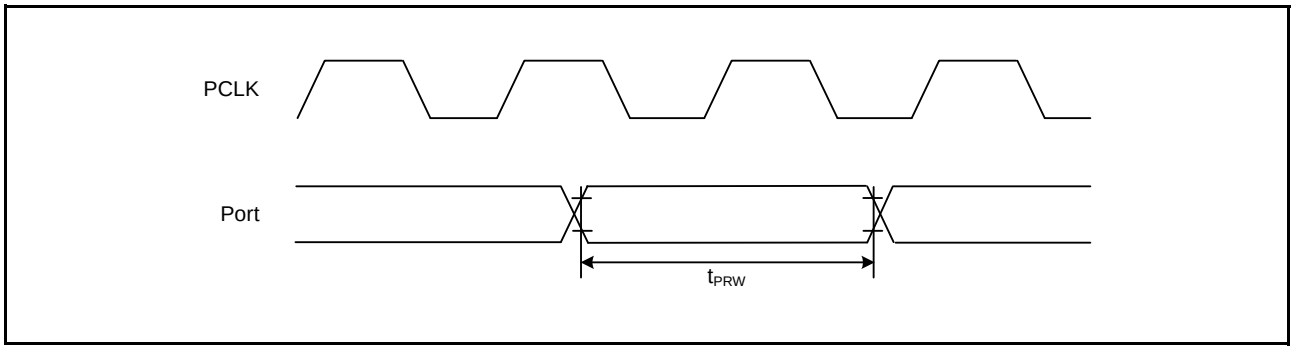


Figure 5.34 I/O Port Input Timing

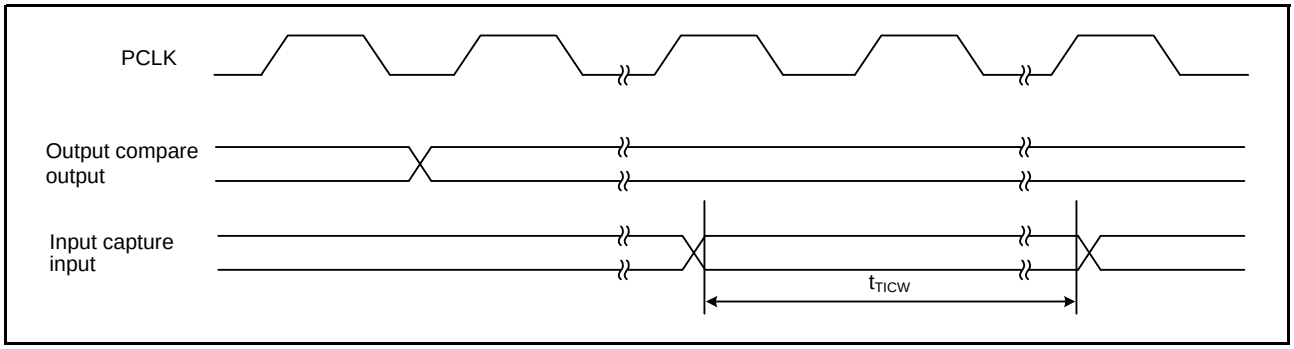
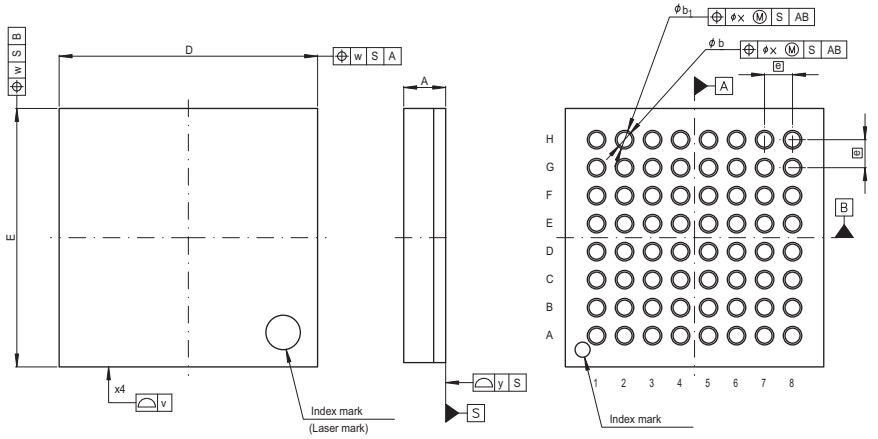


Figure 5.35 MTU Input/Output Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA64-6x6-0.65	PTLG0064JA-A	64F0G	0.07g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.0	—
E	—	6.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.39	0.43	0.47
x	—	—	0.08
y	—	—	0.10

Figure H 64-pin TFLGA (PTLG0064JA-A)

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.80	May 13. 2014	Features		
		1	Operating temp. range chaged, Unique ID added	
		1. Overview		
		2 to 7	Table 1.1 Outline of Specifications: Operating temperature changed, Unique ID and Note 2, added	
		8	Table 1.2 Comparison of Functions for Different Packages: Unique ID, added	
		9 to 16	Table 1.3 List of Products, changed and Note 2, added	TN-RX*-A092A/J
		17	Figure 1.1 How to Read the Product Part Number: Operating temperature range, changed	
		19, 23	Table 1.4 Pin Functions: VBATT and USB power pins, changed	
		3. Address Space		
		76	Figure 3.1 Memory Map in Each Operating Mode, changed	TN-RX*-A081A/E
		77	Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode), changed	TN-RX*-A081A/E
		5. Electrical Characteristics		
		130	Table 5.1 Absolute Maximum Ratings: Operating temperature, changed	
		131	Table 5.2 DC Characteristics (1): Note 1, chaged	
		133 to 134	Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C)): Title	
		135 to 136	Table 5.5 DC Characteristics (4) (for G Version (-85 < Ta ≤ +105°C)), added	
		1921	Table 5.12 Clock Timing (Except for Sub-Clock Related): LOCO changed to LOCO and IWDTCLKB	TN-RX*-A097A/J
		144	Figure 5.6 LOCO, IWDTCLK Clock Oscillation Start Timing, added	TN-RX*-A097A/J
		189	Figure 5.68 Battery Backup Function Characteristics changed	

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.